4000 Series CMOS Logic

1984

Solid State Scientific

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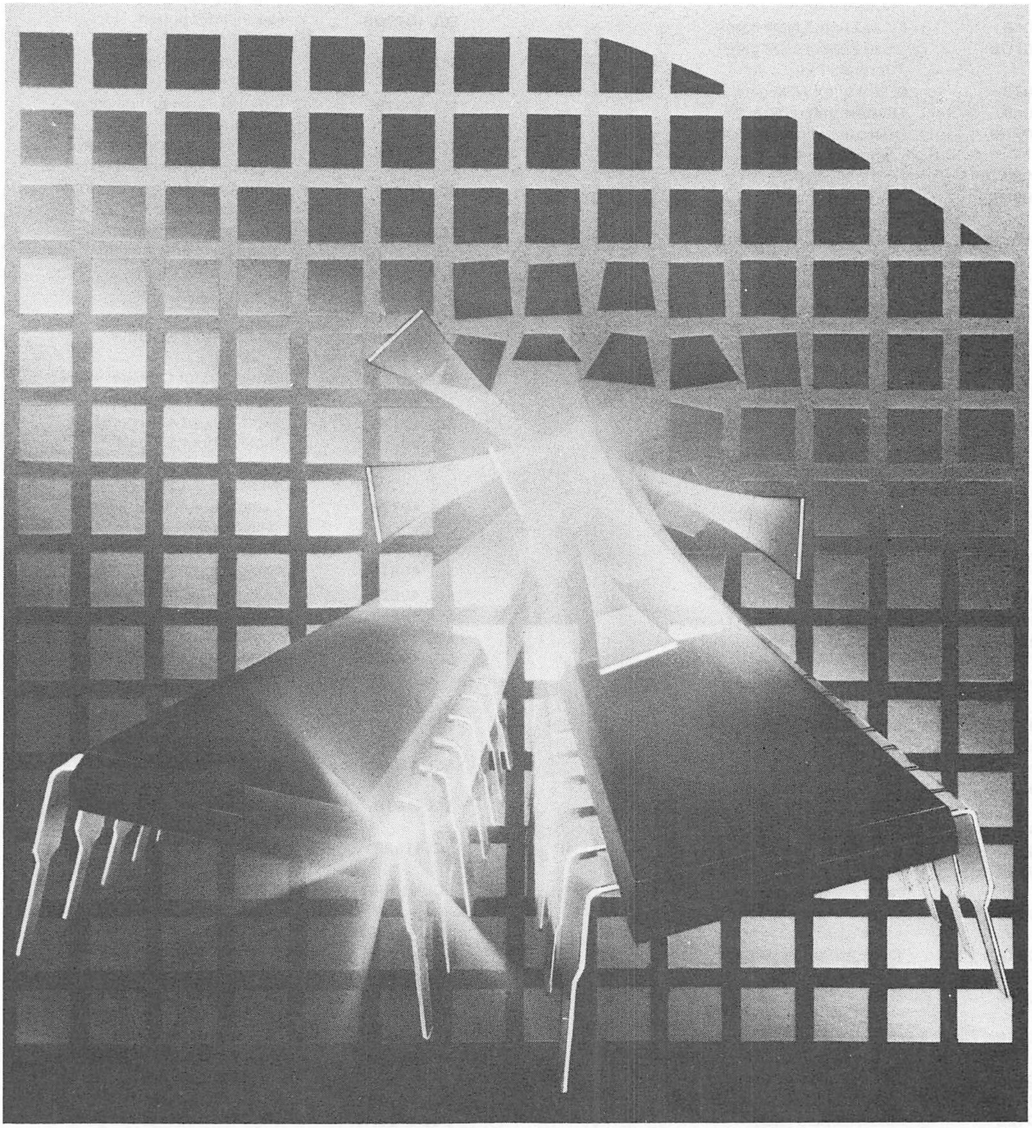

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NUMERICAL DEVICE INDEX

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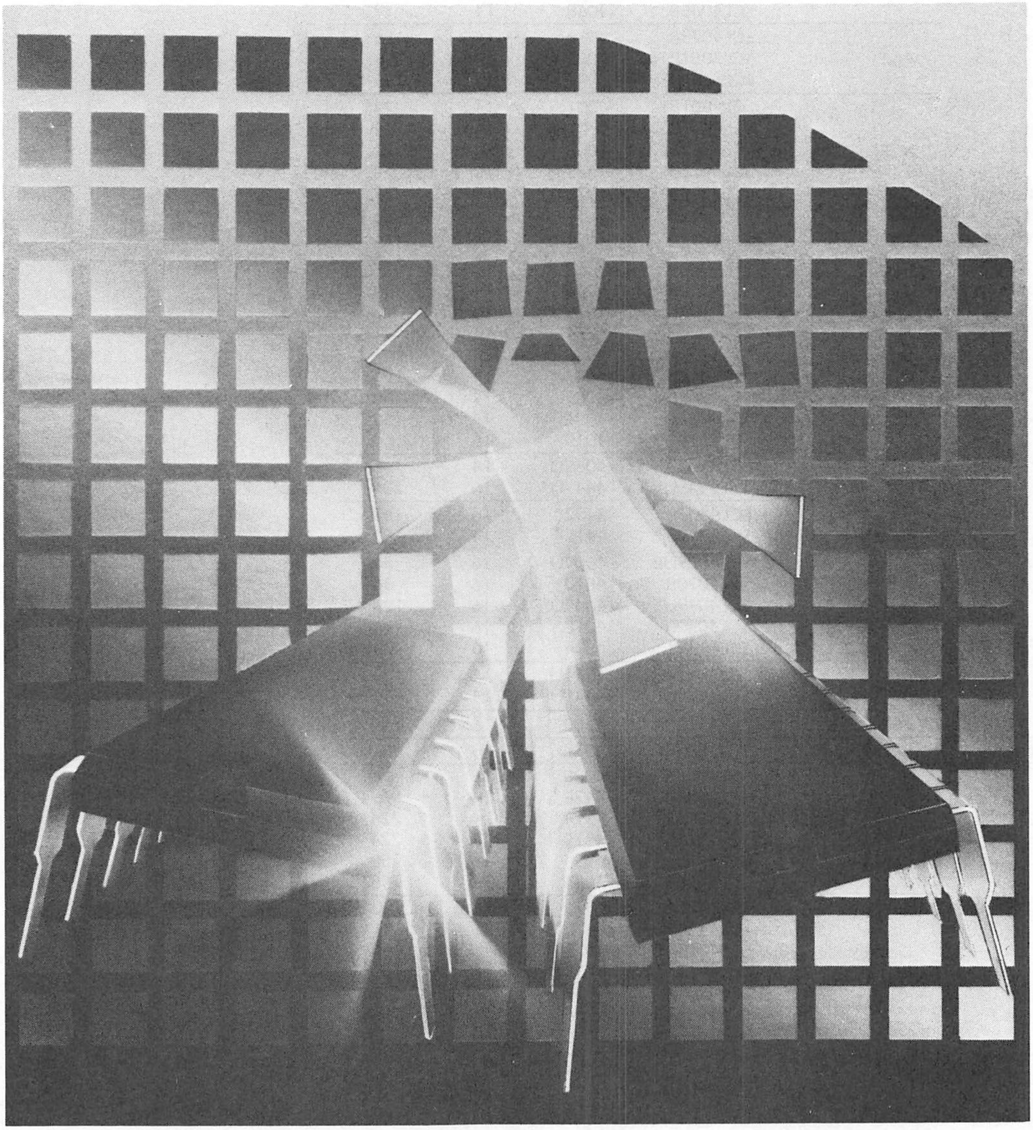

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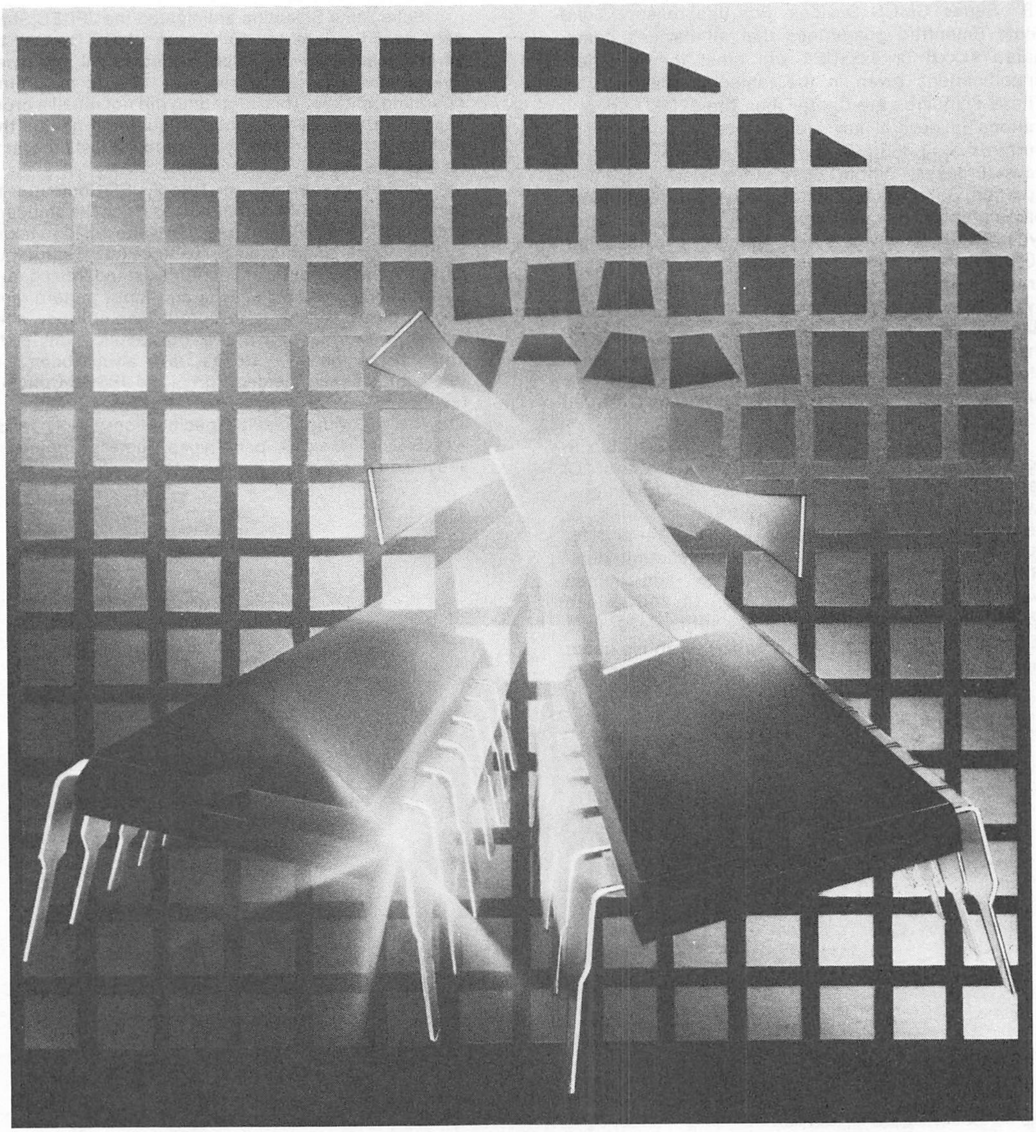
* Part Number is a sole source item of Solid State Scientific.

Family Specifications



THE 4000 SERIES FAMILY

INTRODUCTION

Solid State Scientific CMOS devices comprise a family of medium-speed integrated circuits with a superior combination of high noise immunity, wide operating voltage range, low power dissipation, and high fan-out. These characteristics greatly minimize power supply costs and simplify system design and layout.

The great majority of the devices in the 4000 Series exceed the JEDEC Standard Specifications for "B" Series CMOS Devices. For this reason, Solid State Scientific guarantees that all devices designated 4xxxB or 4xxxUB[1] will meet the electrical specifications given in the tables in this section. These standards are tighter than the JEDEC Specifications in several key areas, notably gate leakage currents (I_{DD}), output voltage (V_{OH}, V_{OL}) and, in several cases, output drive current (I_{OH}, I_{OL}). In addition, Solid State Scientific does not degrade any parameter for any commercial-temperature-range part type. The few device types which fail to meet the 4000B Series Family Specifications for any reason are designated by the suffix AB. These devices, however, are guaranteed to meet all Absolute Maximum Ratings and Recommended Operating Conditions of the 4000B Series, as well as most of the electrical characteristics. Therefore, these few part types are fully compatible with 4000B devices in virtually all applications.

All 4000 Series CMOS devices are available in commercial temperature range (−40°C to +85°C) versions, and a variety of package configurations. Available packages include Frit-seal ceramic or Cerdip dual-in-line packages (C suffix — 14- and 16-lead types), welded-seal or side-brazed ceramic dual-in-line packages (D suffix — 14-, 16-, and 24-lead types), ceramic flat packs (K suffix — 14- and 16-lead types), leadless chip carriers (L suffix — 20 lead JEDEC), and bare chip form (H suffix) for those users manufacturing hybrid microcircuits. Commercial temperature range devices are available in the Epoxy or plastic dual-in-line package (E suffix — 14-, 16- and 24-lead types). Since electrical parameters are never degraded for devices in this package, any mix of packages may be used in a system with confidence that they will be fully compatible throughout the entire range of valid operating conditions.

THE 4000B SERIES

Solid State Scientific anticipated the JEDEC Standard Specifications for "B" Series CMOS Devices by several years in several important areas. All part types have been consistently rated at 18 Vdc maximum operating voltage. This upgrading did not entail a process alteration; performance specifications for the higher voltages were simply added to the test programs for each device.

In addition, the decision of the JEDEC Committee to consider devices with buffered outputs as the standard part types in the "B" Series supports the position taken by Solid State Scientific in 1970. Since buffered-output gates exhibit higher noise immunity, standardized output drive independent of type and input pattern, and decreased ac sensitivity to output loading, they offer superior performance in digital logic applications. Gate functions in the 4000 Series have always been buffered, anticipating the decision of the JEDEC Committee by a full six years.

The following Family Specifications apply to all 4xxxB and 4xxxUB part types, unless otherwise specified on individual data sheets.

[1]As defined in JEDEC Standard Specification

4000B SERIES
FAMILY SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS [1]

DC Supply Voltage	V_{DD}	−0.5 to +18	Vdc
Input Voltage	V_{IN}	−0.5 to V_{DD} +0.5	Vdc
DC Input Current (any one input)	I_{IN}	±10	mAdc
Power Dissipation	P_T	300	mW
Storage Temperature Range	T_S	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS[1]

DC Supply Voltage	V_{DD}	3 to 15	Vdc
Operating Temperature Range	T_A		
C,D,F packages, chips		−55 to +125	°C
E package		−40 to +85	°C

[1]Voltage referenced to V_{SS}

Parametric limits are guaranteed for V_{DD} = 5, 10, and 15 Vdc. Where low power is required, the lowest supply voltage, consistent with required speed, should be used. For larger noise immunity and higher speed, higher supply voltages should be specified. The lower limit of supply regulation is 3 Vdc or as determined by required system speed, noise immunity, or interface to other logic. The recommended upper limit is 15 Vdc or as determined by power dissipation restrictions or interface to other logic.

Unused inputs must be connected to V_{DD}, V_{SS}, or another input.

Care should be used in handling CMOS devices; static charges may damage the device.

ELECTRICAL SPECIFICATIONS

Parametric limits listed here are guaranteed for the entire 4000B Series Family unless otherwise specified on the individual data sheets.

STATIC CHARACTERISTICS (V_{SS} = 0V)

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[1]		+25°C			T_{HIGH}[1]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}										
Gates		5		–	0.05	–	0.0005	0.05	–	1.5	μAdc
		10		–	0.1	–	0.001	0.1	–	3.0	
		15	V_{IN}=V_{SS} or V_{DD}	–	0.2	–	0.002	0.2	–	6.0	
Buffers, Flip-Flops		5	All valid input	–	1.0	–	0.005	1.0	–	30	μAdc
		10	combinations	–	2.0	–	0.01	2.0	–	60	
		15		–	4.0	–	0.02	4.0	–	120	
MSI		5		–	5	–	0.05	5	–	150	μAdc
		10		–	10	–	0.1	10	–	300	
		15		–	20	–	0.2	20	–	600	
HIGH-LEVEL OUTPUT VOLTAGE	V_{OH}	5	V_{IN}=V_{SS} or V_{DD}	4.99	–	4.99	5	–	4.95	–	Vdc
		10		9.99	–	9.99	10	–	9.95	–	
		15	$\|I_O\| \leq 1\mu A$	14.99	–	14.99	15	–	14.95	–	
LOW-LEVEL OUTPUT VOLTAGE	V_{OL}	5	V_{IN}=V_{SS} or V_{DD}	–	0.01	–	0	0.01	–	0.05	Vdc
		10		–	0.01	–	0	0.01	–	0.05	
		15	$\|I_O\| \leq 1\mu A$	–	0.01	–	0	0.01	–	0.05	
MINIMUM INPUT HIGH VOLTAGE	V_{IH}	5	V_O=0.5V or 4.5V	–	3.5	–	2.75	3.5	–	3.5	Vdc
		10	V_O=1.0V or 9.0V	–	7.0	–	5.5	7.0	–	7.0	
		15	V_O=1.5V or 13.5V	–	11.0	–	8.25	11.0	–	11.0	
			$\|I_O\| \leq 1\mu A$								

[1] T_{LOW} = -55°C for C, D, F, and H devices
= -40°C for E device

T_{HIGH} = +125°C for C, D, F, and H devices
= +85°C for E device

STATIC CHARACTERISTICS (V_{SS} = 0V) Continued

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[1]		+25°C			T_{HIGH}[1]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
MAXIMUM INPUT LOW VOLTAGE	V_{IL}	5	V_O=0.5V or 4.5V	1.5	–	1.5	2.25	–	1.5	–	Vdc
		10	V_O=1.0V or 9.0V	3.0	–	3.0	4.5	–	3.0	–	
		15	V_O=1.5V or 13.5V	4.0	–	4.0	6.75	–	4.0	–	
			$\|I_O\| \leq 1\mu A$								
OUTPUT HIGH (SOURCE) CURRENT B Series	I_{OH}	5	V_{OH}=4.6V	-0.64	–	-0.51	-1.25	–	-0.36	–	mAdc
		10	V_{OH}=9.5V	-1.6	–	-1.3	-3.25	–	-0.9	–	
		15	V_{OH}=13.5V	-4.2	–	-3.4	-10	–	-2.4	–	
			$V_{IN}=V_{SS}$ or V_{DD}								
OUTPUT LOW (SINK) CURRENT B Series	I_{OL}	5	V_{OL}=0.4V	0.64	–	0.51	1.25	–	0.36	–	mAdc
		10	V_{OL}=0.5V	1.6	–	1.3	3.25	–	0.9	–	
		15	V_{OL}=1.5V	4.2	–	3.4	10	–	2.4	–	
			$V_{IN}=V_{SS}$ or V_{DD}								
INPUT CURRENT	I_{IN}	15	V_{IN}=0 or 15V	–	±0.1	–	$\pm10^{-5}$	±0.1	–	±1.0	μAdc

[1] T_{LOW} = -55°C for C, D, F, and H devices
= -40°C for E device
T_{HIGH} = +125°C for C, D, F, and H devices
= +85°C for E device

DYNAMIC CHARACTERISTICS (T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
INPUT CAPACITANCE	C_{IN}	–	–	5	7.5	pF

Part types designated "UB"[1] meet the above parametric specifications with the following exception, unless otherwise specified on the individual data sheets.

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[1]		+25°C			T_{HIGH}[1]		Unit
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
MINIMUM INPUT HIGH VOLTAGE	V_{IH}	5	V_O=0.5V or 4.5V	–	4.0	–	2.75	4.0	–	4.0	Vdc
		10	V_O=1.0V or 9.0V	–	8.0	–	5.5	8.0	–	8.0	
		15	V_O=1.5V or 13.5V	–	12.0	–	8.25	12.0	–	12.0	
			$\|I_O\| \leq 1\mu A$								
MAXIMUM INPUT LOW VOLTAGE	V_{IL}	5	V_O=0.5V or 4.5V	1.0	–	1.0	2.25	–	1.0	–	Vdc
		10	V_O=1.0V or 9.0V	2.0	–	2.0	4.5	–	2.0	–	
		15	V_O=1.5V or 13.5V	3.0	–	3.0	6.75	–	3.0	–	
			$\|I_O\| \leq 1\mu A$								

[1] T_{LOW} = -55°C for C, D, F, and H devices
= -40°C for E device
T_{HIGH} = +125°C for C, D, F, and H devices
= +85°C for E device

The user should consult the section of this book entitled "CMOS Design Considerations" in conjunction with the Family Specifications given here to assure proper system performance.

[1]As defined in JEDEC Standard Specification

PARAMETER DEFINITIONS AND WAVEFORMS

DEFINITIONS

The following information provides detailed explanations of the electrical parameters specified on 4000 Series data sheets. These parameters are categorized into Absolute Maximum Ratings, Recommended Operating Conditions, Static Electrical Characteristics, and Dynamic Electrical Characteristics. Virtually all devices in the 4000 Series are fully described by a combination of the parameters identified in this section; in a few special cases, however, parameters unique to a device are defined on the individual data sheet.

While all parameters exhibit a statistical distribution about a mean value, only the mean value and one worst-case limit — either the minimum or the maximum value — appears on the data sheet. Following the EIA standard guidelines, the minimum limit value is always less than the mean or typical value, and the maximum limit value is always greater than the typical value. Several parameters, therefore, require the prefix "minimum" or "maximum" in order to maintain the proper convention on the data sheet. These prefixes should not be confused with the minimum and maximum designations applied to limit values. Thus, "maximum clock frequency" has minimum limit values specified, while "minimum clock pulse width" has maximum limit values specified.

Each parameter is measured under a specified set of conditions: supply voltage, input voltages and currents, output voltages and currents, input signal switching characteristics, etc. To assist the designer in constructing his system, any given parameter is measured under the same test conditions for all devices in the 4000 Series, whether they fall into the B, UB, or AB designation.

ABSOLUTE MAXIMUM RATINGS

These ratings are absolute limits within which safe operation occurs. The presence of conditions outside these limits may cause severe device degradation, and possibly catastrophic failure. These ratings apply across the entire temperature range.

DC Supply Voltage Range

To prevent forward biasing and possibly damaging the structural and protective diode junctions present in CMOS construction, V_{DD} must never be more than 0.5Vdc negative with respect to V_{SS}.

The maximum limit of 18Vdc prevents primary breakdown of any internal device junction.

Input Voltage Range

The voltage at any device input must not exceed either the V_{SS} or V_{DD} supply voltages by more than 0.5Vdc. Unrestricted operation outside this range may damage the input protection diodes, or cause internal latch-up.

DC Input Current

To prevent excessive dissipation in the junctions of the protection diodes, input current must be limited to less than 10mAdc.

Maximum Package Power Dissipation

This requirement prevents excessive junction or package temperatures from developing. The maximum rating of 300mW includes both quiescent (dc) and dynamic (ac) dissipation, and should be calculated from the discussion of Power Dissipation in the section entitled "Design Considerations."

Storage Temperature Range

The temperature range within which devices may be stored without electrical connection is −65°C to +150°C. Device reliability may be degraded when stored outside this range.

RECOMMENDED OPERATING CONDITIONS

These conditions specify ranges within which reliable operations may be maintained. Systems utilizing CMOS should be designed to operate within these ranges.

DC Supply Voltage Range

The lower limit of 3Vdc is based upon transistor threshold levels. The recommended maximum limit of 15V is substantially below the primary breakdown limit for the devices to allow for limited power-supply transient and regulation limits.

Operating Temperature Range

The maximum ambient temperature range within which the device may be reliably operated is −55°C to +125°C (the standard military temperature range) for the C, D, and F packages, and −40°C to +85°C (an extended commercial range) for the E package. Chips (H suffix) may be operated over the full military temperature range, −55°C to +125°C.

STATIC ELECTRICAL CHARACTERISTICS

These parameters apply to devices in the steady-state condition. They are specified at the low temperature limits (−55°C or −40°C), +25°C, and the high temperature limits (+125°C or +85°C), with typical values given at +25°C.

Quiescent Device Current (I_{DD})

Quiescent current is defined as the current flowing into the V_{DD} terminal of the device with no load on the outputs. This current is measured under all valid input combinations (inputs tied in all valid combinations to V_{SS} or V_{DD}). The maximum limit reflects domination by surface leakage effects. Most devices exhibiting typical leakage currents are dominated by junction leakage which doubles with every 11°C increase in temperature.

These values have been standardized into three

categories: gates, buffers and flip-flops, and MSI devices. Solid State Scientific does not degrade this parameter for commercial temperature range devices (E package).

Output Voltage (V_{OH}, V_{OL})

V_{OH} is defined as the high-level output voltage under no-load conditions ($|I_O|<1\mu A$), with inputs tied to V_{SS} or V_{DD}. Similarly, V_{OL} is the low-level output voltage measured under the same conditions. Both parameters are guaranteed to be no more than 0.01Vdc from the supply voltage at low temperature and +25°C, and no more than 0.05Vdc from the supply voltage at high temperature.

Input Voltage (V_{IH}, V_{IL})

V_{IH} and V_{IL} are defined as the minimum input high voltage and the maximum input low voltage, respectively, which produce no more than a 10% V_{DD} change in output voltage under no-load conditions ($|I_O|<1\mu A$). This parameter differentiates device designations "B" and "UB".

In general, "B" devices have greater noise immunity, i.e., lower V_{IH} and higher V_{IL}, than "UB" devices because output buffering more effectively isolates outputs from input voltage variations.

Output Drive Currents (I_{OH}, I_{OL})

Output drive current is the source current (I_{OH}) with the output high, or the sink current (I_{OL}) with the output low, that flows out of or into the device from a load of specific voltage. Polarity is defined as positive when flowing into the output. Inputs are tied directly to V_{SS} or V_{DD}, output voltages are specified at equal voltage drops for both parameters at given supply voltage.

At V_{DD} = 5Vdc, I_{OH} and I_{OL} are specified at V_{OH} = 4.6Vdc and V_{OL} = 0.4Vdc, respectively. Logic outputs of "B" and "UB" devices are capable of driving one low-power TTL load across temperature. Although the source current (I_{OH}) specification for these devices is lower than the sink current (I_{OL}) specification (I_{IL} (TTL) >> I_{IH}), many devices in the 4000 Series Family are designed for balanced drives at these output voltages. All gates and flip-flops, and a number of MSI parts, fall into this category; this is noted on the individual data sheets.

At V_{DD} = 10Vdc, an output voltage drop of 0.5Vdc from either supply is used as the standard condition for specifying I_{OH} and I_{OL}.

At V_{DD} = 15Vdc, 1.5Vdc is used as the standard output voltage drop. Current values are designed to drive two standard HTL loads over temperature.

The limits at the temperature extremes reflect the 0.3%/°C current decrease with increasing temperature at 25°C characteristic of CMOS. Most device data sheets supply transistor characteristic curves for determination of output drive current under other operating conditions.

Solid State Scientific does not degrade these parameters for commercial temperature range devices (E package).

3-State Output Leakage Current (I_{ZL})

Leakage current at the output terminal of a 3-state device when disabled (high-impedance state) is measured under the two worst-case conditions: V_{DD} is applied at the output along with input combinations which would normally force the output low; V_{SS} is applied at the output along with input combinations which would normally force the output high.

Solid State Scientific does not degrade this parameter for commercial temperature range devices (E package).

Input Current

Input current is defined as the current that flows into or out of an input terminal when V_{SS} or V_{DD} is applied to that terminal. Input current consists of junction leakages in the diode protection circuit, and is typically ±10pAdc. Worst-case input current is specified at V_{DD} = 15Vdc across temperature, with a maximum of ±1.0uAdc at +125°C (+85°C for commercial temperature range devices).

Solid State Scientific does not degrade this parameter for commercial temperature range devices.

DYNAMIC ELECTRICAL CHARACTERISTICS

Switching characteristics are specified at a total output load capacitance per output C_L =50pF, ambient temperature T_A = 25°C, and input rise and fall times t_r, t_f = 20nS (except for maximum input rise and fall time specifications). Typical temperature coefficient for dynamic characteristics is $|0.3\%/°C|$ (negative for maximum clock frequency (f_{CL}) and positive for other parameters). Solid State Scientific does not degrade dynamic parameters for commercial temperature range devices (E package).

Propagation Delay Time (t_{PLH}, t_{PHL})

These parameters are specified on all data sheets. For non-synchronous circuits and inputs, the delay time is measured from the 50% point of the input signal edge to the 50% point of the resulting output signal edge. For synchronous inputs (having a clock signal), the delay time is measured from the 50% of the clock signal edge associated with the input level to the 50% point of the resulting output signal edge. The designation "LH" refers to the low-to-high output transition; "HL" refers to the high-to-low output transition. Propagation delays increase linearly with load capacitance.

3-State Propagation Delay (t_{PHZ}, t_{PLZ}, t_{PZH}, t_{PZL})

The t_{PHZ} (high-level to 3-state) and t_{PLZ} (low-level to 3-state) propagation delays are measured from the 50% point of the disable input leading edge to the 90% point of the output signal falling edge (t_{PHZ}) or to the 10% point of the output signal rising edge (t_{PLZ}). The t_{PZH} (3-state to high-level) and t_{PZL} (3-state to low-level) propagation delays are measured from the 50% point of the disable input trailing edge to the 10% point of the output signal rising edge (t_{PZH}) or to the 90% point of the output signal falling edge (t_{PZL}). In addition to the 50pF load capacitance, a 1KΩ load resistor is tied to V_{SS} (t_{PHZ} and t_{PZH}) or V_{DD} (t_{PLZ} and t_{PZL}).

Output Transition Time (t_{TLH}, t_{THL})

These parameters refer to the rise (t_{TLH}) and fall (t_{THL}) times at device outputs. They are measured from the 10% to the 90% points of the output waveform. Both parameters are functions of output transistor sizes, and fall into standard categories in the same way as output drive current. Output transition times vary linearly with load capacitance C_L.

Minimum (Clock) Pulse Width (PW)

Minimum pulse width refers to that portion of the input signal between the active (leading) edge and the opposite (trailing) edge. It is defined as the interval between the 50% points of each edge. When applied to clock signals, this parameter also refers to the remaining portion of the signal, i.e., 50% duty cycle.

Maximum Clock Frequency (f_{CL})

The maximum clock frequency is the rate at which information can transfer through a synchronous circuit without developing system problems due to excessive propagation delays across internal stages.

Maximum Clock Rise and Fall Times (t_{rCL}, t_{fCL})

These limits refer to the maximum allowable input transition times which prevent interactions between internal stages from interfering with proper clocking. These parameters are measured from the 10% point to the 90% point of the input signal, and usually decrease with increasing operating voltage.

When synchronous stages are cascaded, however, maximum rise and fall times of the clock input should be equal to or less than the transition times of data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load. This prevents improper operation resulting from logic state interaction between adjoining stages.

Minimum Setup Time (t_{setup})

Setup time refers to the minimum interval between the data or control input signal and the clock or strobe signal which guarantees proper entry of that information into the device. It is measured between the 50% points of the two appropriate edges.

Minimum Hold Time (t_{hold})

Hold time refers to the interval after the clock or strobe edge during which data or control information must remain valid. It is measured between the 50% points of the two appropriate edges.

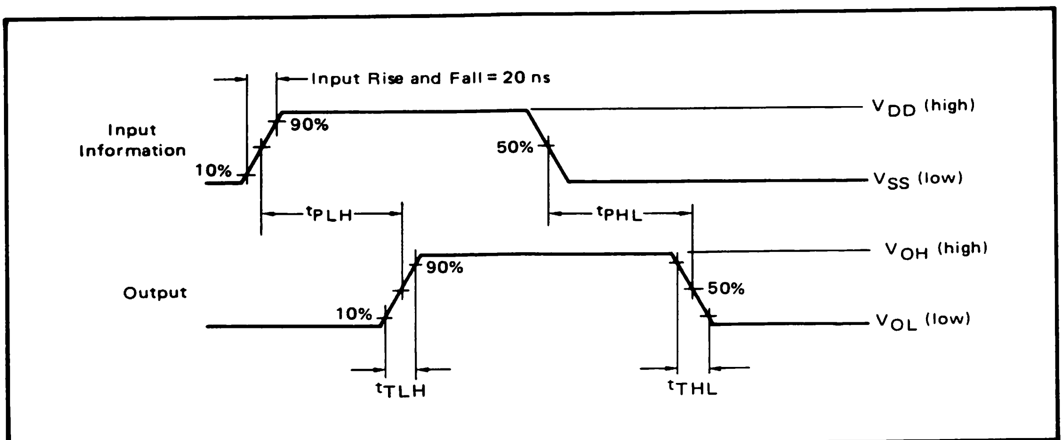
Removal Time (t_{rem})

Removal time is defined as the interval after removing an asynchronous control input during which a clock or strobe signal edge may not be recognized. This parameter is similar to minimum setup time, and is measured from the 50% point of the control input trailing edge to the 50% point of the clock or strobe signal leading edge.

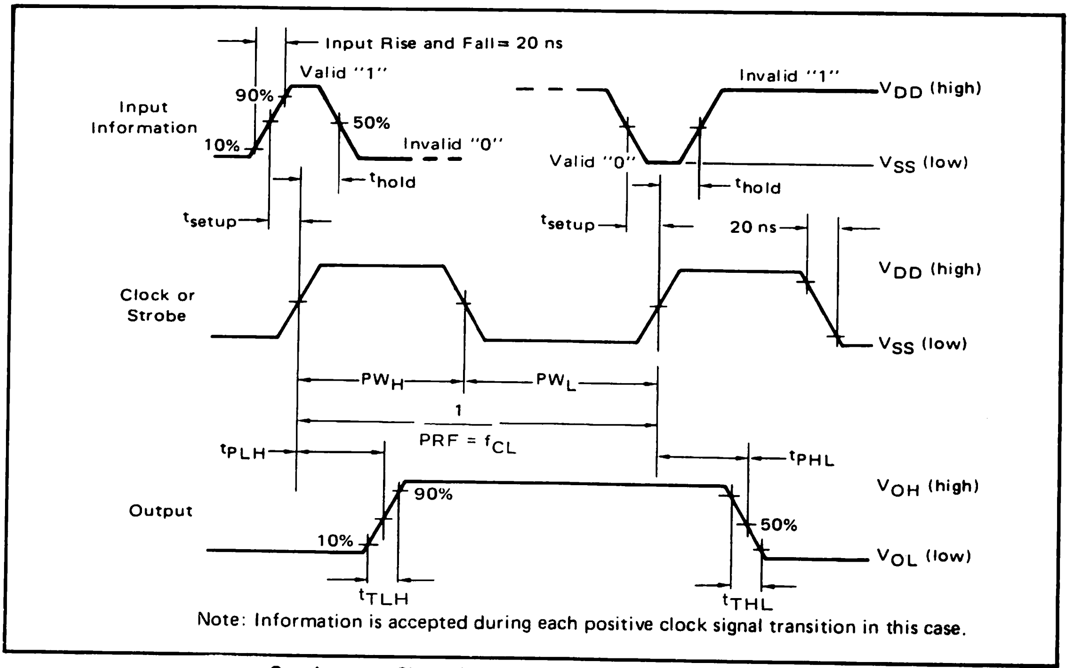
Input Capacitance (C_{IN})

The input capacitance is defined as the ac capacitance under zero bias conditions as applied to any input. This capacitance is typically 5pF for most devices; it is somewhat higher for inputs to high-current buffers.

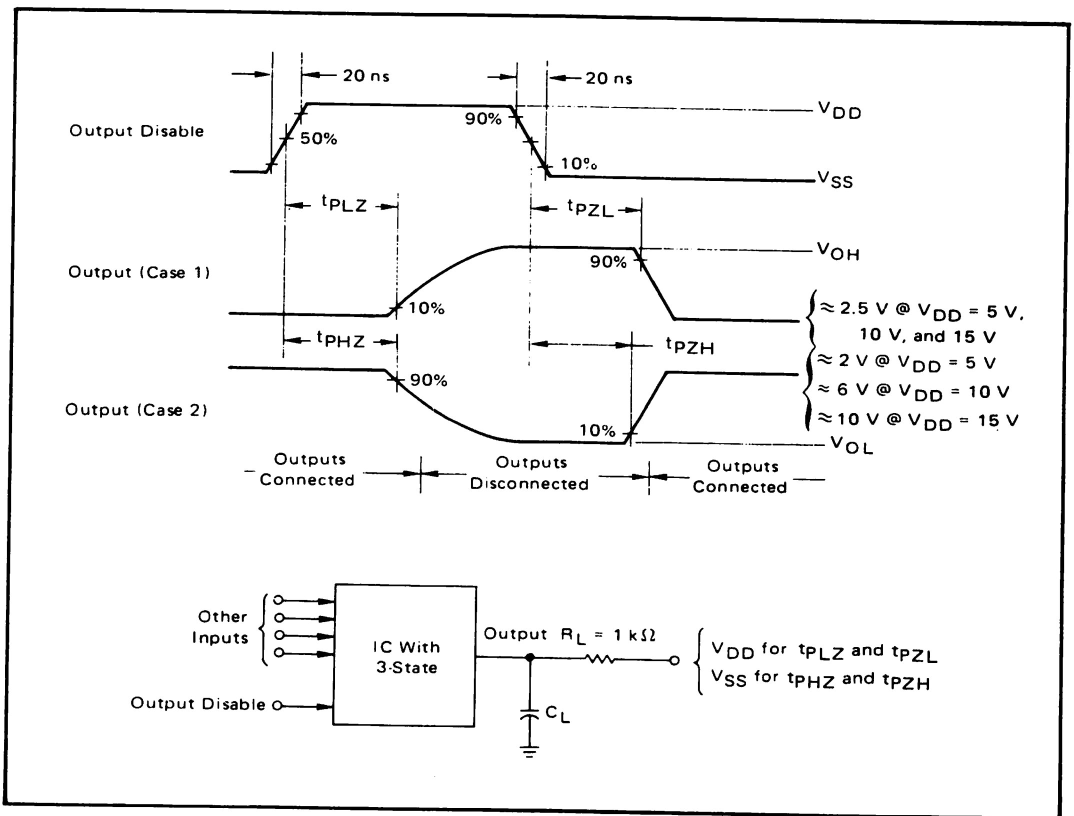
DYNAMIC PARAMETER WAVEFORMS



Non-Synchronous Circuit Waveshapes and Timing Parameters

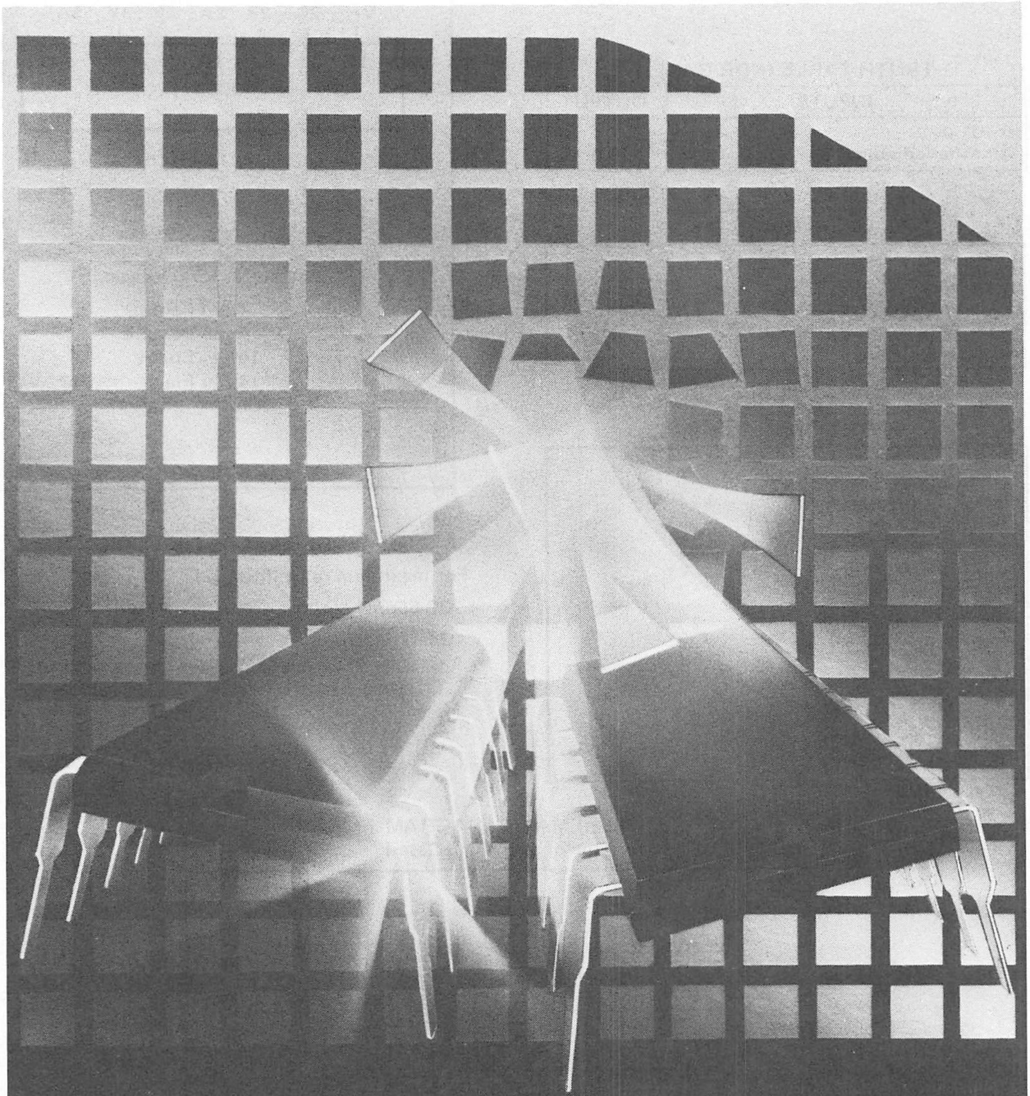


Synchronous Circuit Waveshapes and Timing Parameters



Three-State Propagation Delay Waveshape and Test Circuit

4000 Series Data



SOLID STATE SCIENTIFIC

SCL4000B

CMOS DUAL 3-INPUT NOR GATE PLUS INVERTER

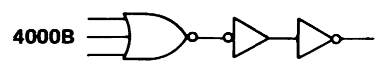
FEATURES

- Buffered Gate Outputs
- Diode Protection on all Inputs
- Fully "B" Series Compatible

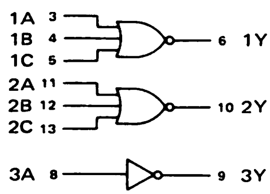
TRUTH TABLE (NOR GATE)

INPUTS	OUTPUT
0 0 0	1
All other combinations	0

LOGIC DIAGRAM



FUNCTION DIAGRAM

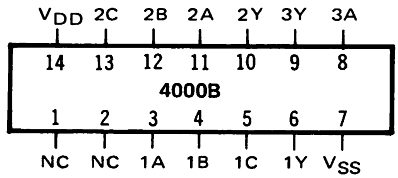


$(1, 2)Y = \overline{A + B + C}$

$3Y = \overline{3A}$

V_{DD} = Pin 14
V_{SS} = Pin 7

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

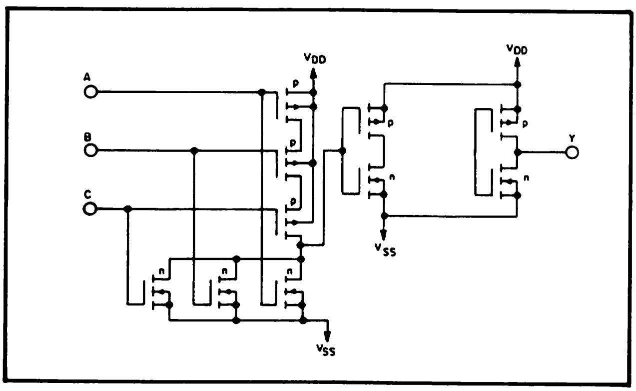
- C 14-pin Cerdip
- D 14-pin Ceramic
- E 14-pin Epoxy
- F 14-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

SCHEMATIC DIAGRAM
(One of two NOR Gates)



ELECTRICAL CHARACTERISTICS

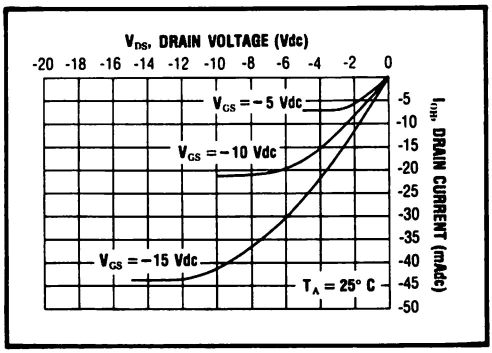
STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[2] Min.	T_{LOW}[2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH}[2] Min.	T_{HIGH}[2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN}=V_{SS}$ or V_{DD}	–	0.05	–	0.0005	0.05	–	1.5	μAdc
		10	All valid input	–	0.10	–	0.001	0.10	–	3.0	
		15	combinations	–	0.20	–	0.002	0.20	–	6.0	

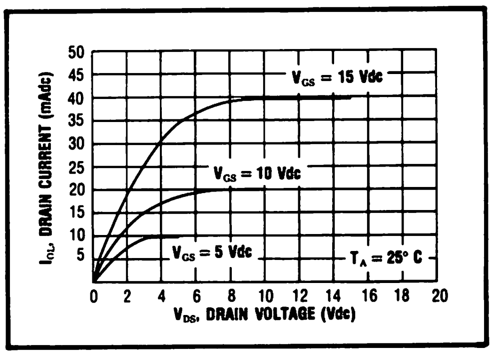
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}	5	–	125	250	ns
		10	–	60	120	
		15	–	45	90	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	



Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

CMOS NOR GATES

4001B – Quad 2-Input NOR
4002B – Dual 4-Input NOR
4025B – Triple 3-Input NOR
4078B – 8-Input NOR

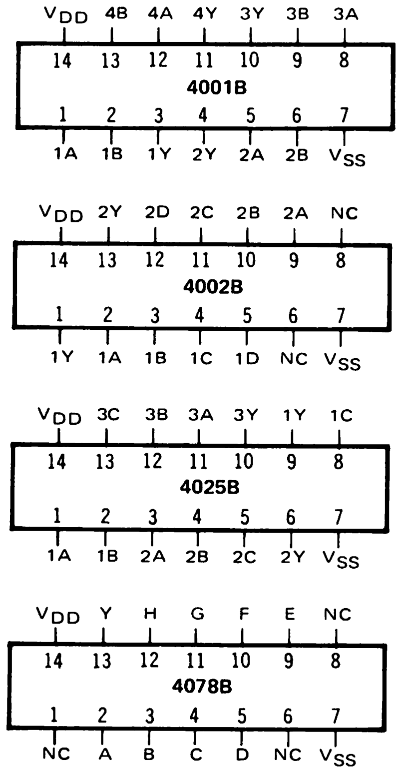
FEATURES

- Buffered Outputs
- Diode Protection on all Inputs
- Fully "B" - Series Compatible

Inputs	Output
0 0 . . . 0	1
All other combinations	0

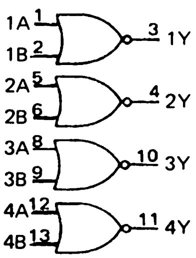
CONNECTION DIAGRAMS

(all packages)



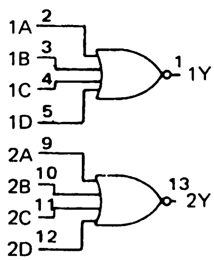
FUNCTION DIAGRAMS

4001B



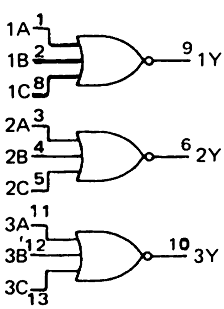
$Y = \overline{A + B}$

4002B



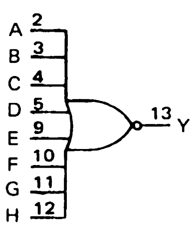
$Y = \overline{A + B + C + D}$

4025B



$Y = \overline{A + B + C}$

4078B



$Y = \overline{A+B+C+D+E+F+G+H}$

V_{DD} = Pin 14
V_{SS} = Pin 7
for All Devices

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

ELECTRICAL CHARACTERISTICS

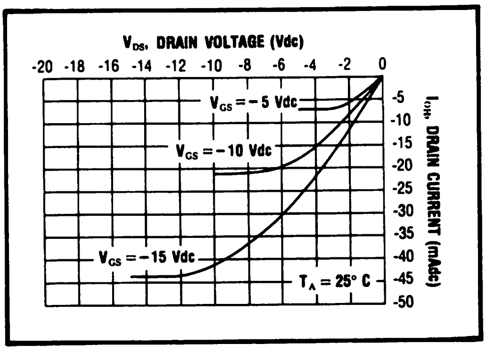
STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[2]		+25°C			T_{HIGH}[2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN}=V_{SS}$ or V_{DD}	–	0.05	–	0.0005	0.05	–	1.5	μAdc
		10	All valid input	–	0.10	–	0.001	0.10	–	3.0	
		15	combinations	–	0.20	–	0.002	0.20	–	6.0	

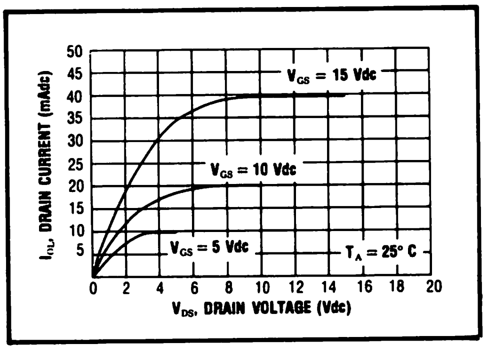
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications."
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}	5	–	125	250	ns
		10	–	60	120	
		15	–	45	90	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	

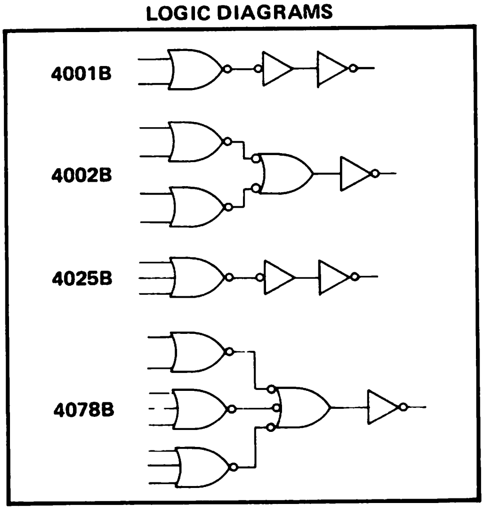


Typical P-Channel
Source Current Characteristics

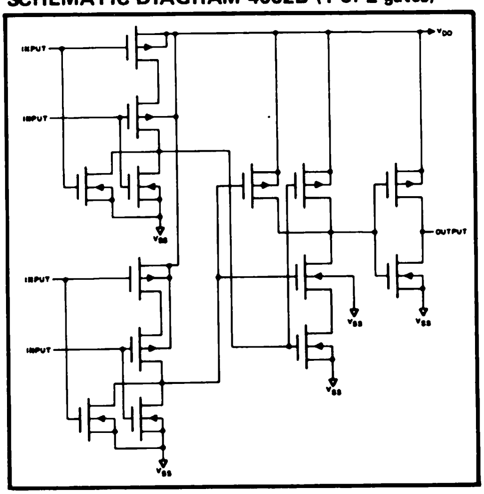


Typical N-Channel
Sink Current Characteristics

LOGIC DIAGRAMS



SCHEMATIC DIAGRAM 4002B (1 of 2 gates)



CMOS NOR GATE (Unbuffered)

FEATURES

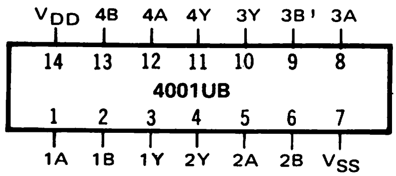
- Unbuffered Outputs for Quasi-Linear Applications
- Quad 2-Input NOR Configuration
- Diode Protection on all Inputs
- Output Drive Current Compatible with "B" Series
- Pin Compatible with Buffered 4001B

DESCRIPTION

The 4001UB consists of four positive-logic NOR gates. The outputs are unbuffered, making the device suitable for quasi-linear applications, such as gated oscillators, multivibrators, and pulse shaping circuits.

For digital applications, the buffered 4001B is recommended for its higher gain and input pattern insensitivity.

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

C	14-pin Cerdip
D	14-pin Ceramic
E	14-pin Epoxy
F	14-pin Flat
H	Chip

TRUTH TABLE

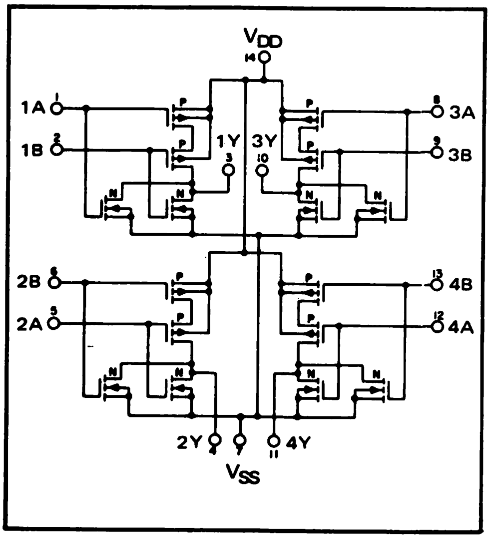
Inputs	Output
0 0	1
All other combinations	0

RECOMMENDED OPERATING CONDITIONS

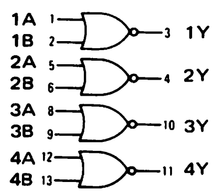
For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

SCHEMATIC DIAGRAM



LOGIC DIAGRAM



$Y = \overline{A + B}$

V_{DD} = Pin 14
V_{SS} = Pin 7

ELECTRICAL CHARACTERISTICS

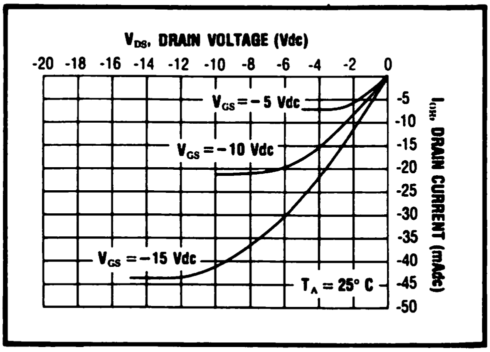
STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2] Min.	T_{LOW} [2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH} [2] Min.	T_{HIGH} [2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN} = V_{SS}$ or V_{DD}	–	0.05	–	0.0005	0.05	–	1.5	μAdc
		10	All valid input	–	0.10	–	0.001	0.10	–	3.0	
		15	combinations	–	0.20	–	0.002	0.20	–	6.0	

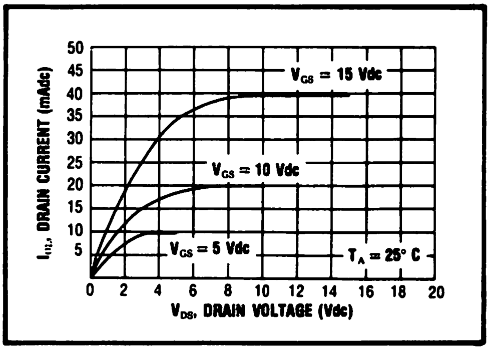
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}	5	–	60	120	ns
		10	–	30	60	
		15	–	25	50	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	

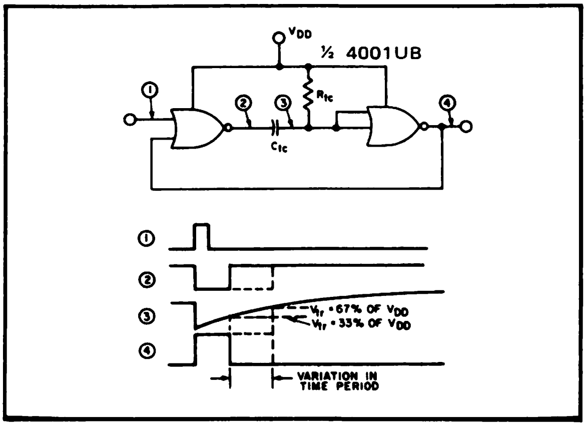


Typical P-Channel
Source Current Characteristics

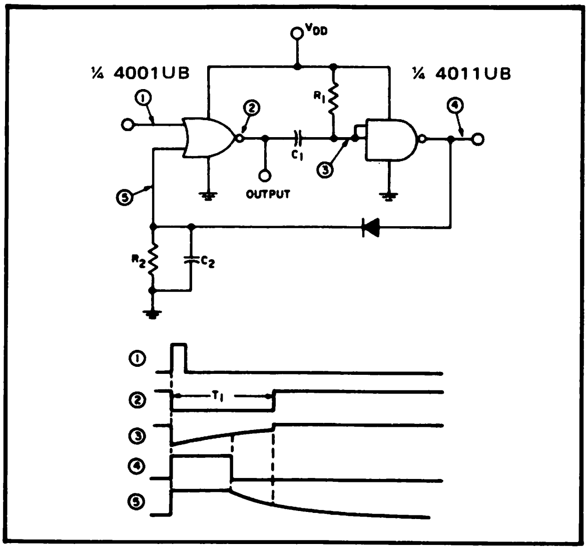


Typical N-Channel
Sink Current Characteristics

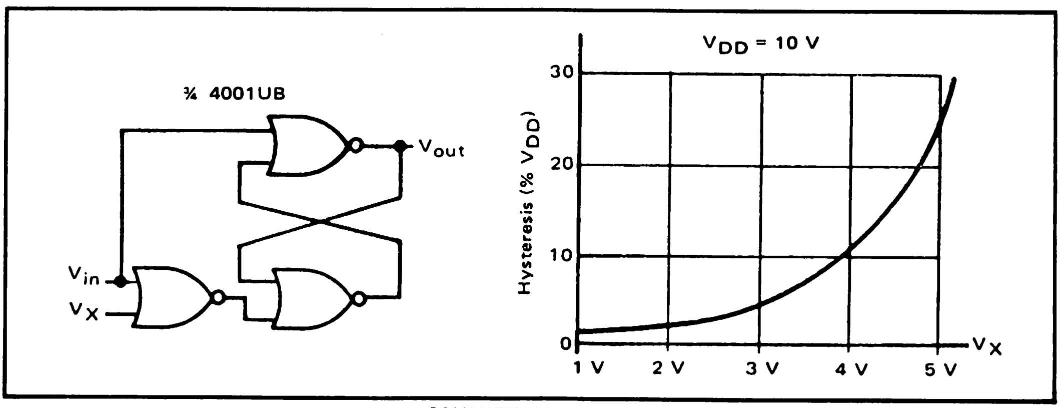
APPLICATIONS INFORMATION



MONOSTABLE MULTIVIBRATOR



COMPENSATED MONOSTABLE MULTIVIBRATOR



SCHMITT TRIGGER

CMOS 18 STAGE SHIFT REGISTER

FEATURES

- Fully Static Operation
- Cascadable
- 5MHz Shift Rate @ 10Vdc

DESCRIPTION

The 4006B is comprised of 4 separate Shift Register sections: two sections of four stages and two sections of five stages with an output tap at the fourth stage. Each section has an independent single rail data path.

A common Clock signal is used for all stages. Data is shifted to the next stage on negative-going transitions of the Clock. Through appropriate connections of inputs and outputs, multiple register sections of 4, 5, 8 and 9 stages or single register sections of 10, 12, 13, 14, 16, 17 and 18 can be implemented using one 4006B package. Longer shift register sections can be assembled by using more than one 4006B.

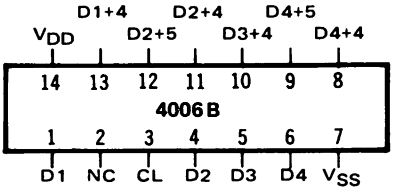
This part is useful in serial shift register and time delay circuits.

TRUTH TABLE

Di	CL	Di + 1
0	↓	0
1	↓	1
X	↑	No Change

X = Don't care

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

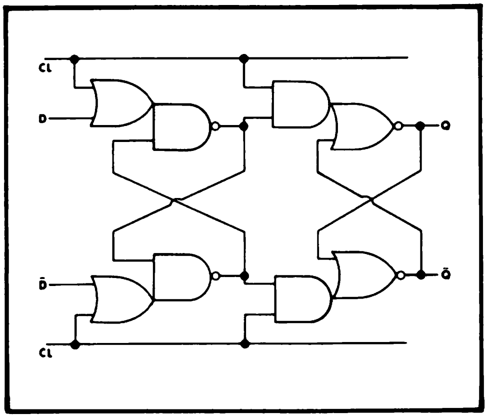
- C 14-pin Cerdip
- D 14-pin Ceramic
- E 14-pin Epoxy
- F 14-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

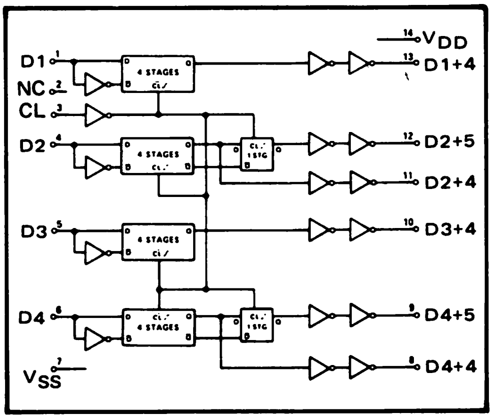
For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

TYPICAL REGISTER STAGE



LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2]		+25°C			T_{HIGH} [2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN}=V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	μAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		15	combinations	–	20	–	0.2	20	–	600	

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}	5	–	250	500	ns
		10	–	125	250	
		15	–	100	200	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
MINIMUM CLOCK PULSE WIDTH	PW_{CL}	5	–	200	400	ns
		10	–	100	200	
		15	–	80	160	
MAXIMUM CLOCK FREQUENCY	f_{CL}	5	1.25	2.5	–	MHz
		10	2.5	5.0	–	
		15	3.0	6.0	–	
MAXIMUM CLOCK RISE AND FALL TIME [1]	t_{rCL}, t_{fCL}	5	15	–	–	μs
		10	5	–	–	
		15	3	–	–	
MINIMUM SETUP TIME	t_{setup}	5	–	40	80	ns
		10	–	25	50	
		15	–	20	40	
MINIMUM HOLD TIME	t_{hold}	5	–	40	80	ns
		10	–	25	50	
		15	–	20	40	

[1] When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.

SOLID STATE SCIENTIFIC

CMOS DUAL COMPLEMENTARY PAIR PLUS INVERTER

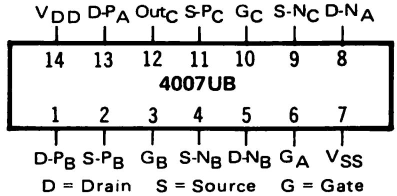
FEATURES

- Low Output Impedance
- Extremely High Input Impedance
- Single Supply Operation - Positive or Negative
- All Inputs Diode-Protected

DESCRIPTION

4007UB contains three N-Channel and three P-Channel enhancement-type MOS transistors on a single monolithic silicon chip. The transistor elements are accessible through the package terminals to provide means for constructing various logic, transmission gating, and linear circuits.

CONNECTION DIAGRAM
(all packages)



D = Drain S = Source G = Gate

Add suffix for package:

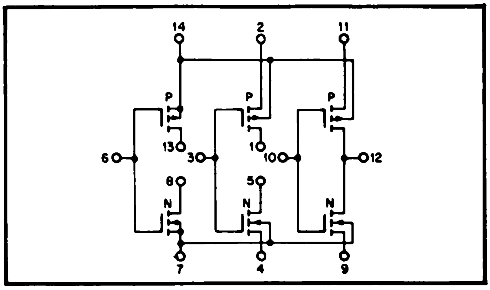
C 14-pin Cerdip
D 14-pin Ceramic
E 14-pin Epoxy
F 14-pin Flat
H Chip

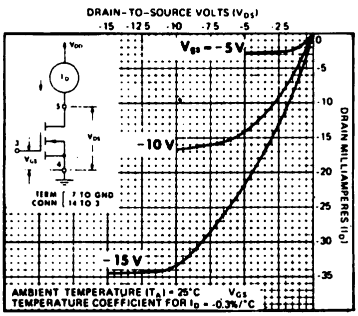
RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

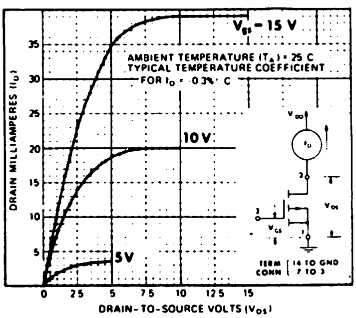
DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

SCHEMATIC DIAGRAM

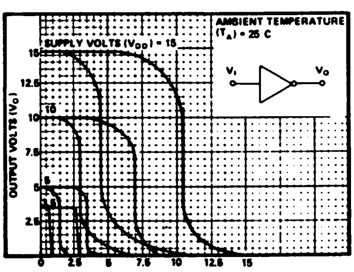




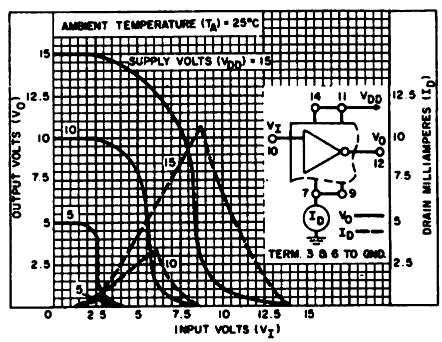
Typ. P-Channel drain characteristics



Typ. N-Channel drain characteristics



Min. and max. voltage transfer characteristics for inverter



Typ. current and voltage transfer characteristics for inverter

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS [1]

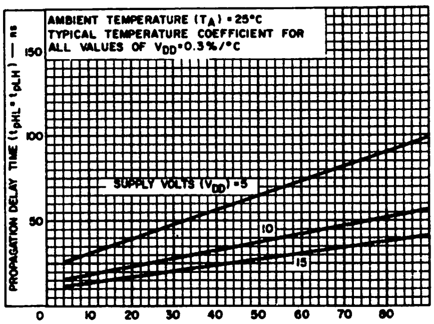
PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2] Min.	T_{LOW} [2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH} [2] Min.	T_{HIGH} [2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN}=V_{SS}$ or V_{DD}	–	0.05	–	0.0005	0.05	–	1.5	μAdc
		10	All valid input	–	0.10	–	0.001	0.10	–	3.0	
		15	combinations	–	0.20	–	0.002	0.20	–	6.0	

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

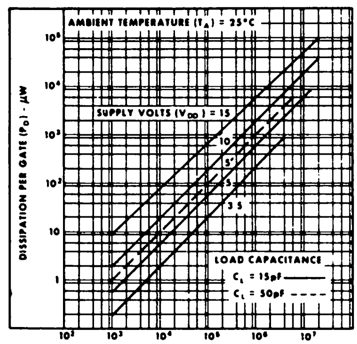
DYNAMIC CHARACTERISTICS (C_L = 50 pF, T_A = 25 C)[1]

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}	5	–	55	110	ns
		10	–	30	60	
		15	–	25	50	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	

[1] Connected as inverter



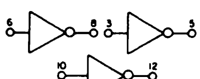
Typ. propagation delay time vs. C_L



Typ. dissipation characteristics

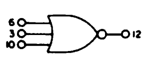
APPLICATIONS INFORMATION

Triple Inverters



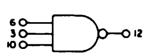
(14,2,11); (8,13);
(1,5); (7,4,9)

3-Input NOR Gate



(13,2); (1,11);
(12,5,8); (7,4,9)

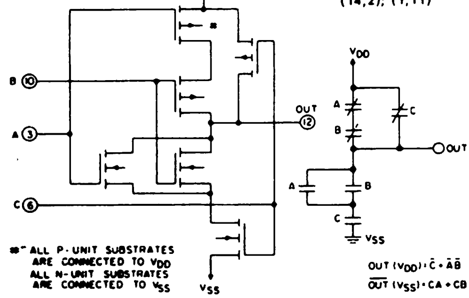
3-Input NAND Gate



(1,12,13); (2,14,11);
(4,8); (5,9)

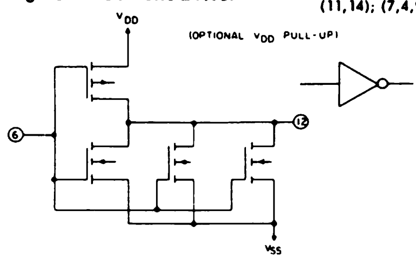
Tree (Relay) Logic

(13,12,5); (4,9,8);
(14,2); (1,11)



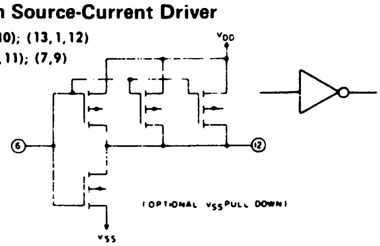
High Sink-Current Driver

(6,3,10); (8,5,12);
(11,14); (7,4,9)



High Source-Current Driver

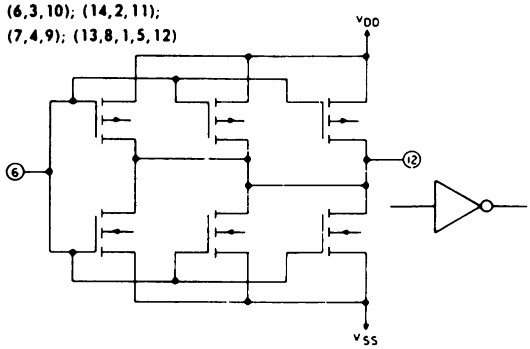
(6,3,10); (13,1,12)
(14,2,11); (7,9)



APPLICATIONS INFORMATION (Continued)

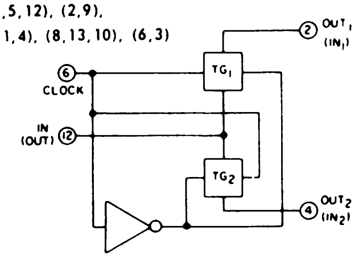
High Sink- and Source-Current Driver

(6,3,10); (14,2,11);
(7,4,9); (13,8,1,5,12)

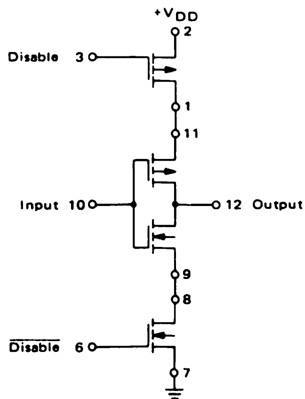


Dual Bi-Directional Transmission Gating

(1,5,12), (2,9),
(11,4), (8,13,10), (6,3)



3-State Buffer



INPUT	DISABLE	OUTPUT
1	0	0
0	0	1
X	1	Open

X = Don't Care

CMOS FOUR-BIT FULL ADDER

FEATURES

- Look-Ahead Carry Output
- High-Speed Operation

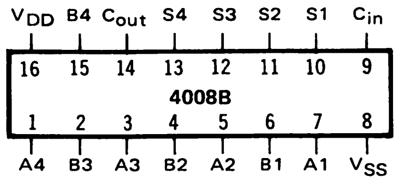
DESCRIPTION

The 4008B consists of four Full-Adder stages with fast Look-Ahead Carry provision from stage to stage. Circuitry is included to provide a fast Parallel-Carry-out bit to permit high-speed operation in arithmetic sections using several 4008B's. 4008B inputs include the four sets of bits to be added, A1 to A4 and B1 to B4, in addition to the Carry-in bit from a previous section. 4008B outputs include the four Sum bits, S1 and S4, in addition to the high-speed Parallel-Carry-out which may be utilized at a succeeding 4008B section.

TRUTH TABLE
(one stage)

C_{in}	B	A	C_{out}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

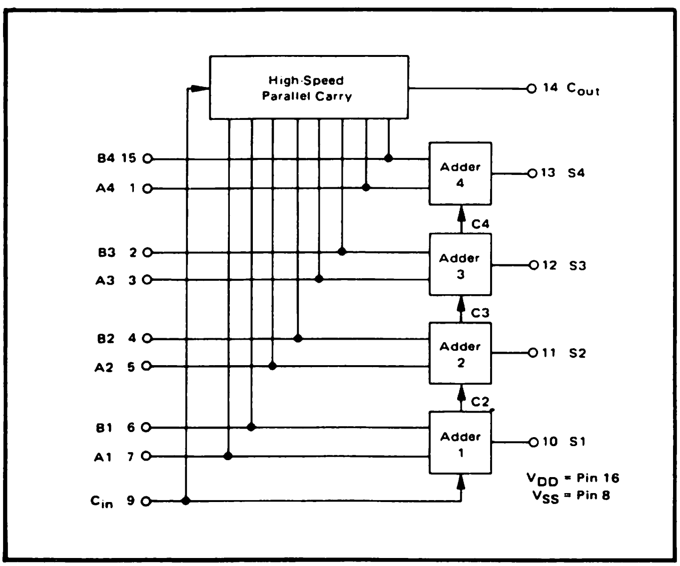
C 16-pin Cerdip
D 16-pin Ceramic
E 16-pin Epoxy
F 16-pin Flat
H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

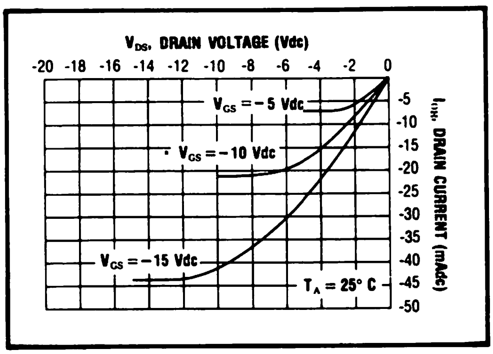
STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[2] Min.	T_{LOW}[2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH}[2] Min.	T_{HIGH}[2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN} = V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	μAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		15	combinations	–	20	–	0.2	20	–	600	

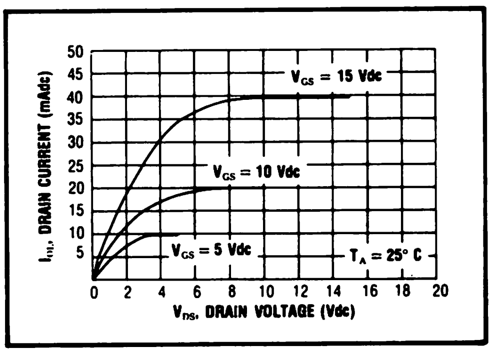
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME Sum In to Sum Out	t_{PLH}, t_{PHL}	5	–	400	800	ns
		10	–	160	320	
		15	–	115	230	
Sum In to Carry Out	t_{PLH}, t_{PHL}	5	–	310	620	ns
		10	–	140	280	
		15	–	110	220	
Carry In to Sum Out	t_{PLH}, t_{PHL}	5	–	380	760	ns
		10	–	150	300	
		15	–	115	230	
Carry In to Carry Out	t_{PLH}, t_{PHL}	5	–	180	360	ns
		10	–	75	150	
		15	–	55	110	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	

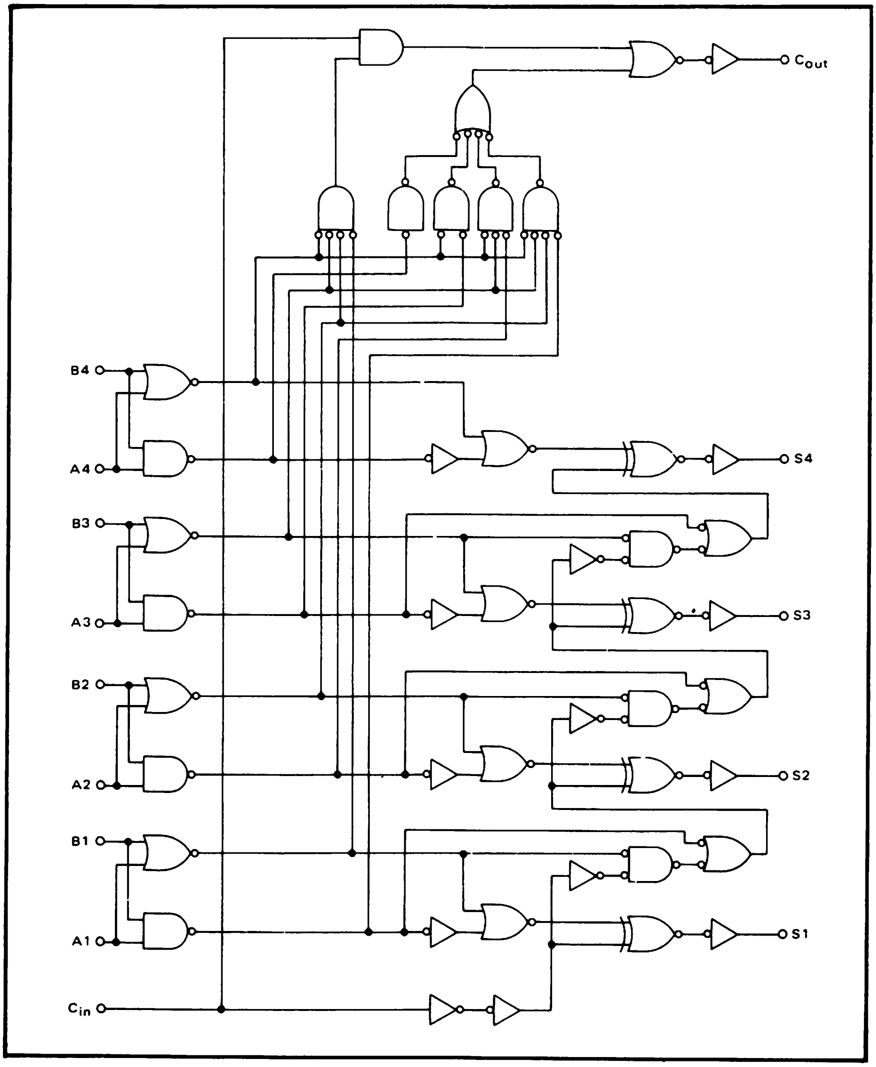


Typical P-Channel
Source Current Characteristics

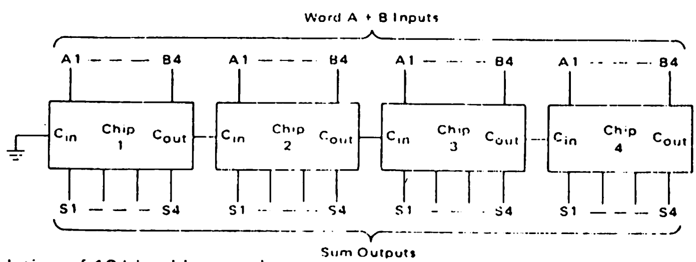


Typical N-Channel
Sink Current Characteristics

LOGIC DIAGRAM



APPLICATIONS INFORMATION

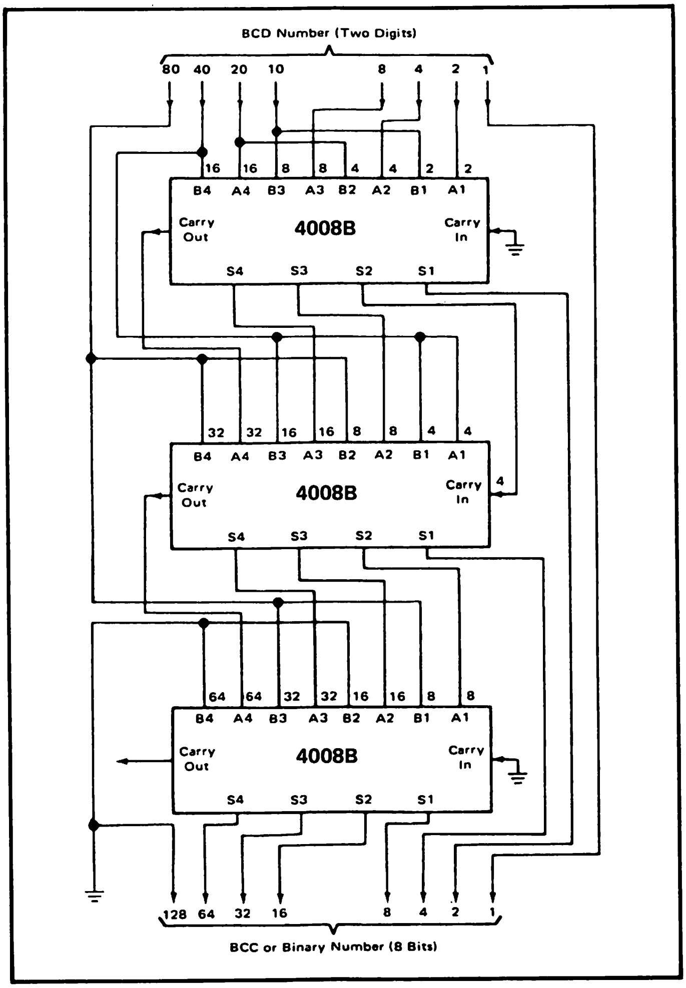


Calculation of 16-bit adder speed:

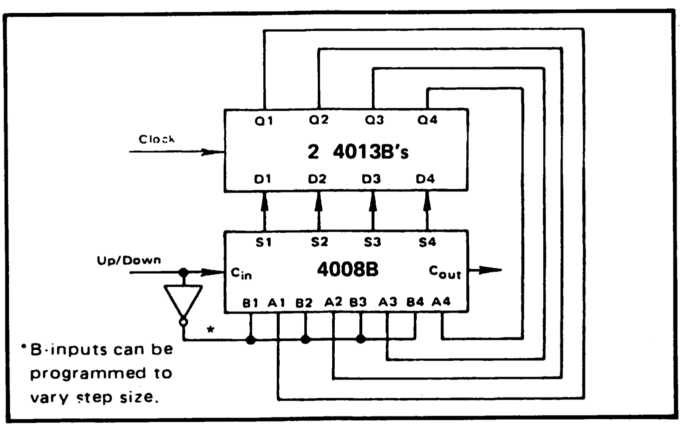
t_p total = t_p (Sum to Carry) + t_p (Carry to Sum) + 2 t_p (Carry to Carry)

16–Bit Adder

APPLICATIONS INFORMATION (Continued)



2-Digit BCD-to-Binary Conversion



4-Bit Up/Down Counter

CMOS HEX BUFFERS/CONVERTERS

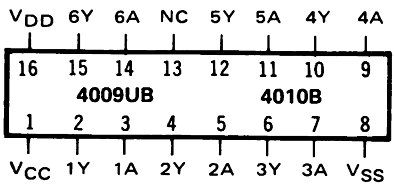
FEATURES

- Direct Drive of 2 TTL/DTL Loads
- Operation from Single or Dual Supplies
- All Inputs Diode-Protected

DESCRIPTION

The 4009UB and 4010B are single-chip monolithic silicon integrated circuits containing eighteen N-Channel and twelve P-Channel enhancement-mode MOS transistors connected to form six independent buffer/converter configurations. These devices are designed for use as hex CMOS-to-DTL or TTL logic level converters or hex CMOS current drivers. Conversion ranges are from CMOS logic operating at 3Vdc to 18Vdc supply levels to DTL or TTL logic operating at 3Vdc to 6Vdc supply levels. Conversion to logic output levels greater than 6Vdc is permitted proving $V_{CC} \leq V_{DD}$.

CONNECTION DIAGRAM
(all packages)

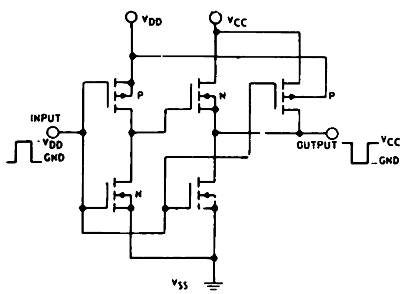


Add Suffix for Package:

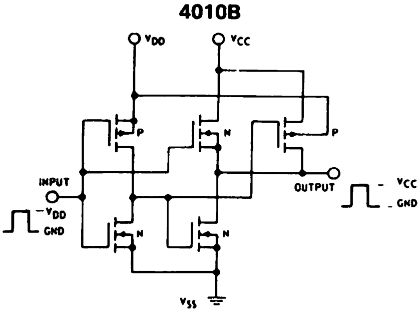
C 16-pin Cerdip
D 16-pin Ceramic
E 16-pin Epoxy
F 16-pin Flat
H Chip

SCHEMATIC DIAGRAMS

4009UB



4010B



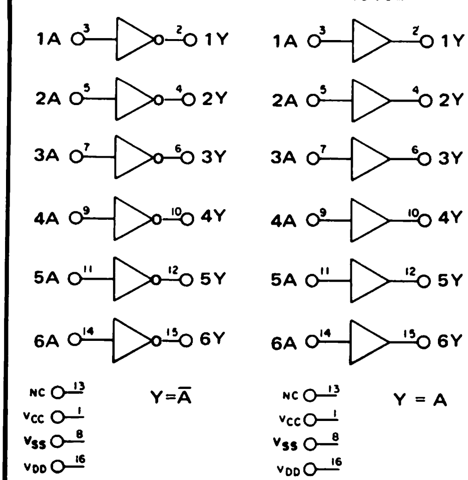
RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
	$V_{CC} - V_{SS}$	3 to 15	Vdc
	V_{CC}	$\leq V_{DD}$	
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

LOGIC DIAGRAMS

4009UB 4010B



ELECTRICAL CHARACTERISTICS

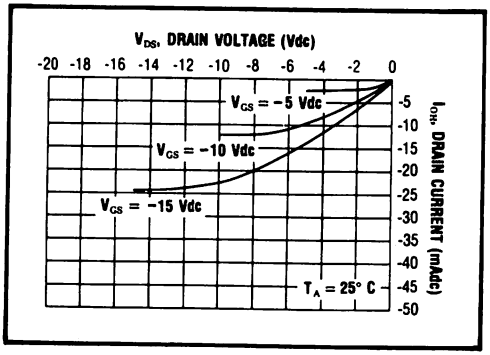
STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[2] Min.	T_{LOW}[2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH}[2] Min.	T_{HIGH}[2] Max.	Units
QUIESCENT DEVICE CURRENT 4009UB	I_{DD}	5 10 15	$V_{IN} = V_{SS}$ or V_{DD} All valid input combinations	– – –	0.25 0.50 1.00	– – –	0.005 0.01 0.02	0.25 0.50 1.00	– – –	7.5 15.0 30.0	μAdc
QUIESCENT DEVICE CURRENT 4010B	I_{DD}	5 10 15	$V_{IN} = V_{SS}$ or V_{DD} All valid input combinations	– – –	1.0 2.0 4.0	– – –	0.005 0.01 0.02	1.0 2.0 4.0	– – –	30 60 120	μAdc
MINIMUM INPUT HIGH VOLTAGE 4009UB	V_{IH}	5 10 15	V_{OL} = 0.5V V_{OL} = 1.0V V_{OL} = 1.5V $I_O \leqslant 1\mu A$	– – –	4.0 8.0 12.0	– – –	2.75 5.5 8.25	4.0 8.0 12.0	– – –	4.0 8.0 12.0	Vdc
MAXIMUM INPUT LOW VOLTAGE 4009UB	V_{IL}	5 10 15	V_{OH} = 3.6V V_{OH} = 7.2V V_{OH} = 10.8V $I_O \leqslant 1\mu A$	1.0 2.0 2.5	– – –	1.0 2.0 2.5	2.25 4.5 6.75	– – –	1.0 2.0 2.5	– – –	Vdc
OUTPUT HIGH CURRENT (SOURCE)	I_{OH}	5 10 15	V_{OH} = 4.6 V_{OH} = 9.5 V_{OH} = 13.5	– 0.25 – 0.62 – 1.9	– – –	– 0.2 – 0.5 – 1.5	– – –	– – –	– 0.14 – 0.35 – 1.1	– – –	mAdc
OUTPUT LOW CURRENT (SINK)	I_{OL}	5 10 15	V_{OL} = 0.4V V_{OL} = 0.5V V_{OL} = 1.5V $V_{IN} = V_{SS}$ or V_{DD}	3.7 9.9 29.8	– – –	3.0 8.0 24	4.0 10 36	– – –	2.1 5.6 16.8	– – –	mAdc

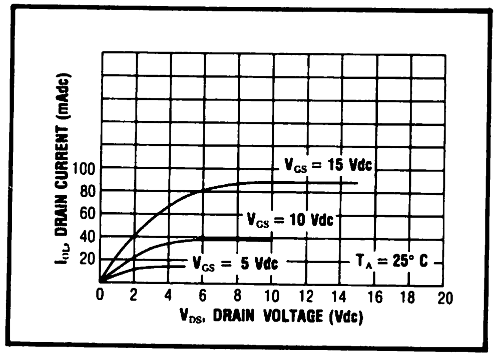
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device T_{HIGH} = +125°C for C, D, F, H device
= -40°C for E device. = + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

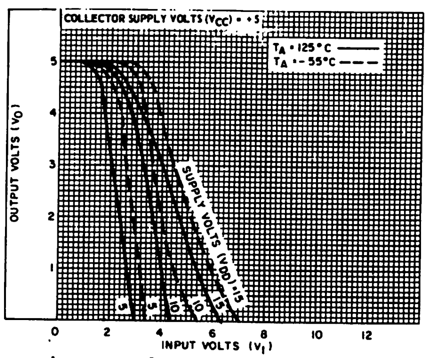
PARAMETER		V_{DD} (Vdc)	V_{CC} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME Driving CMOS	t_{PLH}	5 10 15	5 10 15	– – –	60 35 28	120 70 56	ns
Driving TTL/DTL		5 10 15	5 5 5	– – –	45 20 15	90 40 30	ns
Driving CMOS	t_{PHL}	5 10 15	5 10 15	– – –	30 18 12	60 36 24	ns
Driving TTL/DTL		5 10 15	5 5 5	– – –	35 15 10	70 30 20	ns
OUTPUT TRANSITION TIME	t_{TLH}	5 10 15	5 10 15	– – –	150 75 60	300 150 120	ns
	t_{THL}	5 10 15	5 10 15	– – –	30 20 12	60 40 24	ns
INPUT CAPACITANCE 4009UB 4010B	C_{IN}	– –	–	– –	10 5	15 7.5	pF



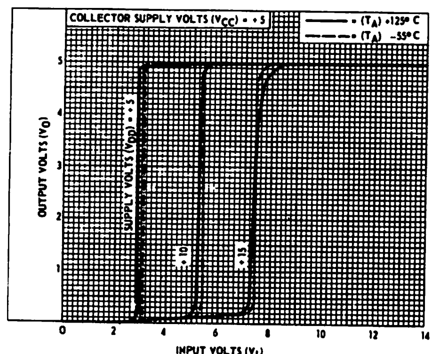
Typical P-Channel
Source Current Characteristics



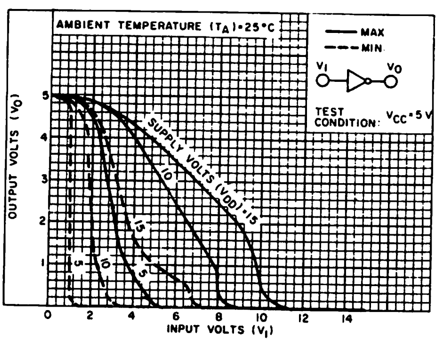
Typical N-Channel
Sink Current Characteristics



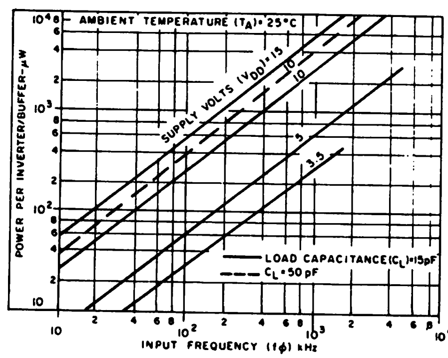
Typ. voltage transfer characteristics as function of temperature – 4009UB



Typ. voltage transfer characteristics as a function of temperature – 4010B



Min. & max. voltage transfer characteristics – 4009UB



Typ. dissipation characteristics – 4009UB, 4010B

CMOS NAND GATES

4011B – Quad 2-Input NAND
4012B – Dual 4-Input NAND
4023B – Triple 3-Input NAND
4068B – 8-Input NAND

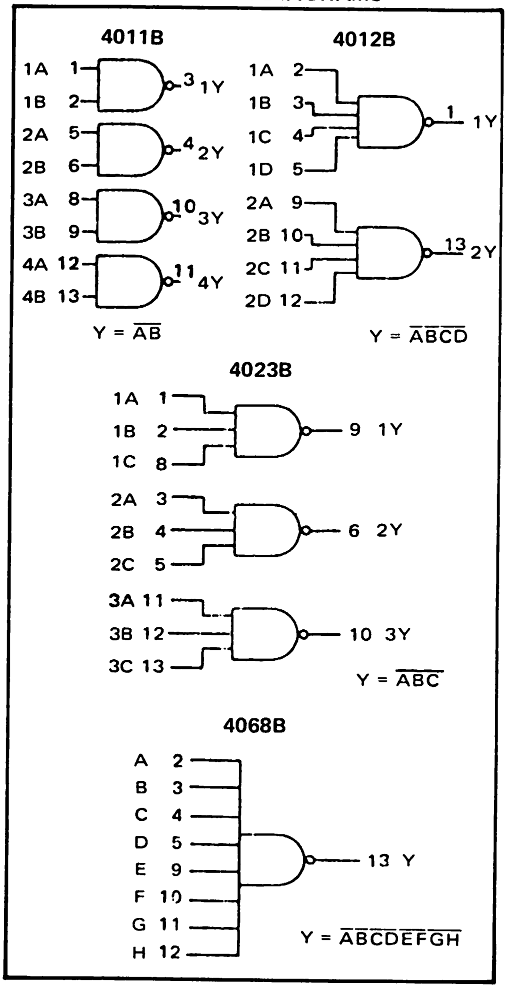
FEATURES

- Buffered Outputs
- Diode Protection on all Inputs
- Fully "B"-Series Compatible

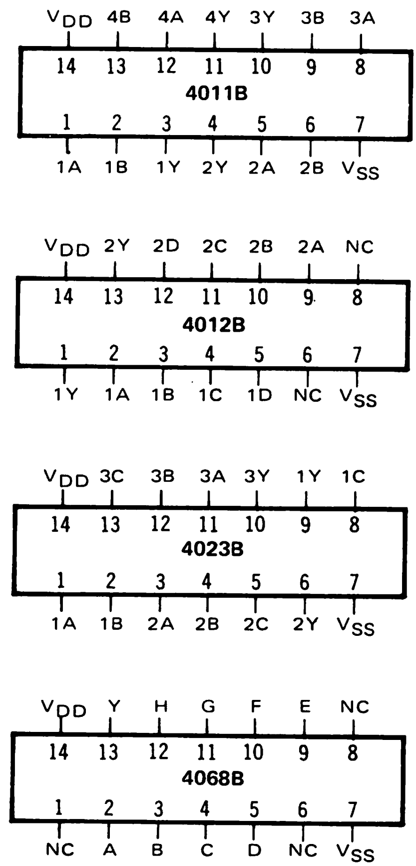
TRUTH TABLE

Inputs	Output
1 1 . . . 1	0
All other combinations	1

FUNCTION DIAGRAMS



CONNECTION DIAGRAMS
(all packages)



RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

ELECTRICAL CHARACTERISTICS

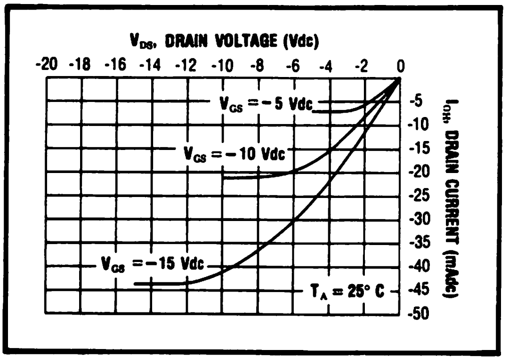
STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2] Min.	T_{LOW} [2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH} [2] Min.	T_{HIGH} [2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN} = V_{SS}$ or V_{DD}	–	0.05	–	0.0005	0.05	–	1.5	μAdc
		10	All valid input	–	0.10	–	0.001	0.10	–	3.0	
		15	combinations	–	0.20	–	0.002	0.20	–	6.0	

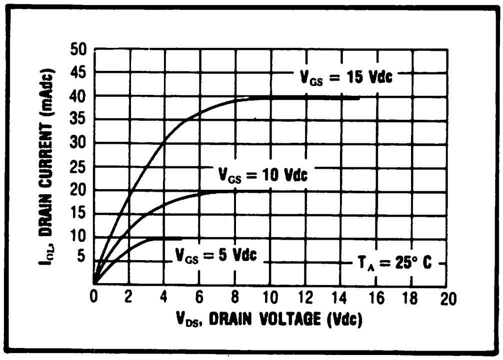
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications."
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}	5	–	125	250	ns
		10	–	60	120	
		15	–	45	90	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	

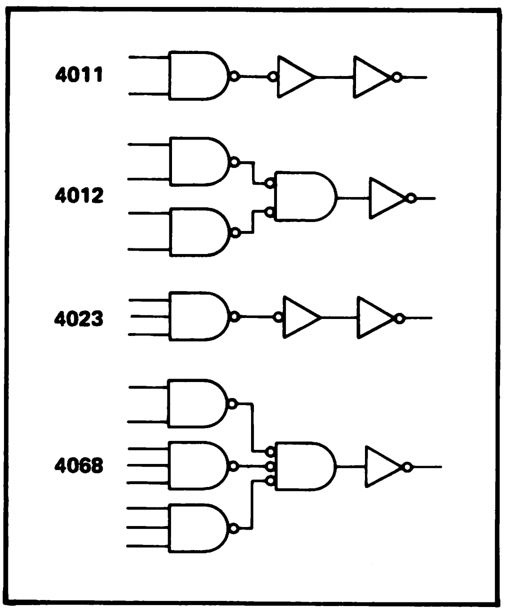


Typical P-Channel
Source Current Characteristics

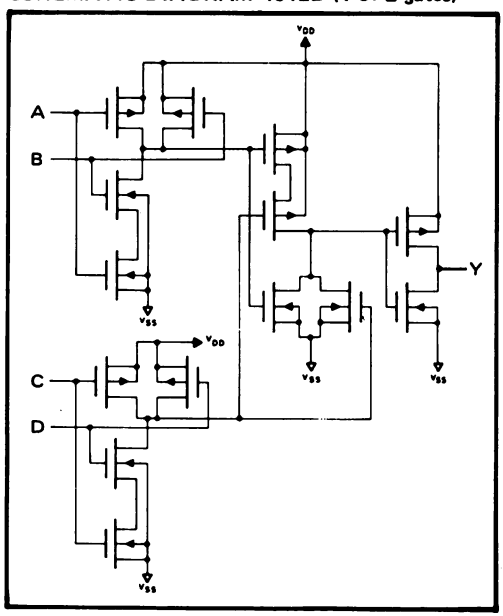


Typical N-Channel
Sink Current Characteristics

LOGIC DIAGRAMS



SCHEMATIC DIAGRAM 4012B (1 of 2 gates)



CMOS NAND GATE (Unbuffered)

FEATURES

- Unbuffered Outputs for Quasi-Linear Applications
- Quad 2-Input NAND Configuration
- Diode Protection on all Inputs
- Output Drive Current Compatible with "B" Series
- Pin Compatible with Buffered 4011B

DESCRIPTION

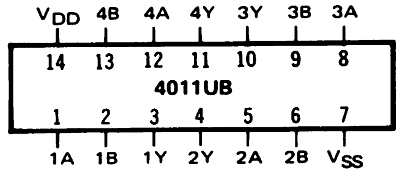
The 4011UB consists of four positive-logic NAND gates. The outputs are unbuffered, making the device suitable for quasi-linear applications, such as gated oscillators, multivibrators, and pulse shaping circuits.

For digital applications, the buffered 4011B is recommended for its higher gain and input pattern insensitivity.

TRUTH TABLE

Inputs	Output
1 1	0
All other combinations	1

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

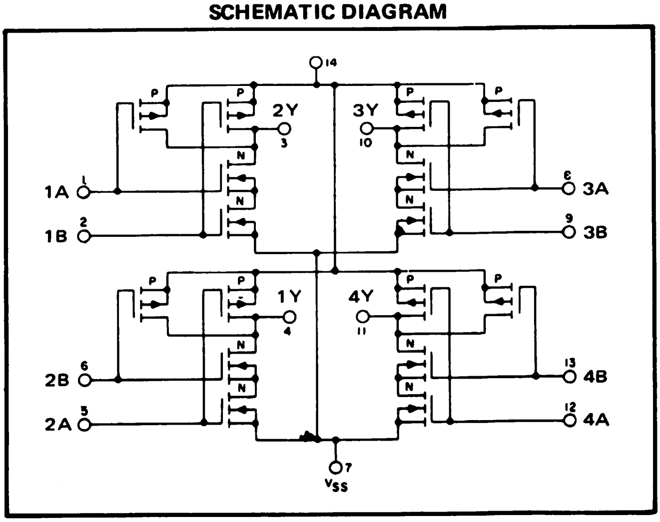
C 14-pin Cerdip
D 14-pin Ceramic
E 14-pin Epoxy
F 14-pin Flat
H Chip

RECOMMENDED OPERATING CONDITIONS

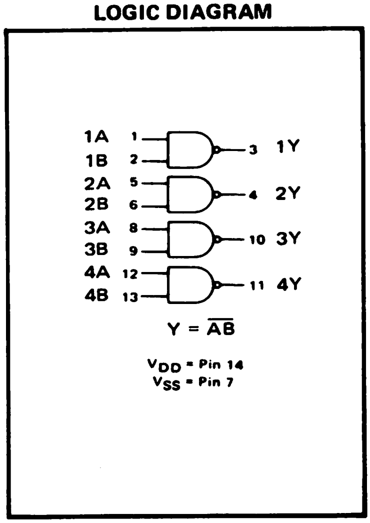
For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

SCHEMATIC DIAGRAM



LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

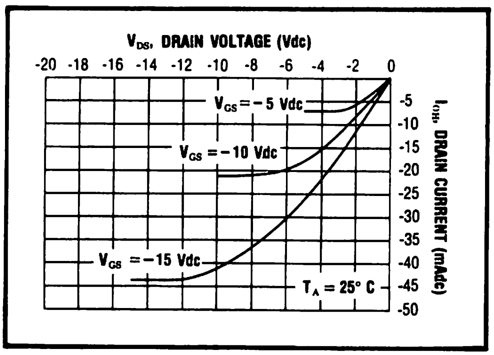
STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[2] Min.	T_{LOW}[2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH}[2] Min.	T_{HIGH}[2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5 10 15	V_{IN} = V_{SS} or V_{DD} All valid input combinations	– – –	0.05 0.10 0.20	– – –	0.0005 0.001 0.002	0.05 0.10 0.20	– – –	1.5 3.0 6.0	μAdc

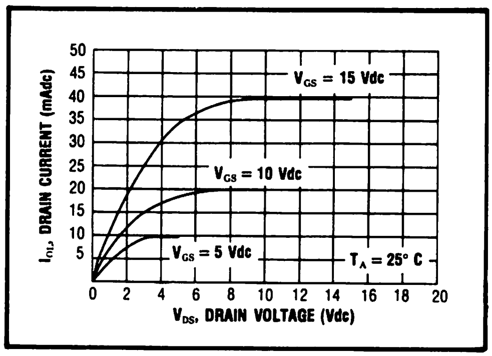
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}	5 10 15	– – –	60 30 25	120 60 50	ns
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5 10 15	– – –	100 50 40	200 100 80	ns

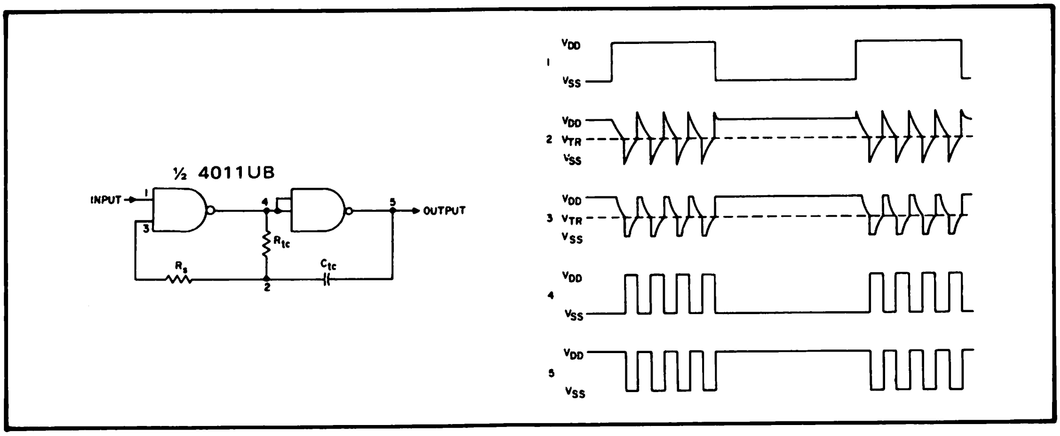


Typical P-Channel
Source Current Characteristics

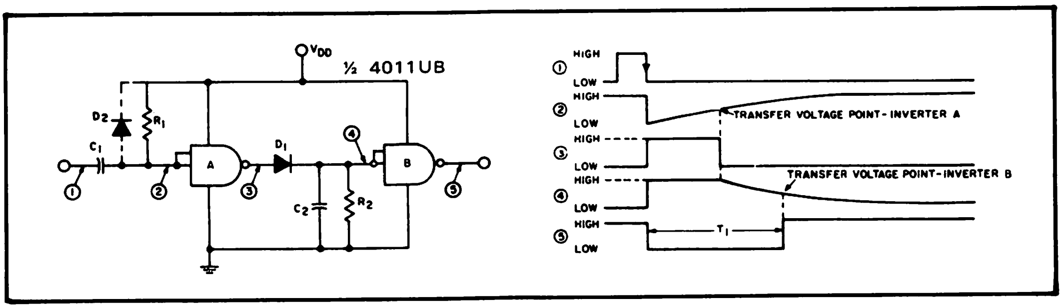


Typical N-Channel
Sink Current Characteristics

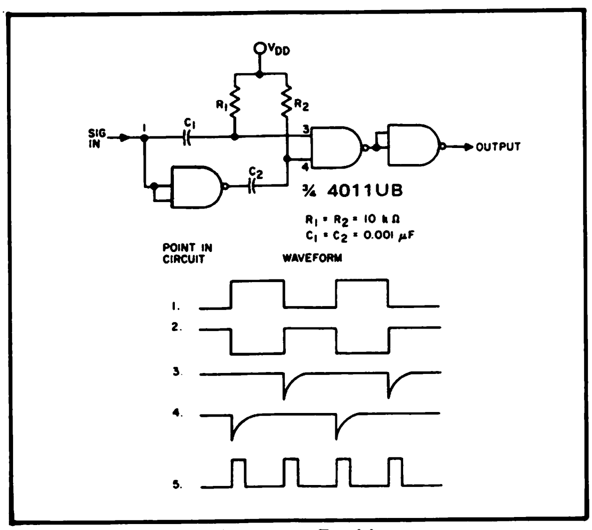
APPLICATIONS INFORMATION



Gated Oscillator



Compensated Monostable Multivibrator (Independent of Transfer Voltage)



Frequency Doubler

CMOS DUAL D-TYPE FLIP-FLOP

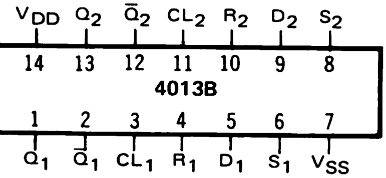
FEATURES

- Independent Set and Reset Controls
- Static Operation
- Logic Edge-Clocked Design
- 16MHz Toggle Rate @ 10Vdc

DESCRIPTION

The 4013B consists of two identical, independent D-type Flip-Flops. These devices can be used for shift register applications, and, by connecting the $\overline{Q}$ output to the Data input, for counter and toggle applications. The logic level present at the D input is transferred to the Q output during the positive-going transition of the Clock pulse. Setting or resetting is independent of the Clock and is accomplished by a high level on the Set or Reset line, respectively.

CONNECTION DIAGRAM
(all packages)



RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

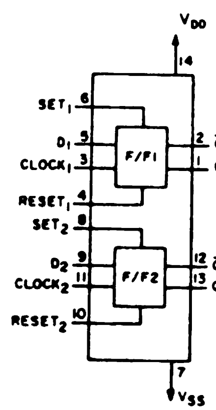
DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

TRUTH TABLE

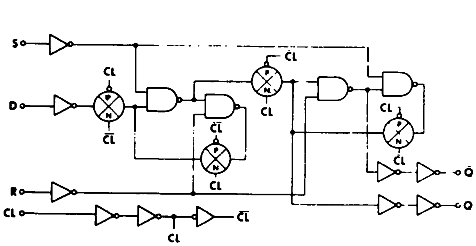
CL ▲	D	R	S	Q	$\overline{Q}$	
_/‾	0	0	0	0	1	
_/‾	1	0	0	1	0	
‾_	x	0	0	Q	$\overline{Q}$	NO CHANGE
x	x	1	0	0	1	
x	x	0	1	1	0	
x	x	1	1	1	1	

▲ = Level Change
x = Don't Care

BLOCK DIAGRAM



LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS [1]

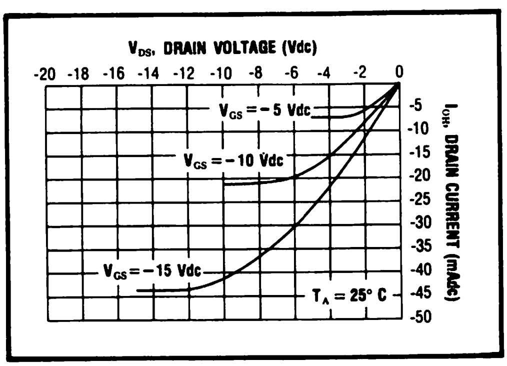
PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2]		+25°C			T_{HIGH} [2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN}=V_{SS}$ or V_{DD}	–	1.0	–	0.005	1.0	–	30	μAdc
		10	All valid input	–	2.0	–	0.01	2.0	–	60	
		15	combinations	–	4.0	–	0.02	4.0	–	120	

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications."
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

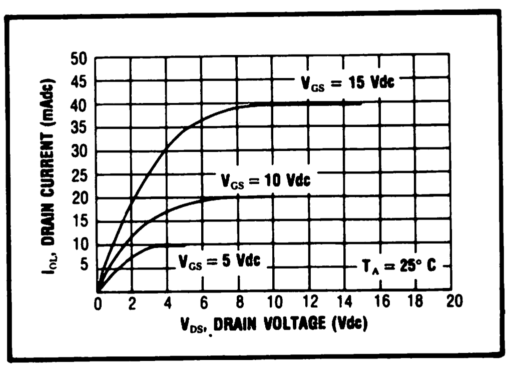
DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}	5	–	125	250	ns
		10	–	65	130	
		15	–	45	90	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
MINIMUM CLOCK PULSE WIDTH	PW_{CL}	5	–	70	140	ns
		10	–	30	60	
		15	–	20	40	
MAXIMUM CLOCK FREQUENCY	f_{CL}	5	4.0	7.0	–	MHz
		10	8.0	16	–	
		15	12.5	25	–	
MAXIMUM CLOCK RISE AND FALL TIME [1]	t_{rCL}, t_{fCL}	5	15	–	–	μs
		10	10	–	–	
		15	5	–	–	
MINIMUM SETUP TIME	t_{setup}	5	–	25	50	ns
		10	–	10	20	
		15	–	7.5	15	
MINIMUM HOLD TIME	t_{hold}	5	–	-25	0	ns
		10	–	-10	0	
		15	–	-5	0	
SET AND RESET OPERATIONS						
PROPAGATION DELAY TIME S to Q, R to $\bar{Q}$	t_{PLH}	5	–	125	250	ns
		10	–	65	130	
		15	–	45	90	
MINIMUM SET AND RESET PULSE WIDTH	PW_S, PW_R	5	–	65	130	ns
		10	–	30	60	
		15	–	25	50	
SET AND RESET REMOVAL TIME	t_{rem}	5	–	0	25	ns
		10	–	0	10	
		15	–	0	5	

[1] When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.



Typical P-Channel Source Current Characteristics



Typical N-Channel Sink Current Characteristics

CMOS 8-STAGE SHIFT REGISTER

FEATURES

- Synchronous Parallel Input/Serial Output
- Synchronous Serial Input/Serial Output
- Fully Static Operation – DC to 6 MHz @ 10Vdc
- Q Outputs from Stages 6, 7, and 8 Available

DESCRIPTION

The 4014B is an 8-stage Parallel-Input/Serial Output Register having common Clock and Parallel/Serial Control inputs, a single Serial Data input, and individual parallel Jam inputs to each register stage. Each register stage is a D-type, master-slave flip-flop. In addition to an output from stage 8, Q outputs are also available from stages 6 and 7. Parallel as well as serial entry is made into the register synchronous with the positive Clock line transition and under control of the Parallel/Serial Control input. When the Parallel/Serial Control input is low, data is serially shifted into the 8-stage register synchronously with the transition of the Clock line. When the Parallel/Serial Control input is high, data is jammed into the 8-stage register via the Parallel Input lines and synchronous with the positive transition of the Clock line. Changes on the Parallel/Serial Control should be made only while the Clock is low. Register expansion using multiple 4014B packages is permitted.

TRUTH TABLE

Serial Operation

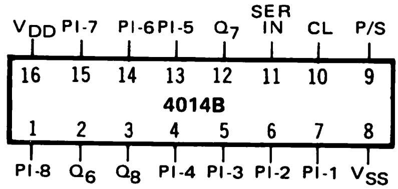
t	CLOCK	SER IN	P/S	Q6 t=n+6	Q7 t-n+7	Q8 t=n+8
n		0	0	0	?	?
n+1		1	0	1	0	?
n+2		0	0	0	1	0
n+3		1	0	1	0	1
		X	0	Q6	Q7	Q8

Parallel Operation

CLOCK	SER IN	P/S	PI-m	*Q_m
	X	1	0	0
	X	1	1	1

*Q6, Q7, and Q8 are available externally
X = Don't Care

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

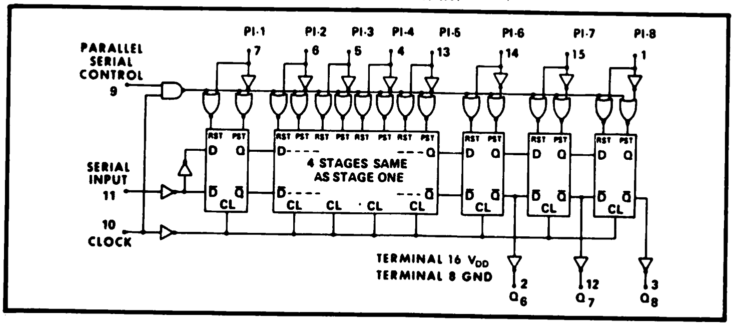
C	16-pin Cerdip
D	16-pin Ceramic
E	16-pin Epoxy
F	16-pin Flat
H	Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS [1]

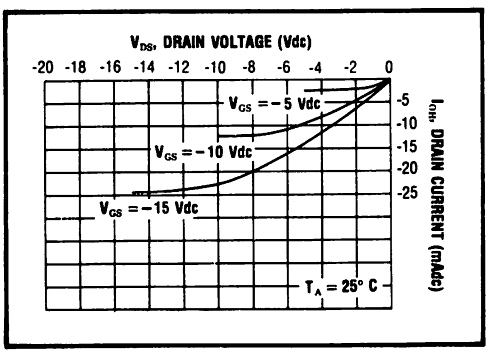
PARAMETER		VDD (Vdc)	CONDITIONS	TLOW [2]		+25°C			THIGH [2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN}=V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	μAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		15	combinations	–	20	–	0.2	20	–	600	

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

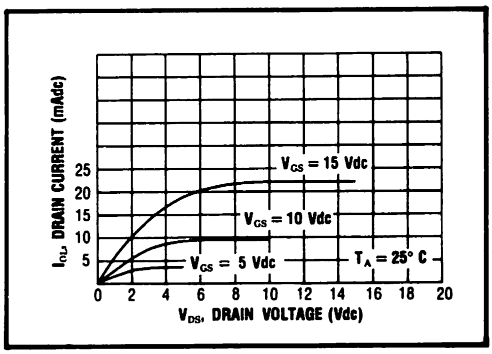
DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A =25°C)

PARAMETER		VDD (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}	5	–	160	320	ns
		10	–	80	160	
		15	–	60	120	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
MINIMUM CLOCK PULSE WIDTH	PW_{CL}	5	–	90	180	ns
		10	–	40	80	
		15	–	25	50	
MAXIMUM CLOCK FREQUENCY	f_{CL}	5	3.0	5	–	MHz
		10	6.0	10	–	
		15	8.5	14	–	
MAXIMUM CLOCK RISE AND FALL TIME[1]	t_{rCL}, t_{fCL}	5	15	–	–	μs
		10	15	–	–	
		15	5	–	–	
MINIMUM SETUP TIME Serial Input	t_{setup}	5	–	60	120	ns
		10	–	40	80	
		15	–	30	60	
P/S Input	t_{setup}	5	–	90	180	ns
		10	–	40	80	
		15	–	30	60	
Parallel Inputs	t_{setup}	5	–	90	180	ns
		10	–	40	80	
		15	–	30	60	
MINIMUM HOLD TIME All Inputs	t_{hold}	5	–	40	80	ns
		10	–	20	40	
		15	–	10	20	

[1] When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.



Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

CMOS DUAL 4-STAGE SHIFT REGISTER

FEATURES

- **Serial Input/Parallel Output**
- **Direct Reset**
- **Two Independent Sections**
- **Fully Static Operation - DC to 5MHz @ 10Vdc**

DESCRIPTION

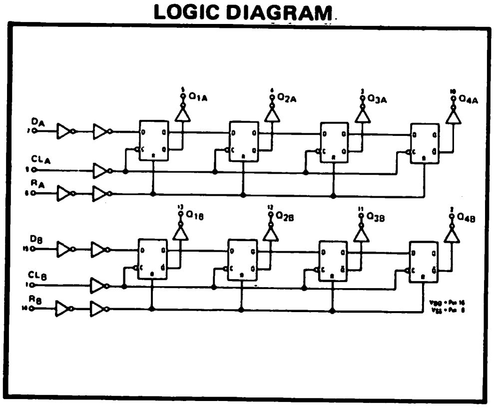
The 4015B consists of two identical, independent, 4-stage Serial-Input/Parallel-Output Registers. Each register has independent Clock and Reset inputs as well as a single serial Data input. Q outputs are available from each of the four stages on both registers. All register stages are D-type, master-slave flip-flops. The logic level present at the Data input is transferred into the first register stage and shifted right one stage at each positive-going Clock transition. Resetting of all stages is accomplished by a high level on the Reset line. Register expansion to 8 stages using one 4015B package, or to more than 8 stages using additional 4015B's, is possible.

TRUTH TABLE

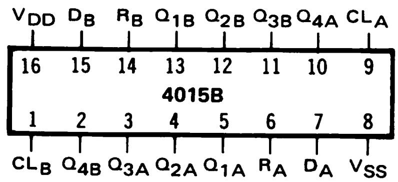
CL*	D	R	Q_1	Q_n	
_/‾	0	0	0	Q_{n-1}	
_/‾	1	0	1	Q_{n-1}	
‾_	X	0	Q_1	Q_n	(NO CHANGE)
X	X	1	0	0	

* = LEVEL CHANGE
X= DON'T CARE

LOGIC DIAGRAM



CONNECTION DIAGRAM
(all packages)



Add suffix for package:

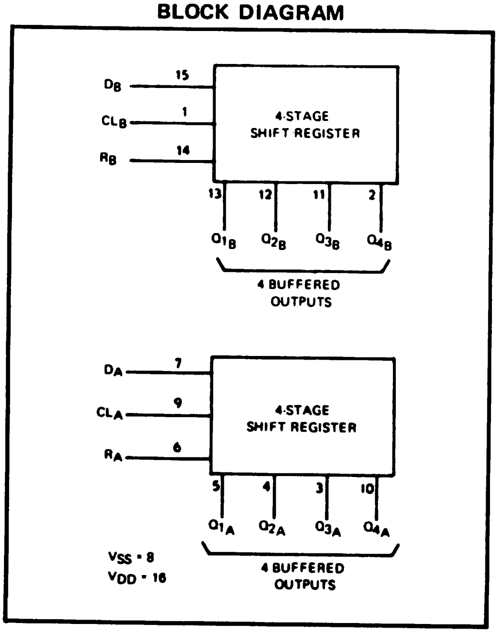
C	16-pin Cerdip
D	16-pin Ceramic
E	16-pin Epoxy
F	16-pin Flat
H	Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	V_{DD} - V_{SS}	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS[1]

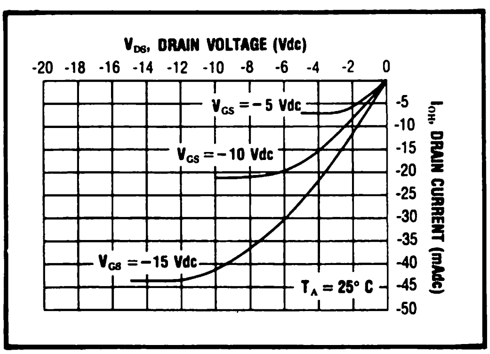
PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[2] Min.	T_{LOW}[2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH}[2] Min.	T_{HIGH}[2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN} = V_{SS}$ or V_{DD}	–	5	–	0.05	5		150	μAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		15	combinations	–	15	–	0.2	20	–	600	

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

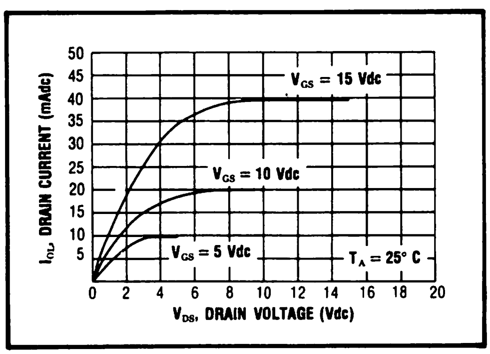
DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}	5	–	250	500	ns
		10	–	100	200	
		15	–	90	180	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
MINIMUM CLOCK PULSE WIDTH	PW_{CL}	5	–	200	400	ns
		10	–	100	200	
		15	–	80	160	
MAXIMUM CLOCK FREQUENCY	f_{CL}	5	1.25	2.5	–	MHz
		10	2.5	5.0	–	
		15	3.0	6.0	–	
MAXIMUM CLOCK RISE AND FALL TIME[1]	t_{rCL}, t_{fCL}	5	15	–	–	μs
		10	15	–	–	
		15	5	–	–	
MINIMUM DATA INPUT DATA SETUP TIME	t_{setup}	5	–	150	300	ns
		10	–	50	100	
		15	–	40	80	
MINIMUM DATA INPUT HOLD TIME	t_{hold}	5	–	0	50	ns
		10	–	0	25	
		15	–	0	15	
RESET OPERATION						
PROPAGATION DELAY TIME	t_{PHL}	5	–	200	400	ns
		10	–	100	200	
		15	–	90	180	
MINIMUM RESET PULSE WIDTH	PW_R	5	–	200	400	ns
		10	–	80	160	
		15	–	60	120	
RESET REMOVAL TIME	t_{rem}	5	–	375	750	ns
		10	–	125	250	
		15	–	100	200	

[1] When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.



Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

CMOS QUAD ANALOG SWITCH

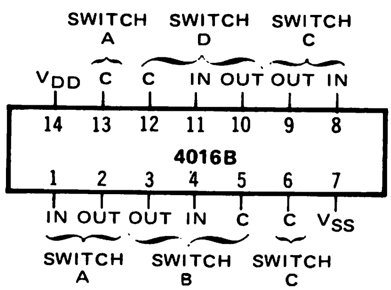
FEATURES

- Wide Range of Digital and Analog Signal Levels-Digital or Analog Signals to 18 Volts peak
- Low ON Resistance – 200 Ω typ. over 15Vp-p Signal Input Range, @ 15Vdc
- Matched Switch Characteristics - 10Ω typ. Difference between R_{ON} Values at a Fixed Bias Point over 15Vp-p Signal Input Range @ 15Vdc
- High On/Off Output Voltage Ratio – 65 dB typ. @ f_{is} = 10kHz, R_L = 10KΩ
- High degree of Linearity - ≤ 0.4% Distortion typ. @ f_{is} = 1kHz, V_{is} = 5$V_{p\text{-}p}$, V_{DD}-V_{SS}≥10V, R_L = 10kΩ
- Extremely Low OFF Switch Leakage Resulting in Very Low Offset Current and High Effective OFF resistance - 10pA typ. @ V_{DD}-V_{SS} = 10V, T_A = 25°C
- Extremely High Control Input Impedance (Control Circuit Isolated from Signal Circuit) 10^{12}Ω typ.
- Low Crosstalk between Switches - -50dB typ. @ f_{is} = 0.9MHz, R_L = 1kΩ
- Matched Control-Input to Signal-Output Capacitances - Reduces Output Signal Transients
- Transmits Frequencies up to 40MHz

DESCRIPTION

The 4016B is a single-chip monolithic silicon integrated circuit containing eight N-channel and eight P-channel enhancement-mode MOS transistors connected to form four independent bilateral signal switches. Each switch consists of both P- and N-channel devices with common source and drain connections. A single control signal is required per switch. Both P and N devices in a given switch are biased ON or OFF by the control signal. The CMOS switch permits peak input-signal voltage swings equal to the full supply voltage, a considerable advantage over single-channel types.

CONNECTION DIAGRAM
(all packages)

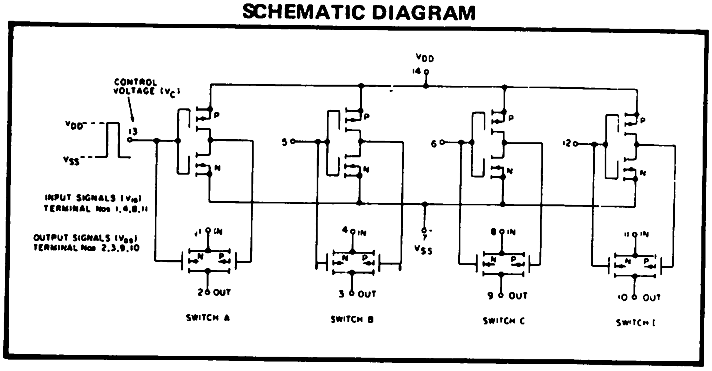


RECOMMENDED OPERATING CONDITIONS

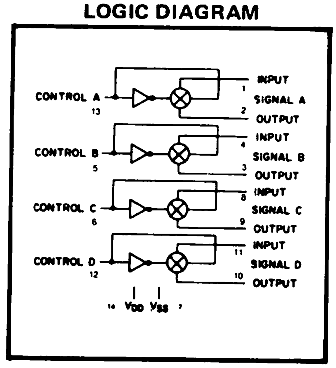
For maximum reliability:

DC Supply Voltage	V_{DD} - V_{SS}	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

SCHEMATIC DIAGRAM



LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS[1]

PARAMETER		CONDITIONS	V_{SS} (Vdc)	V_{DD} (Vdc)	T_{LOW}[2] Min.	T_{LOW}[2] Max.	25°C Min.	25°C Typ.	25°C Max.	T_{HIGH}[2] Min.	T_{HIGH}[2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	$V_{IN} = V_{SS}$ or V_{DD} All valid input combinations	0 0 0	5 10 15	– – –	0.05 0.1 0.2	– – –	0.0005 0.001 0.002	0.05 0.1 0.2	– – –	1.5 3.0 6.0	μAdc
MINIMUM INPUT HIGH VOLTAGE (Control Input)	V_{IH}		0 0 0	5 10 15	– – –	3.5 7.0 11.0	– – –	1.5 1.5 1.5	3.5 7.0 11.0	– – –	3.5 7.0 11.0	Vdc
MAXIMUM INPUT LOW VOLTAGE (Control Input)	V_{IL}	$V_{IS} = V_{SS}$ $V_{OS} = V_{DD}$ $I_{OS} = 10\mu A$	0 0 0	5 10 15	0.9 0.9 0.9	– – –	0.7 0.7 0.7	1.5 1.5 1.5	– – –	0.4 0.4 0.4	– – –	Vdc
SWITCH INPUT/OUTPUT LEAKAGE (Switch off)	I_{OFF}	$V_C = V_{SS}$ $V_{IS} = V_{DD}$	0	15	–	±0.1	–	$\pm 10^{-5}$	±0.1	–	±1.0	μAdc
ON-RESISTANCE	R_{ON}	$V_{IS} = \frac{V_{DD} - V_{SS}}{2}$ $V_C = V_{DD}$ $R_L = 10k\Omega$	0 0	15 10	– –	360 600	– –	200 250	400 660	– –	520 840	Ω
ON-RESISTANCE MATCH (Same package)	ΔR_{ON}	$V_C = V_{DD}$ $R_L = 10k\Omega$ V_{IS} (Vdc): ±7.5, ±5	-7.5 -5	+7.5 +5	– –	– –	– –	10 15	– –	– –	– –	Ω

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications."
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.
[3] Conditions for measuring V_{IH}:

V_{DD}	V_{OS}	V_{IS}	I_{OS} T_{LOW}	I_{OS} 25°C	I_{OS} T_{HIGH}	UNITS
5	5	4.6	–.25	–.20	–.14	
10	10	9.5	–.62	–.50	–.35	mA
15	15	13.5	–1.8	–1.50	–1.10	

DYNAMIC CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

PARAMETER		CONDITIONS		V_{SS} (Vdc)	V_{DD} (Vdc)	Min.	Typ.	Max.	UNIT
SIGNAL INPUTS (V_{IS}) AND OUTPUTS (V_{OS})									
PROPAGATION DELAY TIME Signal input to signal output	t_{PLH}, t_{PHL}	$V_C = V_{DD}$ V_{IS} = square wave $R_L = 10k\Omega$		0 0 0	5 10 15	– – –	20 10 7.5	40 20 15	ns
BANDWIDTH (-3dB) (Sine Wave)	BW	$V_C = V_{DD}$ $V_{IS} = 5V_{p\text{-}p}$ centered @0.0Vdc	R_L: 1kΩ 10kΩ 100kΩ 1MΩ	-5	+5	– – – –	54 40 38 37	– – – –	MHz

ELECTRICAL CHARACTERISTICS (Continued)

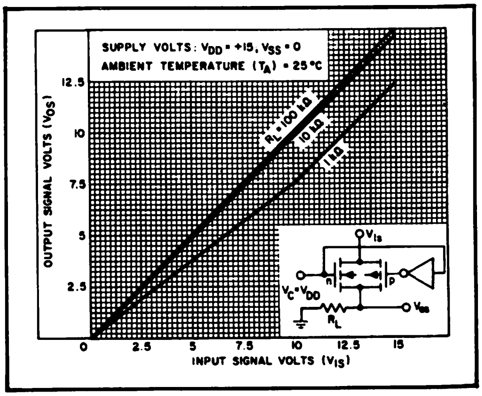
DYNAMIC CHARACTERISTICS (C_L = 50 pF, T_A = 25°C) (Continued)

PARAMETER		CONDITIONS		V_{SS} (Vdc)	V_{DD} (Vdc)	Min.	Typ.	Max.	Units
SIGNAL INPUTS (V_{IS}) AND OUTPUTS (V_{OS}) (Continued)									
INSERTION LOSS (= 20 log$_{10}\frac{V_{OS}}{V_{IS}}$)		V_C = V_{DD} V_{IS} = 5$V_{p\text{-}p}$ centered @0.0Vdc	R_L 1kΩ 10kΩ 100kΩ 1MΩ	-5	+5	– – – –	2.3 0.2 0.1 0.05	– – – –	dB
SIGNAL DISTORTION (Sine Wave)		V_C = V_{DD} V_{IS} = 5$V_{p\text{-}p}$ centered @0.0Vdc f_{IS} = 1.0kHz R_L = 10kΩ		-5	+5	–	0.4	–	%
FEEDTHROUGH (-50dB)		V_C = V_{SS} V_{IS} = 5$V_{p\text{-}p}$ centered @0.0Vdc	R_L 1kΩ 10kΩ 100kΩ 1MΩ	5	+5	– – – –	1250 140 18 2	– – – –	kHz
CROSSTALK (-50dB) (Between two switches)		V_C (A) = V_{DD} V_C (B) = V_{SS} V_{IS}(A) = 5$V_{p\text{-}p}$ centered @0.0Vdc R_L = 1.0k		-5	+5	–	0.9	–	MHz
CAPACITANCE Input Output Feedthrough	 C_{IS} C_{OS} C_{IOS}	V_C = V_{SS}		-5	+5	 – – –	 4 4 0.2	 – – –	 pF pF pF
CONTROL INPUT (V_C)									
PROPAGATION DELAY TIME Turn on	t_{PLH}, t_{PHL}	$V_{SS} \leqslant V_{IS} \leqslant V_{DD}$ R_L = 10kΩ		0 0 0	5 10 15	– – –	40 20 15	80 40 30	ns
MAXIMUM INPUT FREQUENCY	f_C	$V_{SS} \leqslant V_{IS} \leqslant V_{DD}$ R_L = 1.0kΩ		0 0 0	5 10 15	– – –	5 10 12	– – –	MHz
CROSSTALK (To signal port)		V_C = Square wave R_L = 10kΩ R_{IN} = 1.0kΩ		0 0 0	5 10 15	– – –	30 50 100	– –	mV

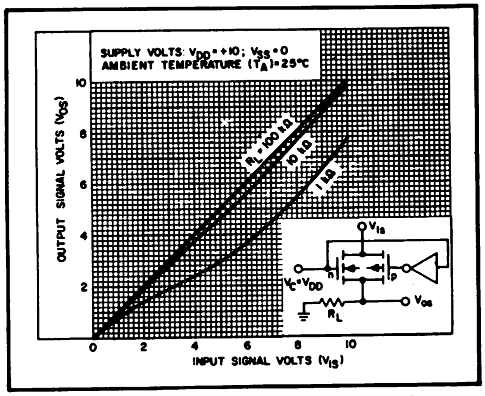
TYPICAL ON-RESISTANCE CHARACTERISTICS

CHARAC-TERISTIC*	SUPPLY CONDITIONS		LOAD CONDITIONS					
			R_L = 1kΩ		R_L = 10kΩ		R_L = 100kΩ	
	V_{DD} (V)	V_{SS} (V)	VALUE (Ω)	V_{is} (V)	VALUE (Ω)	V_{is} (V)	VALUE (Ω)	V_{is} (V)
R_{ON}	+15	0	200	+15	200	+15	180	+15
			200	0	200	0	200	0
R_{ON}(max.)	+15	0	300	+11	300	+9.3	320	+9.2
R_{ON}	+10	0	290	+10	250	+10	240	+10
			290	0	250	0	300	0
R_{ON}(max.)	+10	0	500	+7.4	560	+5.6	610	+5.5
R_{ON}	+ 5	0	860	+ 5	470	+ 5	450	+ 5
			600	0	580	0	800	0
R_{ON}(max.)	+ 5	0	1.7k	+4.2	7k	+2.9	33k	+2.7
R_{ON}	+7.5	−7.5	200	+7.5	200	+7.5	180	+7.5
			200	−7.5	200	−7.5	180	−7.5
R_{ON}(max.)	+7.5	−7.5	290	±0.25	280	±25	400	±0.25
R_{ON}	+ 5	− 5	260	+ 5	250	+ 5	240	+ 5
			310	− 5	250	− 5	240	− 5
R_{ON}(max.)	+ 5	− 5	600	±0.25	580	±0.25	760	±0.25
R_{ON}	+2.5	−2.5	590	+2.5	450	+2.5	490	+2.5
			720	-2.5	520	-2.5	520	−2.5
R_{ON}(max.)	+2.5	−2.5	232k	±0.25	300k	±0.25	870k	±0.25

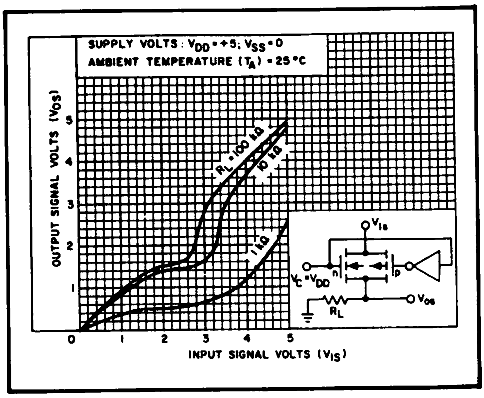
* Variation from a perfect switch; R_{ON} = 0Ω.



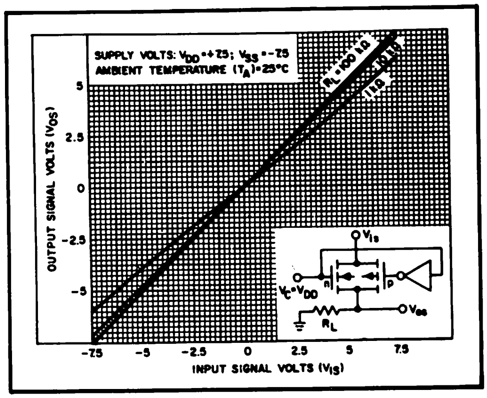
Typ. ON characteristics for 1 of 4 switches with V_{DD}=+15V, V_{SS}=0V



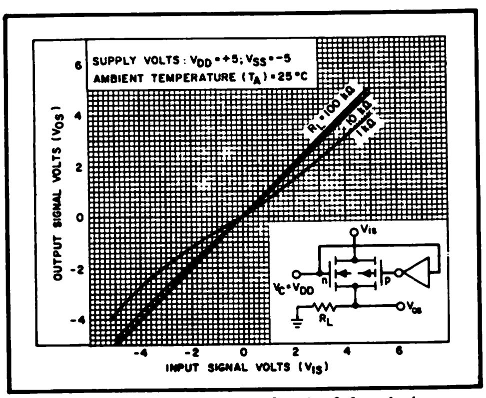
Typ. ON characteristics for 1 of 4 switches with V_{DD}=+10V, V_{SS}=0V



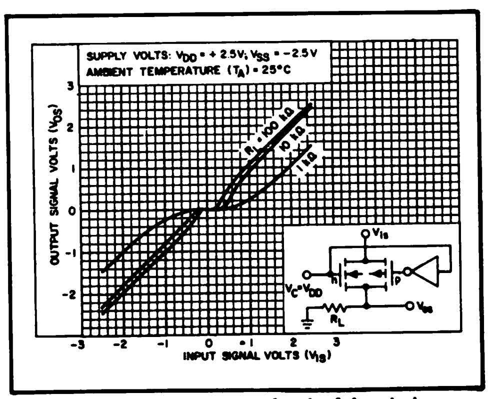
Typ. ON characteristics for 1 of 4 switches with V_{DD}=+5V, V_{SS}=0V



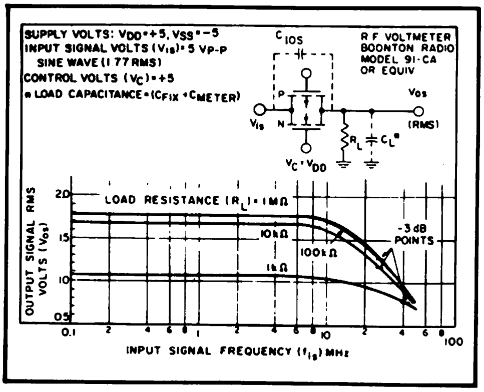
Typ. ON characteristics for 1 of 4 switches with V_{DD}=+7.5V, V_{SS}=-7.5V



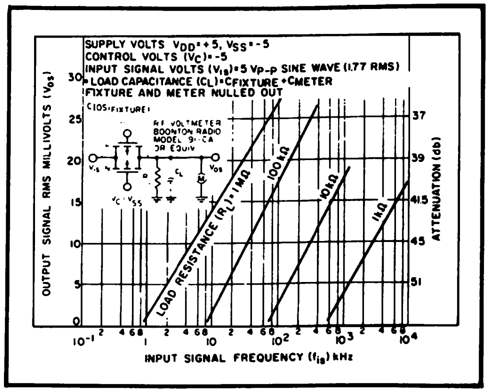
Typ. ON characteristics for 1 of 4 switches with V_{DD}=+5V, V_{SS}=-5V



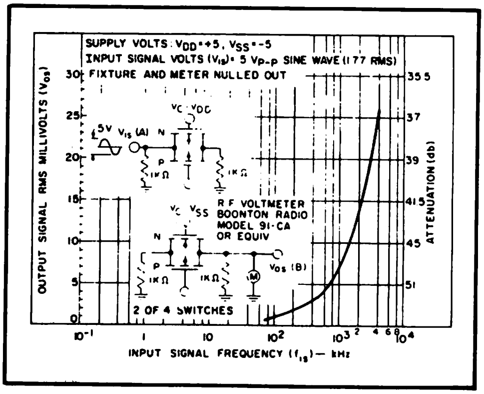
Typ. ON characteristics for 1 of 4 switches with V_{DD}=+2.5V, V_{SS}=-2.5V



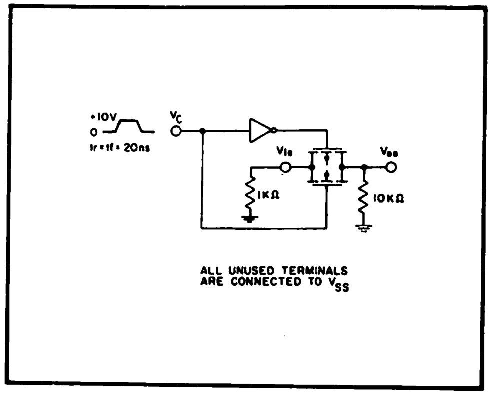
Typ. switch frequency response - switch ON



Typ. feedthru vs. freq. - switch OFF



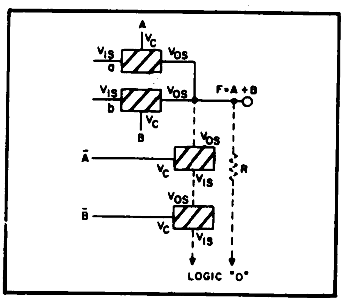
Typ. crosstalk between switch circuits in the same package



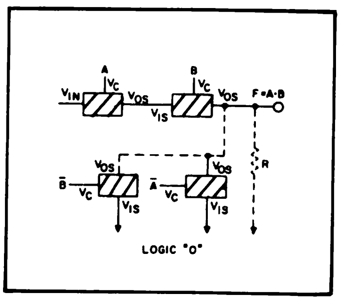
Crosstalk-control input to signal output

APPLICATIONS INFORMATION

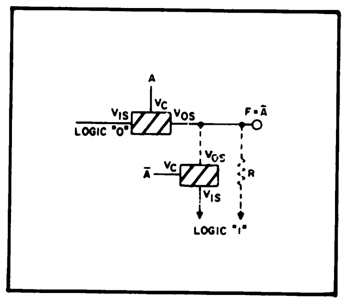
LOGIC FUNCTIONS USING THE 4016B



OR Gate



AND Gate

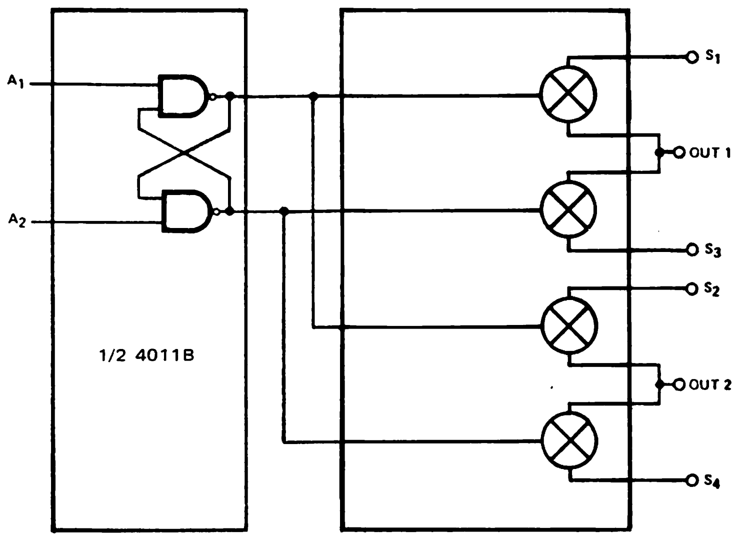


Inverter

APPLICATIONS INFORMATION (Continued)

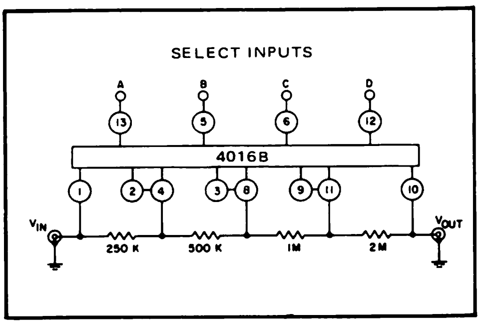
LATCHING DPDT SWITCH

The latch feature insures positive switching action in response to non-repetitive or erratic commands. A HIGH input to A_1 turns S_3 and S_4 ON, a HIGH to A_2 turns S_1 and S_2 ON. Desirable for use with limit detectors, peak detectors, or mechanical contact closures.

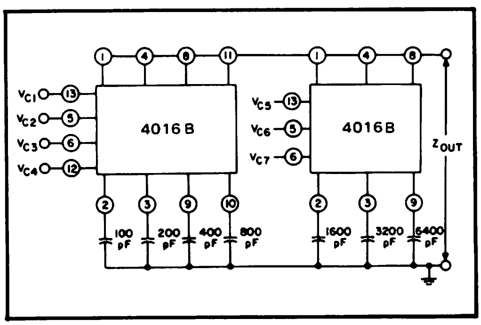


TRUTH TABLE

Command		State of Switches After Command	
A_2	A_1	S_3 & S_4	S_1 & S_2
0	0	Same	Same
0	1	On	Off
1	0	Off	On
1	1	INDETERMINATE	



Digitally controlled resistor network



Digitally-controlled capacitor network. ($V_{C1} \rightarrow V_{C7}$ are Select Inputs)

CMOS DECADE COUNTER/DIVIDER

FEATURES

- 10 Decoded Decimal Outputs
- Direct Reset
- Trigger from either Edge of Clock Input
- Carry Output for Cascading Stages
- Fully Static Operation—DC to 12MHz @ 10Vdc

DESCRIPTION

The 4017B consists of a 5-stage Johnson Decade Counter and an Output Decoder. Inputs include Clock, Reset, and Clock Enable signals.

The counter has interchangeable Clock and Clock Enable lines for incrementing on either a positive-going or negative-going transition, respectively. A high Reset signal clears the counter to its zero count.

Use of the Johnson decade counter configuration permits high-speed operation, 2-input decode gating, and spike-free decoded outputs. Anti-lock gating is provided, thus assuring proper counting sequence. The 10 decoded outputs are normally low and go high only at their respective decoded time slot. Each decoded output remains high for one full clock cycle. A Carry-out (C_{OUT}) signal completes one cycle every 10 clock input cycles and is used to directly clock the succeeding counter in multi-stage applications.

This part can be used in frequency division circuits as well as decade counter or decimal decode display applications.

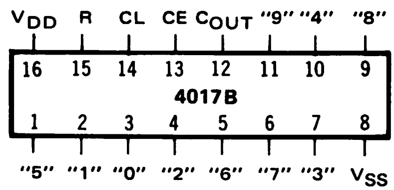
FUNCTIONAL TRUTH TABLE
(Positive Logic)

Clock	Clock Enable	Reset	Decode Output = n
0	X	0	n
X	1	0	n
X	X	1	"0"
$\uparrow$	0	0	n + 1
$\downarrow$	X	0	n
X	$\uparrow$	0	n
1	$\downarrow$	0	n + 1

x = Don't Care

If n < 5 Carry = "1", Otherwise = "0"

CONNECTION DIAGRAM
(all packages)

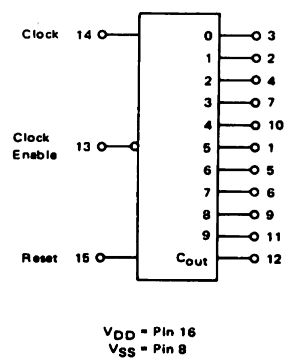


RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2]		+25°C			T_{HIGH} [2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN}=V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	μAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		15	combinations	–	20	–	0.2	20	–	600	

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

ELECTRICAL CHARACTERISTICS

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME To Decoded Outputs	t_{PLH}, t_{PHL}	5 10 15	-- – –	350 200 150	700 400 300	ns
To Carry Output	t_{PLH}, t_{PHL}	5 10 15	– – –	325 175 125	650 350 250	ns
OUTPUT TRANSITION TIME Decoded Outputs	t_{TLH}, t_{THL}	5 10 15	– – –	100 50 40	200 100 80	ns
Carry Output	t_{TLH}, t_{THL}	5 10 15	– – –	100 50 40	200 100 80	ns
MINIMUM CLOCK PULSE WIDTH	PW_{CL}	5 10 15	– – –	100 40 30	200 70 60	ns
MAXIMUM CLOCK FREQUENCY	f_{CL}	5 10 15	2.5 7.0 9.3	5.0 12.0 16.0	– – –	MHz
MAXIMUM CLOCK OR ENABLE RISE AND FALL TIME	t_{rCL}, t_{fCL}	5 10 15	NO LIMIT			
MINIMUM ENABLE SETUP TIME	t_{setup}	5 10 15	– – –	100 50 35	300 100 70	ns
MINIMUM ENABLE REMOVAL TIME	t_{rem}	5 10 15	– – –	250 100 75	500 200 150	ns
RESET OPERATION						
PROPAGATION DELAY TIME To Decoded Outputs	t_{PLH}, t_{PHL}	5 10 15	– – –	325 175 125	650 350 250	ns
To Carry Output	t_{PLH}, t_{PHL}	5 10 15	– – –	325 175 125	650 350 250	ns
MINIMUM RESET PULSE WIDTH	PW_R	5 10 15	– – –	150 75 60	300 150 120	ns
RESET REMOVAL TIME	t_{rem}	5 10 15	– – –	250 100 80	500 200 1.60	ns

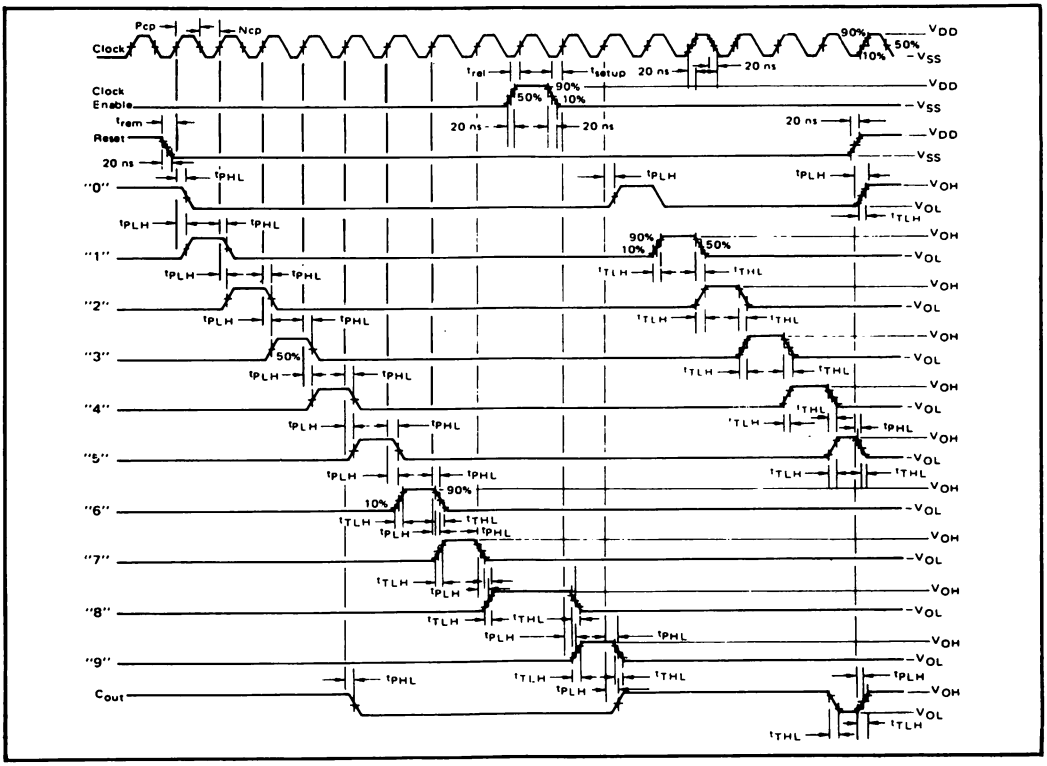
STATIC CHARACTERISTICS[1]

PARAMENTER	V_{DD}	CONDITIONS	T_{LOW}[2]		25°C			T_{HIGH}[2]		Units
			Min	Max	Min	Typ	Max	Min	Max	
QUIESCENT DEVICE CURRENT	5 10 15	$V_{IN} = V_{SS}$ or V_{DD} All Valid Input Combinations	– – –	5 10 20	– – –	– – –	5 10 20	– – –	150 300 600	μAdc

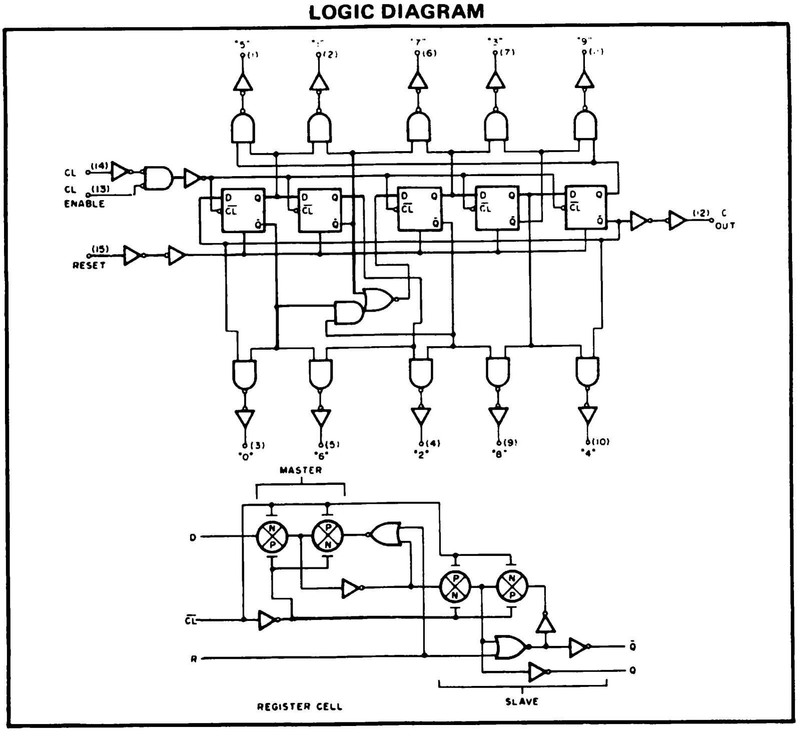
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications"

[2] T_{LOW} = – 55°C for C, D, F, H devices.
= – 40°C for E devices.
T_{HIGH} = + 125°C for C, D, F, H devices.
= + 85°C for E devices.

AC MEASUREMENT DEFINITION AND FUNCTIONAL WAVEFORMS



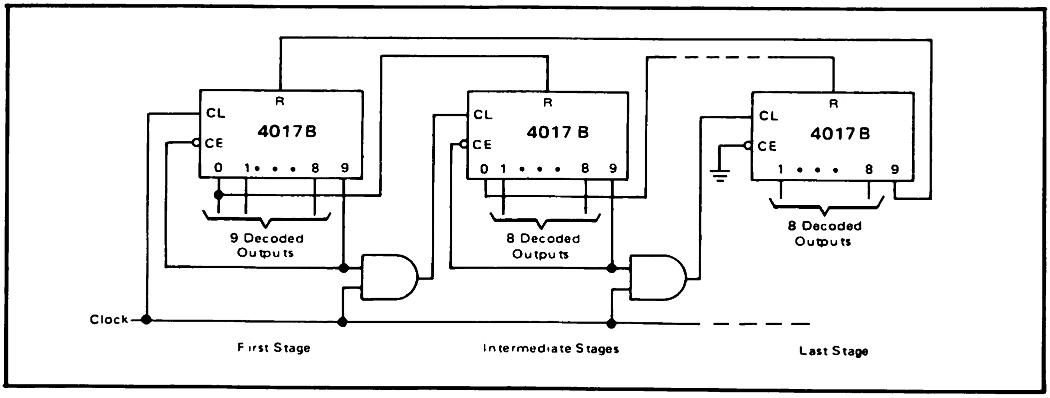
LOGIC DIAGRAM



APPLICATIONS INFORMATION

COUNTER EXPANSION

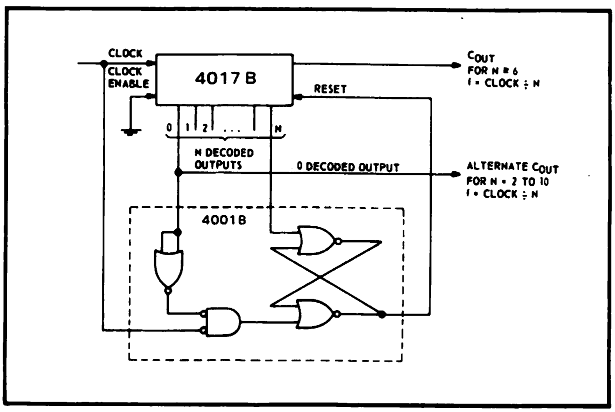
This figure shows a technique for extending the number of decoded output states for the 4017B. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).



DIVIDE-BY-N COUNTER

When the Nth decoded output is reached (Nth clock pulse), the S-R flip-flop (constructed from the 4001B) generates a reset pulse which clears the 4017B to its zero count. At this time, if the Nth decoded output is greater than or equal to 6, the C_{OUT} line goes high to clock the next counter section. The "O" decoded output also goes high at this time. Coincidence of the clock "low" and decoded "O" output "high" resets the S-R flip-flop to enable the 4017B.

If the Nth decoded output is less than 6, the C_{OUT} line will not go high, and, therefore, cannot be used. In this case, the "O" decoded output may be used to perform the clock function for the next counter.



SOLID STATE SCIENTIFIC

SCL4018B

CMOS PRESETTABLE TABLE DIVIDE-BY-N COUNTER

FEATURES

- Divide by any Number Between 2 and 10 with One External Gate
- Johnson Counter Configuration for Spike-Free Counting
- Fully Static operation - DC to 5MHz @ 10Vdc

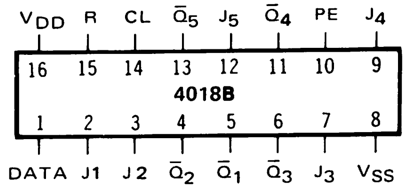
DESCRIPTION

The 4018B consists of 5 Johnson-Counter stages, buffered Q outputs from each stage, and counter preset control gating. Clock, Reset, Data, Preset Enable, and 5 individual Jam inputs are provided. Divide-by 10, 8, 6, 4, or 2 counter configurations can be implemented by feeding the Q5, Q4, Q3, Q2, Q1 signals, respectively, back to the Data input. Divide-by-9, 7, 5, or 3 counter configurations can be implemented by use of a single SCL4081B gate to properly gate the feedback connections to the Data input. Divide-by functions greater than 10 can be achieved by use of multiple 4018B units. The counter is advanced one count at the positive clock-signal transition. A high Reset signal clears the counter to an all-zero condition. A high Preset-Enable signal allows information on the Jam inputs to preset the counter. Reset and Preset gating is provided to assure the proper counting sequence.

This device is particularly useful in frequency-division and control applications.

CONNECTION DIAGRAM

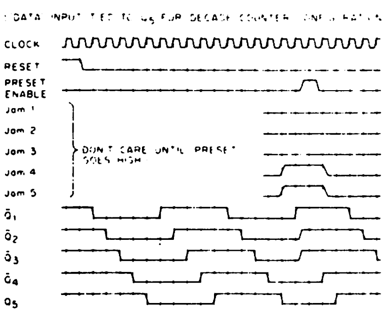
(all packages)



Add suffix for package:

C	16-pin Cerdip
D	16-pin Ceramic
E	16-pin Epoxy
F	16-pin Flat
H	Chip

TIMING DIAGRAM

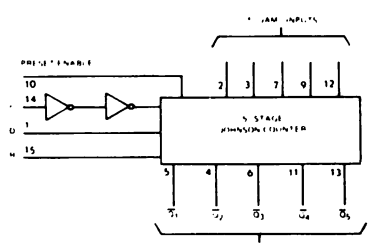


RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS[1]

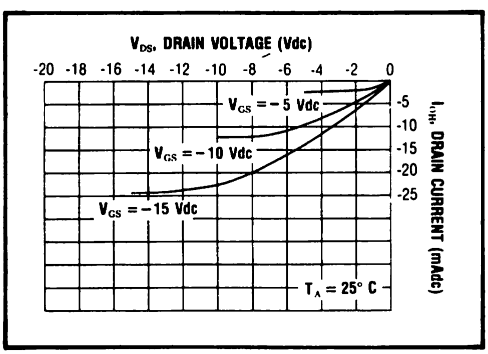
PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[2] Min.	T_{LOW}[2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH}[2] Min.	T_{HIGH}[2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN}=V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	μAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		15	combinations	–	20	–	0.2	20	–	600	

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

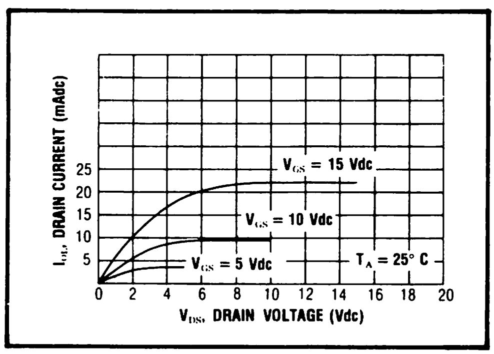
DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}	5	–	500	1000	ns
		10	–	150	300	
		15	–	120	240	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	130	260	ns
		10	–	65	130	
		15	–	50	100	
MINIMUM CLOCK PULSE WIDTH	PW_{CL}	5	–	200	400	ns
		10	–	100	200	
		15	–	80	160	
MAXIMUM CLOCK FREQUENCY	f_{CL}	5	1.25	2.5	–	MHz
		10	2.5	5.0	–	
		15	3.0	6.0	–	
MAXIMUM CLOCK RISE AND FALL TIME[1]	t_{rCL}, t_{fCL}	5	15	–	–	μs
		10	15	–	–	
		15	5	–	–	
MIMIMUM DATA INPUT SETUP TIME	t_{setup}	5	–	200	400	ns
		10	–	100	200	
		15	–	80	160	
MINIMUM DATA INPUT HOLD TIME	t_{hold}	5	–	0	100	ns
		10	–	0	50	
		15	–	0	40	
PRESET OR RESET OPERATION						
PROPAGATION DELAY TIME From PE or Reset Input	t_{PLH}, t_{PHL}	5	–	500	1000	ns
		10	–	250	500	
		15	–	200	400	
MINIMUM PRESET OR RESET PULSE WIDTH	PW_{PR}, PW_R	5	–	200	400	ns
		10	–	100	200	
		15	–	80	160	
MINIMUM JAM INPUT SETUP TIME	t_{setup}	5	–	200	400	ns
		10	–	100	200	
		15	–	80	160	
PRESET OR RESET REMOVAL TIME	t_{rem}	5	–	375	750	ns
		10	–	125	250	
		15	–	90	180	

[1] When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.

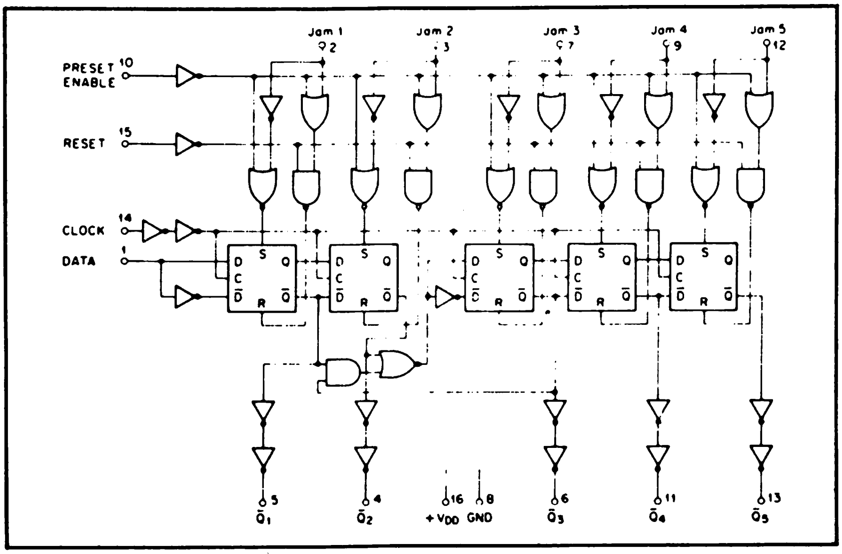


Typical P-Channel
Source Current Characteristics

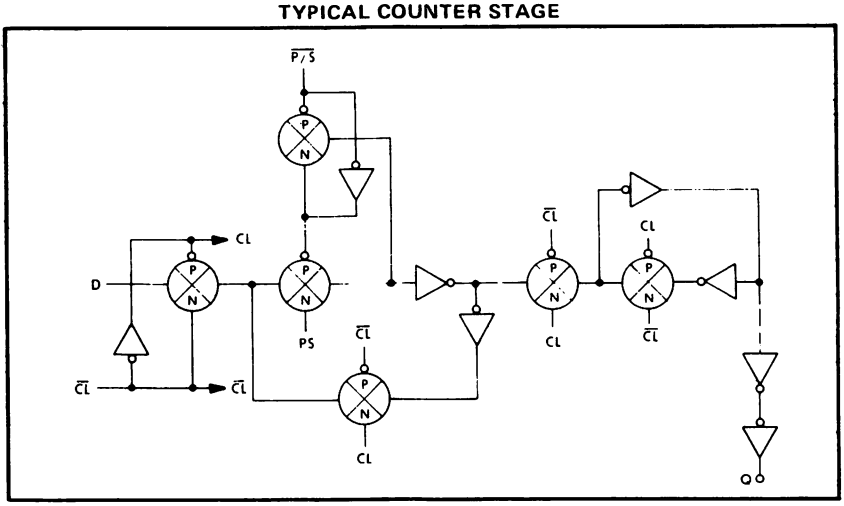


Typical N-Channel
Sink Current Characteristics

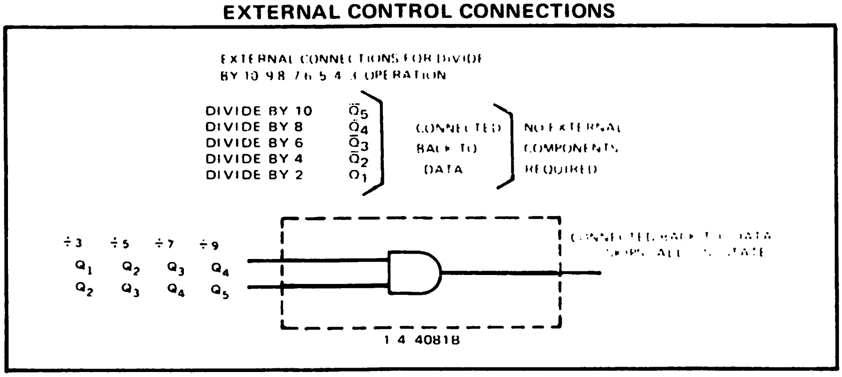
LOGIC DIAGRAM



TYPICAL COUNTER STAGE



EXTERNAL CONTROL CONNECTIONS



SOLID STATE SCIENTIFIC

SCL4019B

CMOS QUAD AND-OR SELECT GATE

FEATURES

- Replaces Three Simple Gate Packages
- Medium Speed Operation
- All Inputs Diode-Protected
- All Outputs Buffered

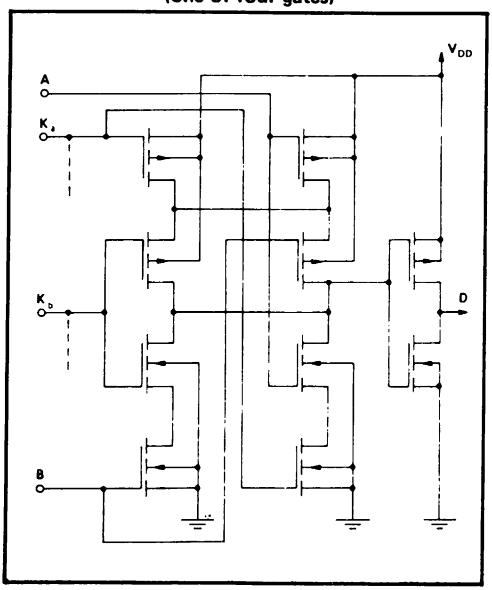
DESCRIPTION

The 4019B is comprised of four "AND-OR Select" gate configurations, each consisting of two 2-input AND gates driving a single 2-input OR gate. Selection is accomplished by control bits K_a and K_b. In addition to selection of either channel A or channel B information, the control bits can be applied simultaneously to accomplish the logical A + B function.

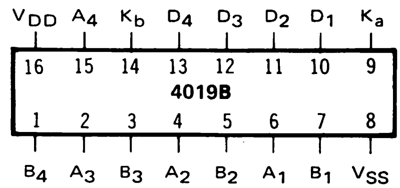
TRUTH TABLE
(one of four gates)

K_a	K_b	D
0	0	0
1	0	A
0	1	B
1	1	A+B

SCHEMATIC DIAGRAM
(one of four gates)



CONNECTION DIAGRAM
(all packages)



Add suffix for package:

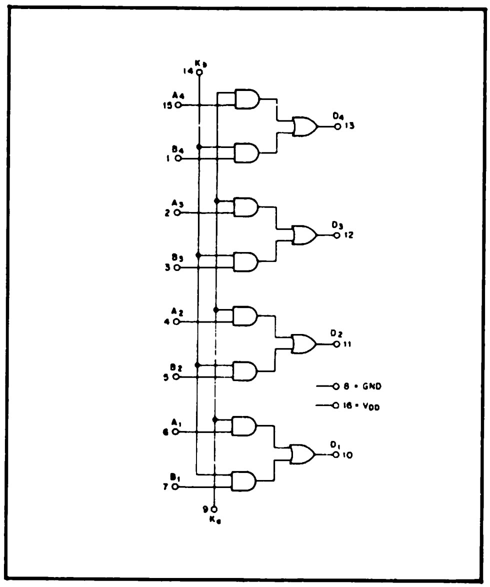
C	16-pin Cerdip
D	16-pin Ceramic
E	16-pin Epoxy
F	16-pin Flat
H	Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

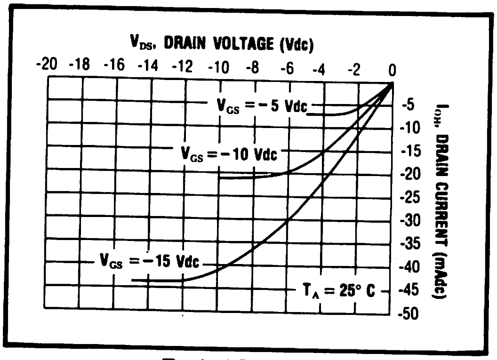
STATIC CHARACTERISTICS [1]

PARAMETER		VDD (Vdc)	CONDITIONS	T_{LOW} [2]		+25°C			T_{HIGH} [2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN}=V_{SS}$ or V_{DD}	–	1.0	–	0.005	1.0	–	30	μAdc
		10	All valid input	–	2.0	–	0.01	2.0	–	60	
		15	combinations	–	4.0	–	0.02	4.0	–	120	

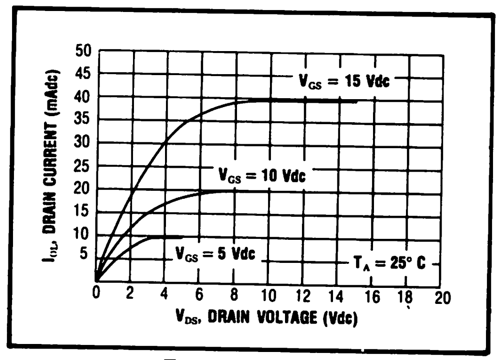
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = −55°C for C, D, F, H device.
= −40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

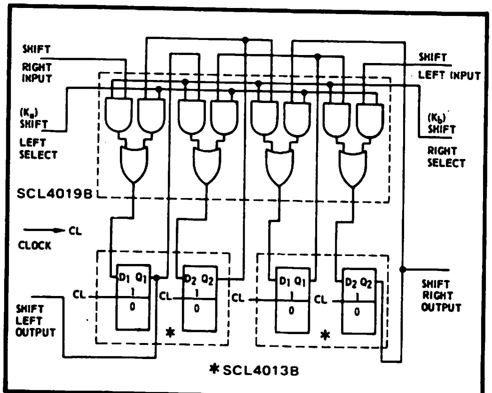
PARAMETER		VDD (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME From Any Input	t_{PLH}, t_{PHL}	5	–	150	300	ns
		10	–	60	120	
		15	–	50	100	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	



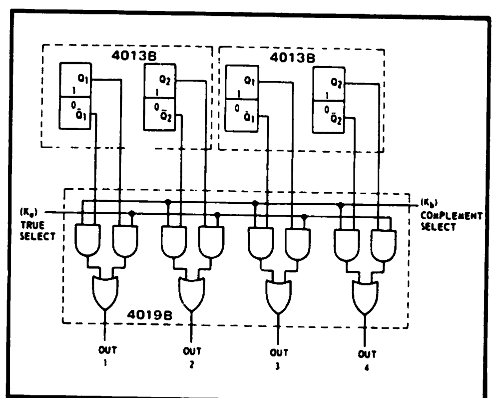
Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics



"Shift left/shift right" register.



"True/complement" selector.

CMOS 14-STAGE BINARY COUNTER

FEATURES

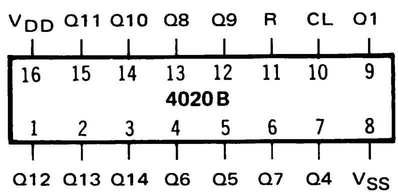
- 14 Fully Static Stages
- Buffered Outputs Available from 12 Stages
- Common Reset Line
- 8MHz Counting Rate @ 10Vdc
- All Inputs Buffered

DESCRIPTION

The 4020B consists of 14 ripple-carry binary counter stages with appropriate input buffers and reset circuitry. Buffered outputs are externally available from stages 1, and 4 through 14. The counter is reset to its "all zeroes" state by a high level on the Reset input. The counter is advanced one count on the negative-going transition of each input pulse. Isolation from external noise and the effects of loading is provided by output buffering.

Applications include time delay circuits, counter controls, and frequency-dividing circuits.

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

C	16-pin Cerdip
D	16-pin Ceramic
E	16-pin Epoxy
F	16-pin Flat
H	Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

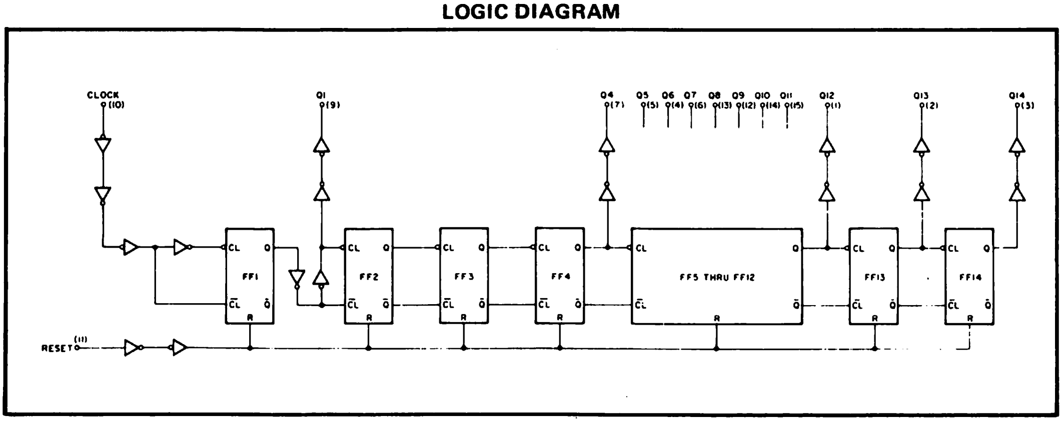
DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

TRUTH TABLE

CLOCK	RESET	OUTPUT STATE
	0	No Change
	0	Advance to next state
X	1	All Outputs are low

X = Don't Care

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

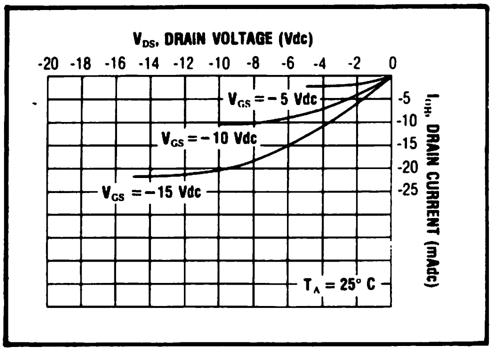
STATIC CHARACTERISTICS[1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[2] Min.	T_{LOW}[2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH}[2] Min.	T_{HIGH}[2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN}=V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	μAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		15	combinations	–	20	–	0.2	20	–	600	

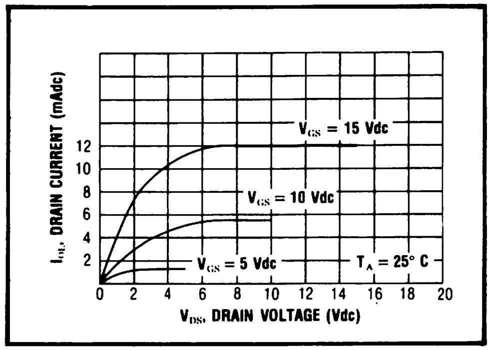
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME Clock to Q1	t_{PLH}, t_{PHL}	5	–	180	360	ns
		10	–	80	160	
		15	–	65	130	
Q_i to Q_i +1	t_{PLH}, t_{PHL}	5	–	100	200	ns
		10	–	40	80	
		15	–	30	60	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	40	80	
		15	–	30	60	
MINIMUM CLOCK PULSE WIDTH	PW_{CL}	5	–	70	140	ns
		10	–	30	60	
		15	–	20	40	
MAXIMUM CLOCK FREQUENCY	f_{CL}	5	3.0	4.5	–	MHz
		10	6.0	9.0	–	
		15	7.5	11.0	–	
MAXIMUM CLOCK RISE AND FALL TIME	t_{rCL}, t_{fCL}	5	–	100	50	μs
		10	–	100	50	
		15	–	100	50	
RESET OPERATION						
PROPAGATION DELAY TIME	t_{PHL}	5	–	200	400	ns
		10	–	100	200	
		15	–	75	150	
MINIMUM RESET PULSE WIDTH	PW_R	5	–	100	200	ns
		10	–	40	80	
		15	–	30	60	
RESET REMOVAL TIME	t_{rem}	5	–	150	300	ns
		10	–	65	125	
		15	–	40	75	

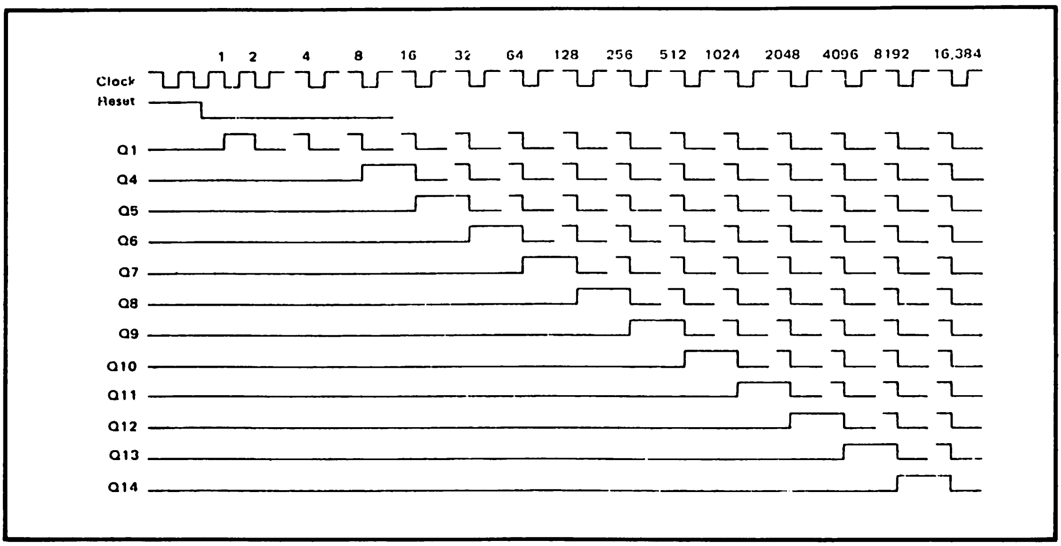


Typical P-Channel
Source Current Characteristics

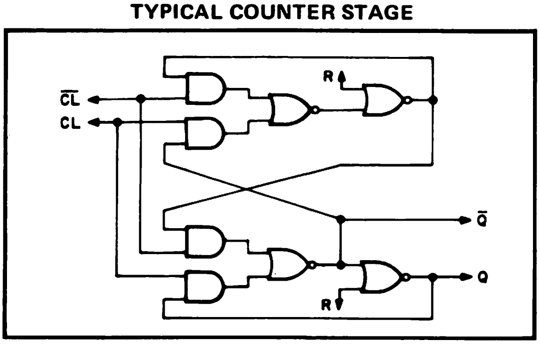


Typical N-Channel
Sink Current Characteristics

TIMING DIAGRAM



TYPICAL COUNTER STAGE



CMOS 8-STAGE STATIC SHIFT REGISTER

FEATURES

- Asynchronous Parallel Input/Serial Output
- Synchronous Serial Input/Serial Output
- Fully Static Operation - DC to 8MHz @ 10Vdc
- Q Outputs from Stages 6, 7, and 8 Available

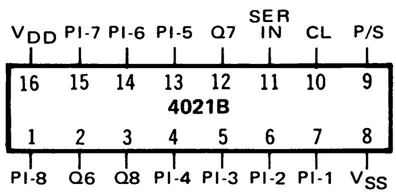
DESCRIPTION

The 4021B is an 8-Stage Parallel or Serial-Input/Serial-Output Shift Register having common Clock and Parallel/Serial Control inputs, a single Serial Data input, and individual parallel Jam inputs to each register stage. Each register stage is a D-type, master-slave flip-flop. "Q" outputs are available from the sixth, seventh, and eighth stages. When the Parallel/Serial Control input is low, data is serially shifted into the 8-stage register synchronously with the positive-going transition of the Clock pulse.

When the Parallel/Serial Control input is "high" data is jammed into the 8-stage register via the Parallel input line asynchronously with the Clock line.

Register expansion is possible using additional 4021B packages.

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

C 16-pin Cerdip
D 16-pin Ceramic
E 16-pin Epoxy
F 16-pin Flat
H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

TRUTH TABLE

SERIAL OPERATION:

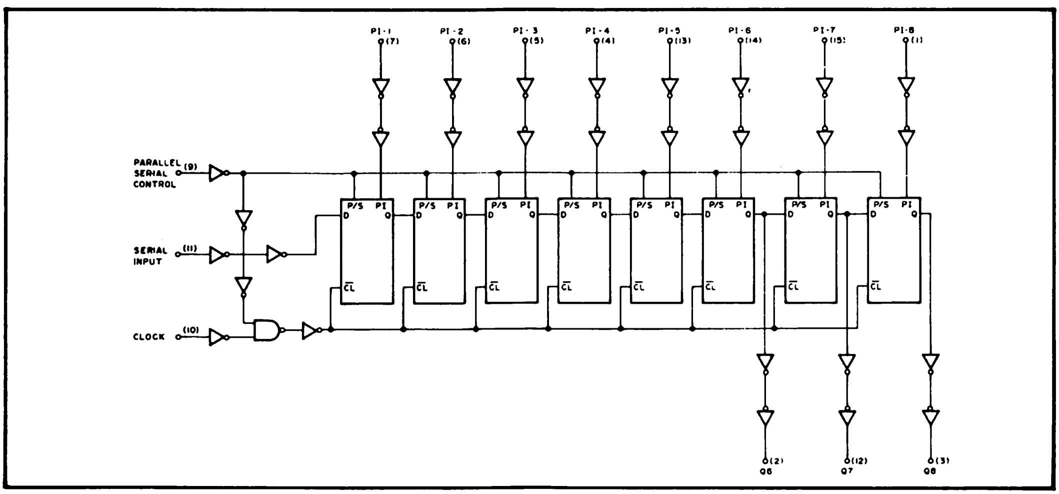
t	CLOCK	SER IN	P/S	Q6 t=n+6	Q7 t=n+7	Q8 t=n+8
n	_/‾	0	0	0	?	?
n+1	_/‾	1	0	1	0	?
n+2	_/‾	0	0	0	1	0
n+3	_/‾	1	0	1	0	1
	‾_	X	0	Q6	Q7	Q8

PARALLEL OPERATION:

CLOCK	SER IN	P/S	PI-m	*Q_m
X	X	1	0	0
X	X	1	1	1

*Q6, Q7, & Q8 are available externally
X = Don't Care

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS [1]

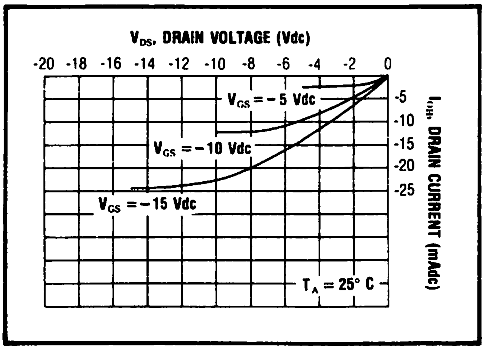
PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2]		+25°C			T_{HIGH} [2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN} = V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	μAdc
		10	All valid input	–	10	–	0.01	10	–	300	
		15	combinations	–	20	–	0.2	20	–	600	

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

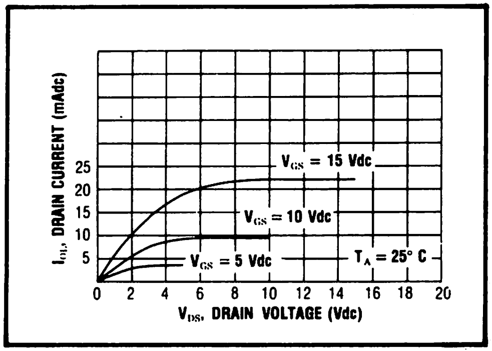
DYNAMIC CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}	5	–	180	360	ns
From Clock or P/S Input		10	–	90	180	
		15	–	75	150	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
MINIMUM CLOCK PULSE WIDTH	PW_{CL}	5	–	90	180	ns
		10	–	40	80	
		15	–	25	50	
MAXIMUM CLOCK FREQUENCY	f_{CL}	5	3	5	–	MHz
		10	6	12	–	
		15	8	16	–	
MAXIMUM CLOCK RISE & FALL TIME[1]	t_{rCL}, t_{fCL}	5	15	–	–	μs
		10	15	–	–	
		15	15	–	–	
MINIMUM P/S PULSE WIDTH	PW	5	–	80	160	ns
		10	–	40	80	
		15	–	25	50	
MINIMUM SETUP TIME	t_{setup}	5	–	60	120	ns
Parallel or Serial Inputs		10	–	40	80	
		15	–	30	60	
MINIMUM HOLD TIME	t_{hold}	5	–	100	200	ns
Parallel or Serial Inputs		10	–	30	60	
		15	–	20	40	
P/S REMOVAL TIME	t_{rem}	5	–	140	280	ns
		10	–	70	140	
		15	–	50	100	

[1] When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.

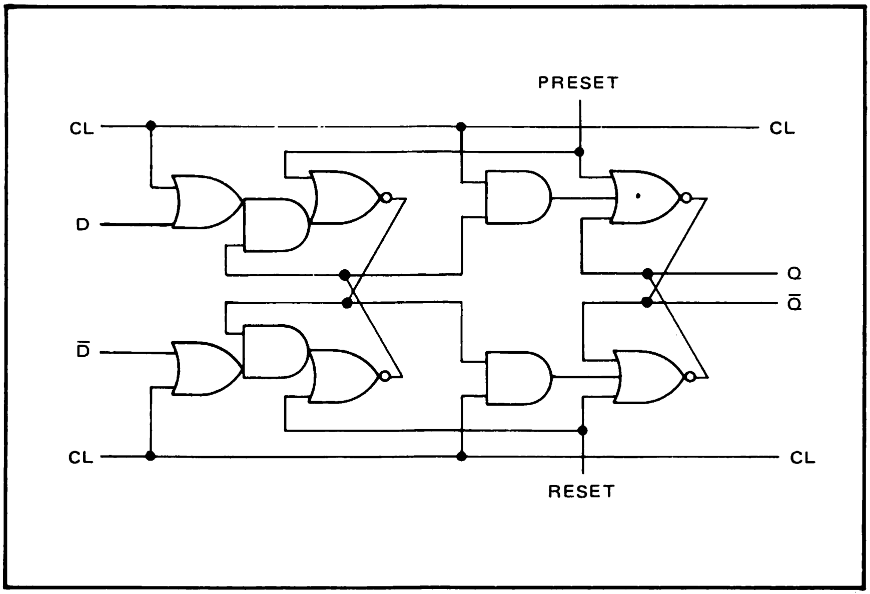


Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

TYPICAL REGISTER STAGE



CMOS OCTAL COUNTER/DIVIDER

FEATURES

- Eight Decoded Outputs
- Direct Reset
- Trigger from either Edge of Clock Input
- Carry Output for Cascading Stages
- Fully Static Operation - DC to 5MHz @ 10Vdc

DESCRIPTION

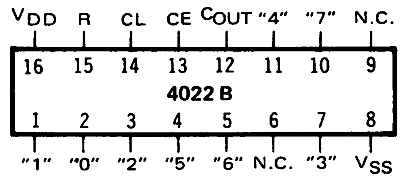
The 4022 B consists of a 4-stage Johnson Divide-by-8 Counter and an Output Decoder. Inputs include Clock, Reset, and Clock Enable signals.

The counter has interchangeable Clock and Clock Enable lines for incrementing on either a positive-going or negative-going transition, respectively. A high Reset signal clears the counter to its zero count.

Use of the Johnson divide-by-eight counter configuration permits high-speed operation, 2-input decode gating, and spike-free decoded outputs. Anti-lock gating is provided, thus assuring proper counting sequence. The 8 decoded outputs are normally low and go high only at their respective decoded time slot. Each decoded output remains high for one full clock cycle. A Carry-out (C_{OUT}) signal completes one cycle every 8 clock input cycles and is used to directly clock the succeeding counter in multi-stage applications.

This part can be used in frequency division circuits as well as octal counter or octal decode display applications.

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

C	16-pin Cerdip
D	16-pin Ceramic
E	16-pin Epoxy
F	16-pin Flat
H	Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

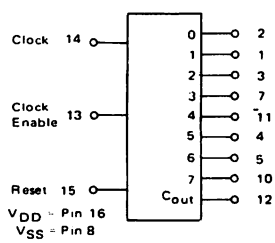
DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

FUNCTIONAL TRUTH TABLE
(Positive Logic)

Clock	Clock Enable	Reset	Output = n
0	X	0	n
X	1	0	n
↑	0	0	n + 1
↓	X	0	n
1	↓	0	n + 1
X	↑	0	n
X	X	1	"0"

X Don't Care   If n < 4 Carry = 1, otherwise = 0

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2]		+25°C			T_{HIGH} [2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN} = V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	µAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		15	combinations	–	20	–	0.2	20	–	600	

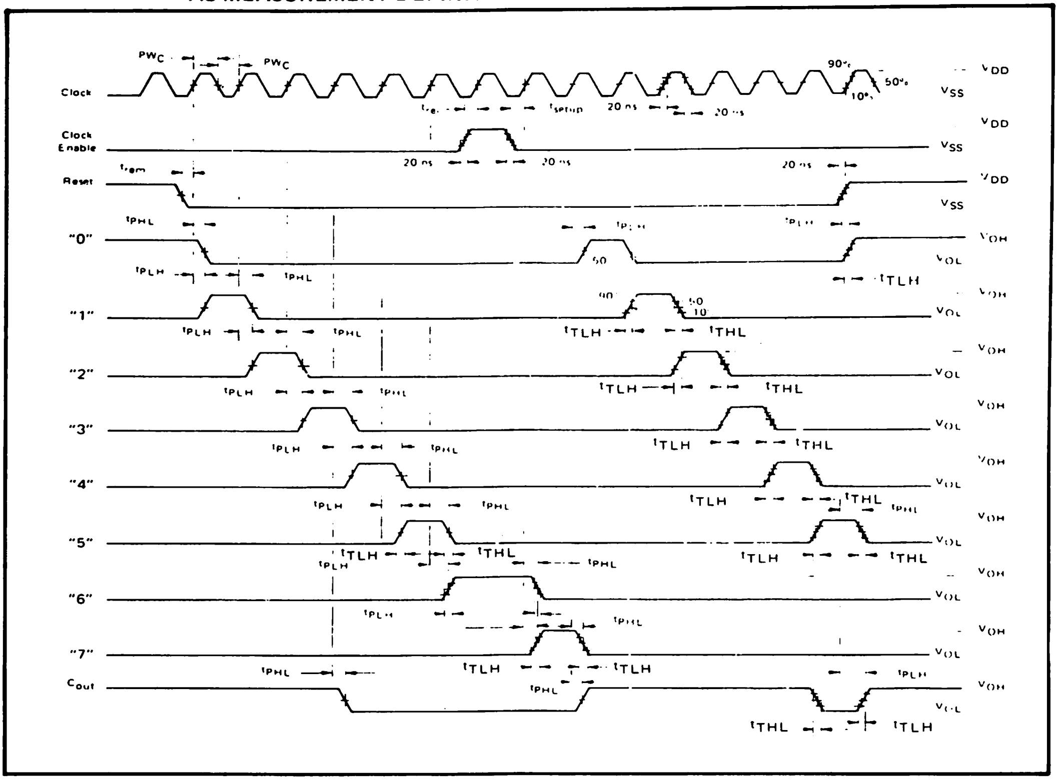
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

ELECTRICAL CHARACTERISTICS (Continued)

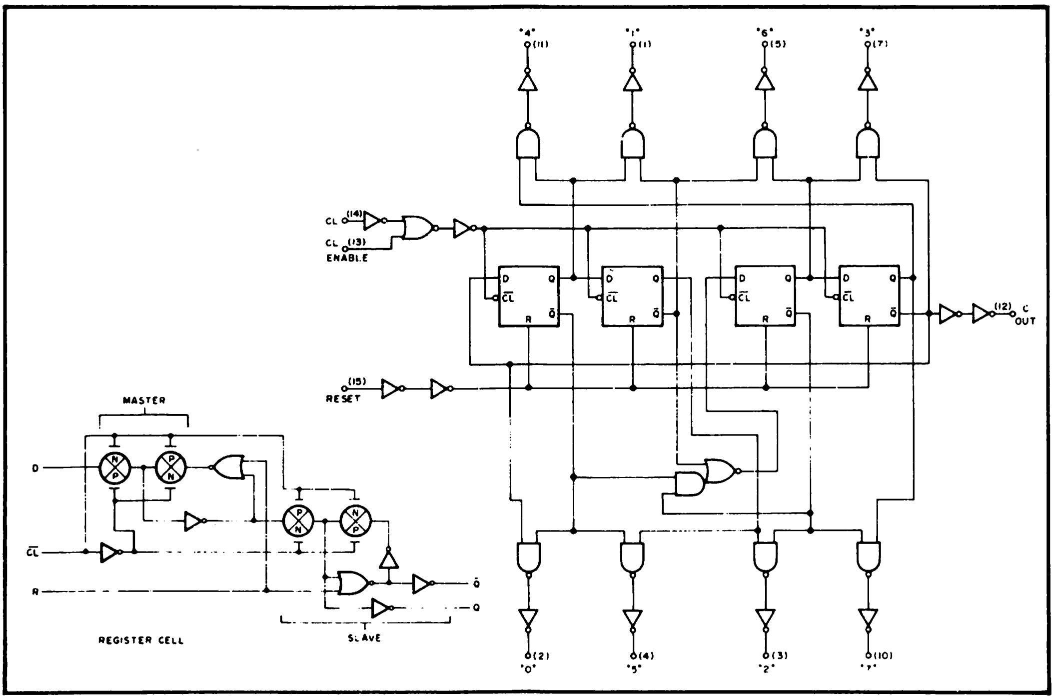
DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME To Decoded Outputs	t_{PLH}, t_{PHL}	5 10 15	– – –	600 240 180	1200 480 360	ns
To Carry Output	t_{PLH}, t_{PHL}	5 10 15	– – –	500 200 150	1000 400 300	ns
OUTPUT TRANSITION TIME Decoded Outputs	t_{TLH}, t_{THL}	5 10 15	– – –	250 125 90	500 250 180	ns
Carry Output	t_{TLH}, t_{THL}	5 10 15	– – –	180 90 65	360 180 130	ns
MINIMUM CLOCK PULSE WIDTH	PW_{CL}	5 10 15	– – –	200 100 80	400 200 160	ns
MAXIMUM CLOCK FREQUENCY	f_{CL}	5 10 15	1.25 2.5 3.0	2.5 5.0 6.0	– – –	MHz
MAXIMUM CLOCK OR ENABLE RISE AND FALL TIME	t_{rCL}, t_{fCL}	5 10 15	15 15 5	– – –	– – –	μs
MINIMUM ENABLE SETUP TIME	t_{setup}	5 10 15	– – –	175 75 55	350 150 110	ns
MINIMUM ENABLE REMOVAL TIME	t_{rem}	5 10 15	– – –	250 100 75	500 200 150	ns
RESET OPERATION						
PROPAGATION DELAY TIME To Decoded Outputs	t_{PLH}, t_{PHL}	5 10 15	– – –	500 200 140	1000 400 280	ns
To Carry Output	t_{PLH}	5 10 15	– – –	400 150 110	800 300 220	ns
MINIMUM RESET PULSE WIDTH	PW_R	5 10 15	– – –	150 75 60	300 150 120	ns
RESET REMOVAL TIME	t_{rem}	5 10 15	– – –	250 100 80	500 200 160	ns

AC MEASUREMENT DEFINITION AND FUNCTIONAL WAVEFORMS



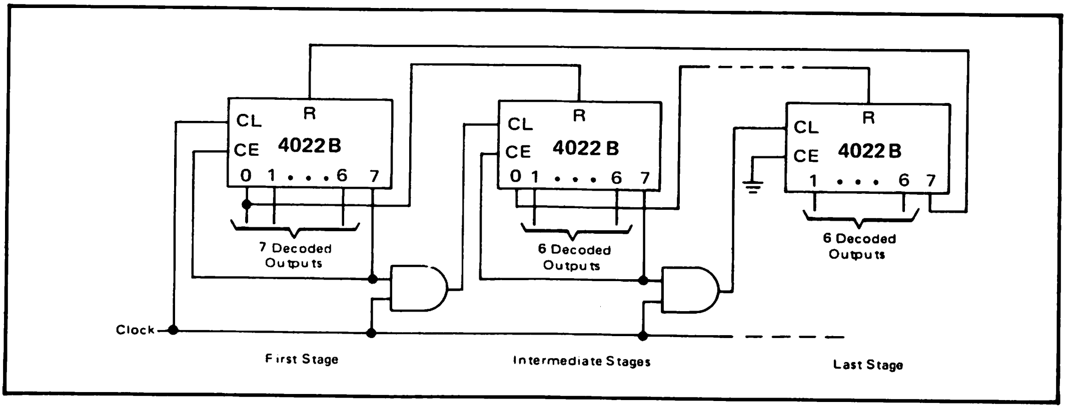
LOGIC DIAGRAM



APPLICATIONS INFORMATION

COUNTER EXPANSION

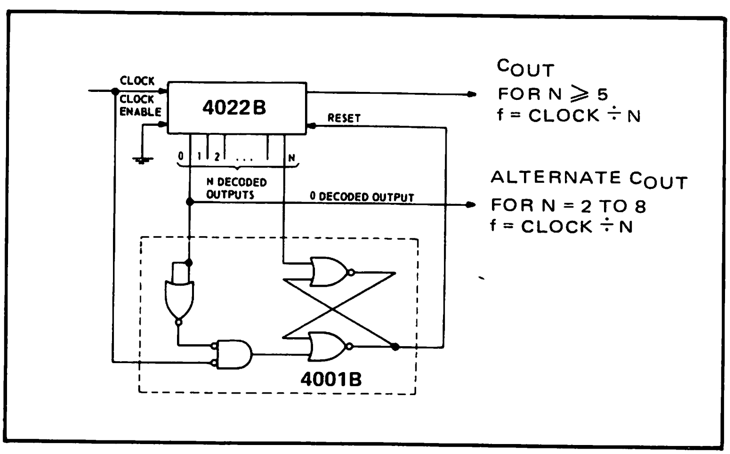
This figure shows a technique for extending the number of decoded output states for the 4022 B. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).



DIVIDE-BY-N-COUNTER

When the Nth decoded output is reached (Nth clock pulse) the S-R flip-flop (constructed from the 4001B) generates a reset pulse which clears the 4022B to its zero count. At this time, if the Nth decoded output is greater than or equal to 4, the C_{OUT} line goes high to clock the next counter section. The "0" decoded output also goes high at this time. Coincidence of the clock "low" and decoded "0" output "high" resets the S-R flip-flop to enable the 4022B.

If the Nth decoded output is less than 4, the C_{OUT} line will not go high, and, therefore, cannot be used. In this case, the "0" decoded output may be used to perform the clock function for the next counter.



CMOS 7-STAGE BINARY COUNTER

FEATURES

- 7 Fully Static Stages
- Buffered Outputs Available from All Stages
- Common Reset Line
- 8 MHz Counting Rate @ 10Vdc
- All Inputs Buffered

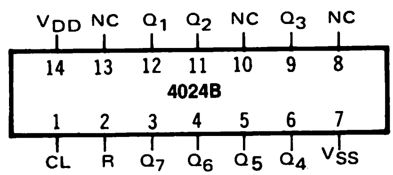
DESCRIPTION

The 4024B is a single chip monolithic medium scale integrated circuit containing N-Channel and P-Channel enhancement-mode MOS transistors. Seven single-phase clocked counting stages are provided with the Q output of each stage accessible. The Counter is reset to "zero" by a high level on the Reset input. Each counter stage is a static master-slave flip-flop. The counter state is advanced one count on the negative-going transition of each input pulse.

TRUTH TABLE

Clock	Reset	State
0	0	No Change
0	1	All Outputs Low
1	0	No Change
1	1	All Outputs Low
_/‾	0	No Change
_/‾	1	All Outputs Low
‾_	0	Advance One Count
‾_	1	All Outputs Low

CONNECTION DIAGRAM
(all packages)

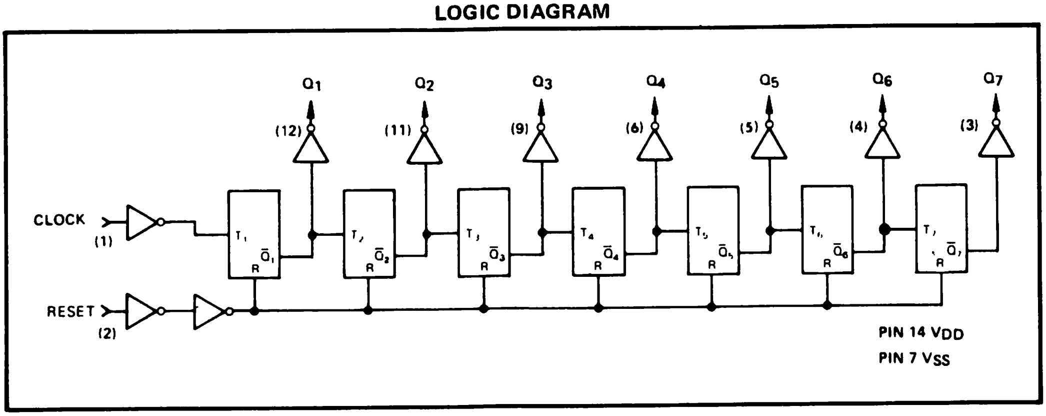


RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

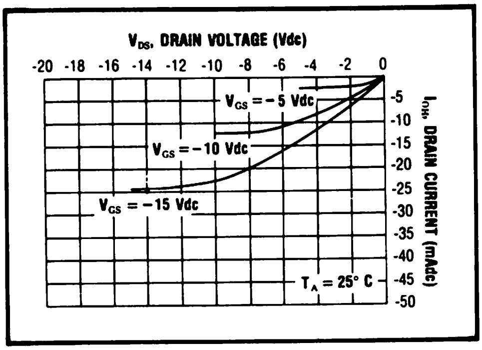
STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2]		+25°C			T_{HIGH} [2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN} = V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	μAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		15	combinations	–	20	–	0.2	20	–	600	

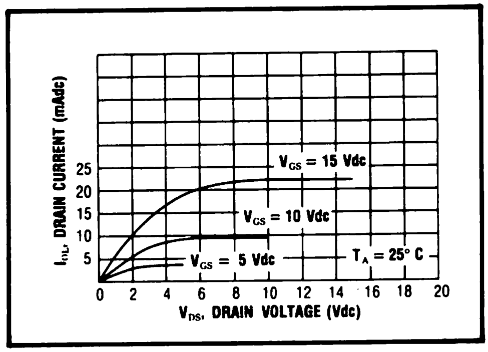
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME Clock to Q_1	t_{PLH}, t_{PHL}	5	–	180	360	ns
		10	–	80	160	
		15	–	65	130	
Q_i to Q_{i+1}	t_{PLH}, t_{PHL}	5	–	100	200	ns
		10	–	40	80	
		15	–	30	60	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
MINIMUM CLOCK PULSE WIDTH	PW_{CL}	5	–	120	240	ns
		10	–	60	120	
		15	–	45	90	
MAXIMUM CLOCK FREQUENCY	f_{CL}	5	2	4	—	MHz
		10	5	10	—	
		15	6	12	—	
MAXIMUM CLOCK RISE AND FALL TIME	t_{rCL}, t_{fCL}	5	15	–	—	μs
		10	10	–	—	
		15	5	–	—	
RESET OPERATION						
PROPAGATION DELAY TIME	t_{PHL}	5	–	200	400	ns
		10	–	100	200	
		15	–	80	160	
MINIMUM RESET PULSE WIDTH	PW_R	5	–	200	400	ns
		10	–	100	200	
		15	–	80	160	
RESET REMOVAL TIME	t_{rem}	5	–	200	400	ns
		10	–	100	200	
		15	–	80	160	

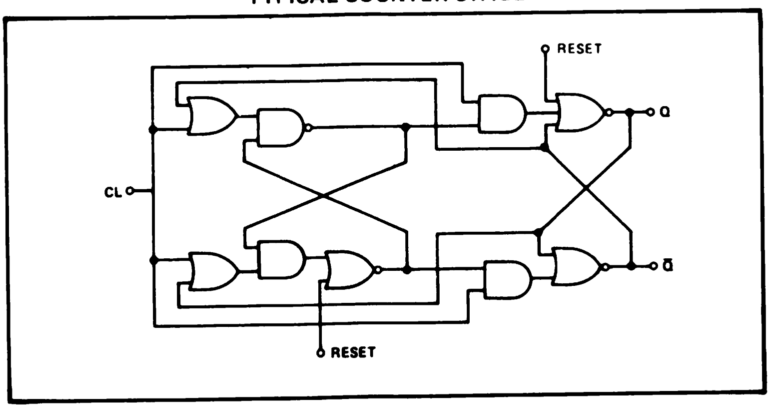


Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

TYPICAL COUNTER STAGE



CMOS DECADE 7-SEGMENT DECODERS

FEATURES

- Decade Counter and 7-Segment Decoder in One Package
- Easily Interfaced with 7-Segment Display Types
- Direct Reset
- Display Enable Function (4026AB)
- Ripple Blanking and Lamp Test Functions (4033AB)
- Trigger from either Edge of Clock Input
- Carry Output for Cascading Stages
- Fully Static Operation - DC to 5MHz @ 10Vdc

DESCRIPTION

These two devices each consist of a 5-stage Johnson Decade Counter and an Output Decoder which converts the Johnson code to a 7-segment decoded output for driving each stage in a numerical display. A high Reset signal clears the decade counter to its zero count. The counters have interchangeable Clock and Clock Enable lines for incrementing on either a positive-going or negative-going transition, respectively. Antilock gating is provided on the Johnson counter, thus assuring proper counting sequence. The Carry-Out (C_{OUT}) signal completes one cycle every ten clock input cycles and is used to directly clock the succeeding decade in a multi-decade counting chain.

4026AB

When the Display Enable is low, the seven decoded outputs are forced off regardless of the state of the counter. Activation of the display only when required results in significant power savings. This system also facilitates implementation of display-character multiplexing.

The Carry Out and ungated "C-segment" signals are not gated by the Display Enable and therefore are available continuously. This feature is a requirement in implementation of certain divider functions such as divide-by-60 and divide-by-12.

4033AB

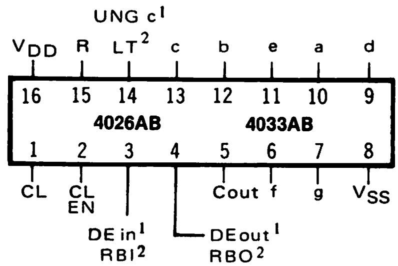
The 4033AB has provisions for automatic blanking of the non-significant zeros in a multi-digit decimal number which results in an easily readable display consistent with normal writing practice. For example, the number 0050.0700 in an eight digit display would be displayed as 50.07. Zero suppression on the integer side is obtained by connecting the RBI terminal of the 4033AB associated with the most significant digit in the display to a "low-level" voltage and connecting the RBO terminal of that stage to the RBI terminal of the 4033AB in the next-lower-significant position in the display. This procedure is continued for each succeeding 4033AB on the integer side of the display. On the fraction side of the display the RBI of the 4033AB associated with the least significant digit is connected to a "low-level" voltage and the RBO of the 4033AB is connected to the RBI terminal of the 4033AB in the next-more-significant-digit position. Again, this procedure is continued for each 4033AB on the fraction side of the display.

In a purely fractional number the zero immediately preceding the decimal point can be displayed by connecting the RBI of that stage to a high voltage (instead of to the RBO of the next-more-significant stage). For Example: optional zero - 0.7346.

Likewise, the zero in a number such as 763.0 can be displayed by connecting the RBI of the 4033AB associated with it to a "high-level" voltage.

A "high" Lamp Test signal turns on all outputs.

CONNECTION DIAGRAM
(all packages)



[1] 4026AB
[2] 4033AB

Add suffix for package:

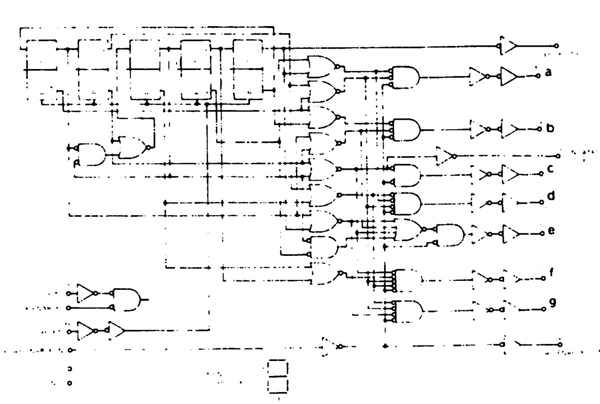
C	16-pin Cerdip
D	16-pin Ceramic
E	16-pin Epoxy
F	16-pin Flat
H	Chip

RECOMMENDED OPERATING CONDITIONS

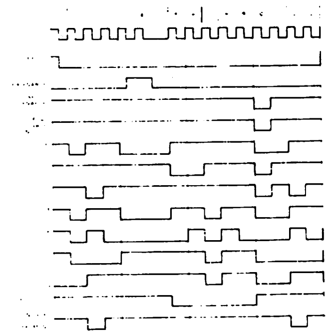
For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

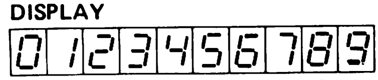
LOGIC DIAGRAM



TIMING DIAGRAM



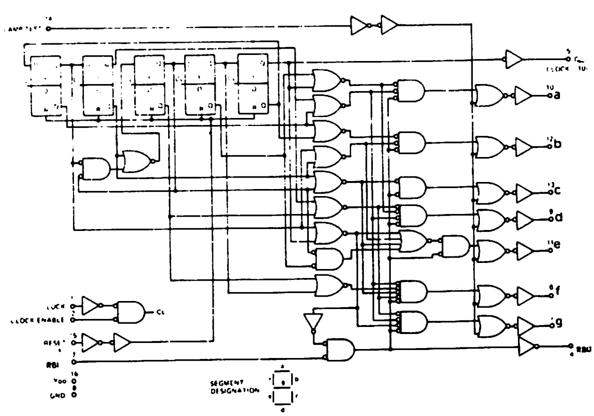
DISPLAY



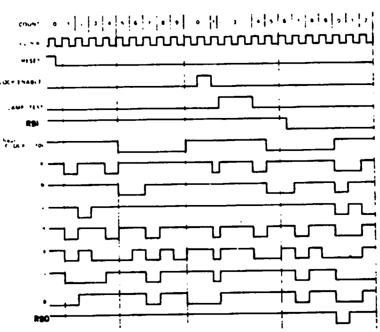
0 1 2 3 4 5 6 7 8 9

4026AB Decade Counter/7-Segment Decoder with Display Enable

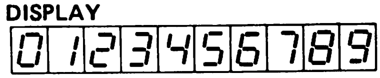
LOGIC DIAGRAM



TIMING DIAGRAM



DISPLAY



0 1 2 3 4 5 6 7 8 9

4033AB Decade Counter/7-Segment Decoder with Ripple Blanking

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[2]		+25°C			T_{HIGH}[2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN}=V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	μAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		15	combinations	–	20	–	0.2	20	–	600	
OUTPUT HIGH (SOURCE) CURRENT	I_{OH}										
Decoded outputs		5	$V_{OH}=4.6V$	-0.175	–	-0.14	-0.28	–	-0.10	–	mAdc
		10	$V_{OH}=9.5V$	-0.375	–	-0.3	-0.6	–	-0.21	–	
		15	$V_{OH}=13.5V$	-1.25	–	-1.0	-2.5	–	-0.7	–	
			$V_{IN}=V_{SS}$ or V_{DD}								
Carry output		5	$V_{OH}=4.6V$	-0.19	–	-0.15	-0.4	–	-0.11	–	mAdc
		10	$V_{OH}=9.5V$	-0.43	–	-0.35	-1.0	–	-0.25	–	
		15	$V_{OH}=13.5V$	-1.57	–	-1.25	-4.0	–	-0.88	–	
			$V_{IN}=V_{SS}$ or V_{DD}								
Remaining Outputs		5	$V_{OH}=4.6V$	-0.10	–	-0.08	-0.2	–	-0.056	–	mAdc
		10	$V_{OH}=9.5V$	-0.25	–	-0.20	-0.5	–	-0.14	–	
		15	$V_{OH}=13.5V$	-0.75	–	-0.60	-1.5	–	-0.42	–	
			$V_{IN}=V_{SS}$ or V_{DD}								
OUTPUT LOW (SINK) CURRENT	I_{OL}										
All Outputs Except Carry		5	$V_{OL}=0.4V$	0.125	–	0.1	0.3	–	0.07	–	mAdc
		10	$V_{OL}=0.5V$	0.31	–	0.25	0.6	–	0.175	–	
		15	$V_{OL}=1.5V$	1.44	–	1.15	2.5	–	0.81	–	
			$V_{IN}=V_{SS}$ or V_{DD}								
Carry output		5	$V_{OL}=0.4V$	0.19	–	0.15	0.4	–	0.11	–	mAdc
		10	$V_{OL}=0.5V$	0.45	–	0.35	1.0	–	0.25	–	
		15	$V_{OL}=1.5V$	1.57	–	1.25	4.0	–	0.88	–	
			$V_{IN}=V_{SS}$ or V_{DD}								

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

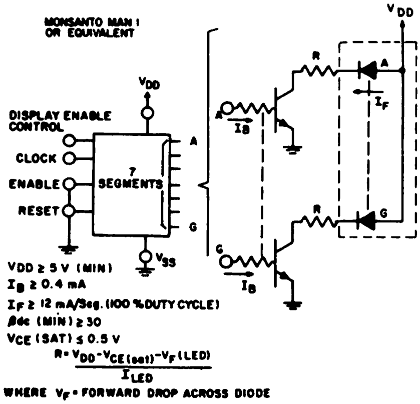
ELECTRICAL CHARACTERISTICS (Continued)

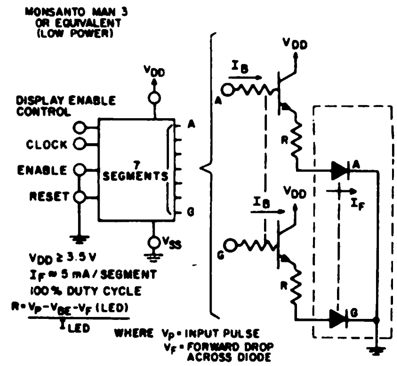
DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

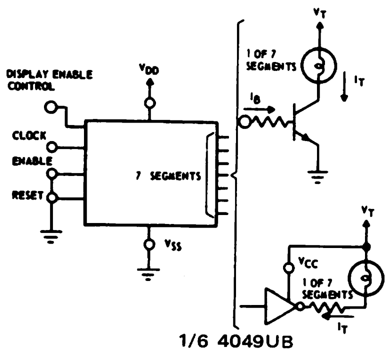
PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME Clock to Decoded Outputs	t_{PLH}, t_{PHL}	5	–	500	1000	ns
		10	–	225	450	
		15	–	175	350	
Clock to Carry Out	t_{PLH}, t_{PHL}	5	–	450	900	ns
		10	–	125	250	
		15	–	100	200	
OUTPUT TRANSITION TIME Decoded Outputs	t_{TLH}, t_{THL}	5	–	250	500	ns
		10	–	125	250	
		15	–	100	200	
Carry Output	t_{TLH}, t_{THL}	5	–	200	400	ns
		10	–	100	200	
		15	–	80	160	
MINIMUM CLOCK OR ENABLE PULSE WIDTH	PW_{CL}, PW_{CE}	5	–	200	400	ns
		10	–	100	200	
		15	–	80	160	
MAXIMUM CLOCK FREQUENCY	f_{CL}	5	1.25	2.5	–	MHz
		10	2.5	5.0	–	
		15	3.0	6.0	–	
MAXIMUM CLOCK OR ENABLE RISE AND FALL TIME	t_{rCL}, t_{fCL}	5	15	–	–	µs
		10	15	–	–	
		15	3	–	–	
MINIMUM CLOCK OR ENABLE SETUP TIME	t_{setup}	5	–	250	500	ns
		10	–	100	200	
		15	–	80	160	
RESET OPERATION						
PROPAGATION DELAY TIME Reset to Decoded Outputs	t_{PLH}, t_{PHL}	5	–	700	1400	ns
		10	–	250	500	
		15	–	200	400	
Reset to Carry Output	t_{PLH}, t_{PHL}	5	–	500	1000	ns
		10	–	125	250	
		15	–	100	200	
MINIMUM RESET PULSE WIDTH	PW_R	5	–	200	400	ns
		10	–	100	200	
		15	–	80	160	
RESET REMOVAL TIME	t_{rem}	5	–	375	750	ns
		10	–	150	300	
		15	–	125	250	

DISPLAY INTERFACE

LIGHT EMITTING DIODE DISPLAYS







LOW-POWER INCANDESCENT READOUTS

ASSUMED
TRANSISTOR
CHARACTERISTICS

β_{dc} (min.) ≥ 30
$V_{CE(sat.)} \leq 0.50$ V

@ $V_{DD} \geq 3.5$ V (min.)
$I_B \geq 0.25$ mA (min.)
$I_T \leq 7.5$ mA (min.)

4049UB

@ $V_{DD} = 10$ V (min.)
V_o "0" ≤ 0.6 V
$I_T = 8$ mA (min.)

@ $V_{DD} = 6$ V (min.)
V_o "0" ≤ 1.0 V
$I_T = 5$ mA (min.)

$V_T \approx 1.5$ V TO 3.5 V

INCANDESCENT READOUTS

ASSUMED
TRANSISTOR
CHARACTERISTICS

β_{dc} (min.) ≥ 25
$V_{CE(sat.)} \leq 0.50$ V

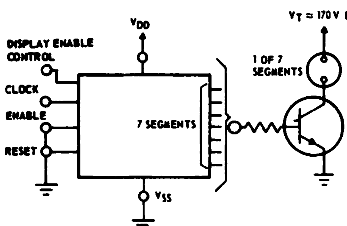
@ $V_{DD} = 8$ V (min.)
$I_B = 1.0$ mA (min.)
$I_T = 24$ mA (min.)

4049UB

@ $V_{DD} = 10$ V (min.)
V_o "0" ≤ 2 V
$I_T = 20$ mA (min.)

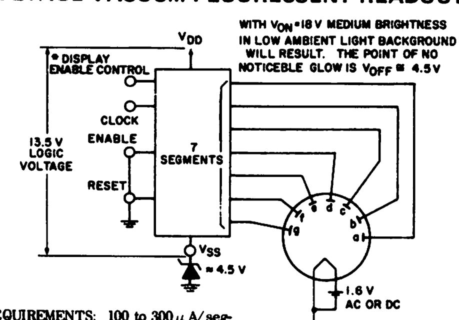
$V_T \approx 3.5$ V TO 6 V

NEON READOUTS



TRANSISTOR CHARACTERISTICS
Leakage with transistor cutoff ≤ 0.05 mA
$V_{(BR)CER}$ ··· $> V_T$
β_{dc}(min) ≥ 30

LOW-VOLTAGE VACUUM FLUORESCENT READOUTS



TUBE REQUIREMENTS: 100 to 300 μA/segment at tube voltages of 12 V to 25 V depending on required brightness. Filament requirement 45 mA at 1.6 V, AC or DC.

CMOS DUAL J-K FLIP-FLOP

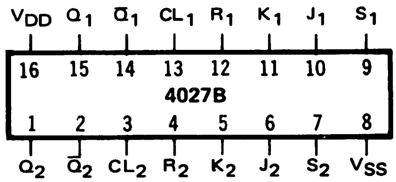
FEATURES

- Individual Set and Reset Controls
- Fully Static Operation
- Logic Edge-Clocked Design
- 8MHz Toggle Rate @ 10Vdc

DESCRIPTION

The 4027B consists of two identical independent CMOS J-K master-slave Flip-Flops. The 4027B is useful in performing control, register, and toggle functions. Logic levels present at the J and K inputs along with internal self-steering control the state of each flip-flop; changes in the flip-flop state are synchronous with the positive-going transition of the Clock pulse. Set and Reset functions are independent of the Clock and are initiated when a high level signal is present at either the Set or Reset input.

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

C	16-pin Cerdip	F	16-pin Flat
D	16-pin Ceramic	H	Chip
E	16-pin Epoxy		

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

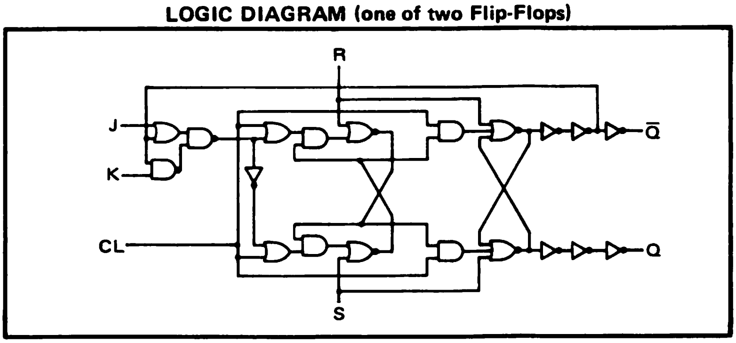
DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

TRUTH TABLE

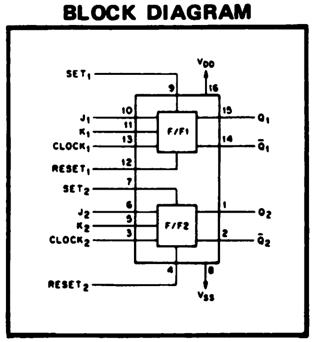
●t_{n-1} INPUTS						†t_n OUTPUTS	
CL▲	J	K	S	R	Q	Q	Q̄
↑	1	X	0	0	0	1	0
↑	X	0	0	0	1	1	0
↑	0	X	0	0	0	0	1
↑	X	1	0	0	1	0	1
↓	X	X	0	0	X	(No Change)	
X	X	X	1	0	X	1	0
X	X	X	0	1	X	0	1
X	X	X	1	1	X	1	1

WHERE 1 = HIGH LEVEL
0 = LOW LEVEL
▲ - LEVEL CHANGE
X - DON'T CARE
● - t_{n-1} REFERS TO THE INTERVAL PRIOR TO THE POSITIVE CLOCK PULSE TRANSITION
† - t_n REFERS TO THE TIME INTERVAL AFTER THE POSITIVE CLOCK PULSE TRANSITION

LOGIC DIAGRAM (one of two Flip-Flops)



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS [1]

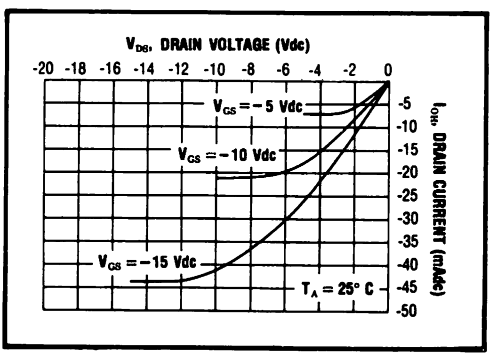
PARAMETER		VDD (Vdc)	CONDITIONS	TLOW[2] Min.	TLOW[2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	THIGH[2] Min.	THIGH[2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN}=V_{SS}$ or V_{DD}	–	1.0	–	0.005	1.0	–	30	μAdc
		10	All valid input	–	2.0	–	0.01	2.0	–	60	
		15	combinations	–	4.0	–	0.02	4.0	–	120	

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

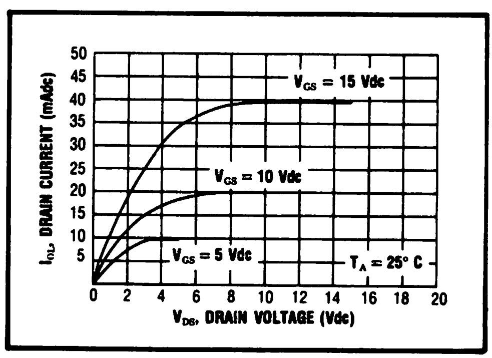
DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		VDD (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}	5	–	150	300	ns
		10	–	65	130	
		15	–	50	100	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
MINIMUM CLOCK PULSE WIDTH	PW_{CL}	5	–	165	330	ns
		10	–	60	120	
		15	–	50	100	
MAXIMUM CLOCK FREQUENCY	f_{CL}	5	1.5	3.0	–	MHz
		10	4.0	8.0	–	
		15	5.0	10		
MAXIMUM CLOCK RISE AND FALL TIME[1]	t_{rCL}, t_{fCL}	5	15	–	–	μs
		10	5	–	–	
		15	3	–	–	
MINIMUM SETUP TIME	t_{setup}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
MINIMUM HOLD TIME	t_{hold}	5	–	-25	0	ns
		10	–	-10	0	
		15	–	-5	0	
SET AND RESET OPERATION						
PROPAGATION DELAY TIME S to Q, R to $\overline{Q}$	t_{PLH}	5	–	150	300	ns
		10	–	65	130	
		15	–	50	100	
MINIMUM SET AND RESET PULSE WIDTH	PW_S, PW_R	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
SET AND RESET REMOVAL TIME	t_{rem}	5	–	0	25	ns
		10	–	0	10	
		15	–	0	5	

[1] When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.



Typical P-Channel Source Current Characteristics



Typical N-Channel Sink Current Characteristics

CMOS BCD-TO-DECIMAL DECODER

FEATURES

- BCD-to-Decimal or Binary-to-Octal Decoding
- Buffered Outputs go High on Selection
- Low Outputs for all Illegal Input Combinations

DESCRIPTION

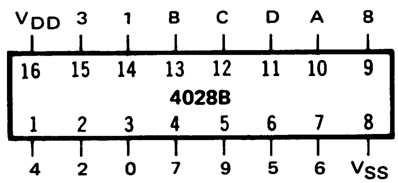
The 4028B types are BCD-to-Decimal or Binary-to-Octal Decoders consisting of pulse shaping circuits on all 4 inputs, decoding/logic gates, and 10 output buffers. A BCD code applied to the four inputs, A to D, results in a high level at the selected one of 10 decimal decoded outputs. Similarly, a 3-bit binary code applied to inputs A through C is decoded in octal code at output 0 to 7. A high-level signal at the D input inhibits octal decoding and causes outputs 0 through 7 to go low. If unused, the D input must be connected to V_{SS}.

Expanded decoding such as binary-to-hexadecimal (1-of-16), etc., can be achieved by using other 4028B devices. This part is useful for code conversion, address decoding, memory selection control, demultiplexing, and readout decoding.

TRUTH TABLE

Input				Output									
D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	0	0	0	0	0	1	0
0	0	1	0	0	0	0	0	0	0	0	1	0	0
0	0	1	1	0	0	0	0	0	0	1	0	0	0
0	1	0	0	0	0	0	0	0	1	0	0	0	0
0	1	0	1	0	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	0	1	0	0	0	0	0	0
0	1	1	1	0	0	1	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	1	1	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

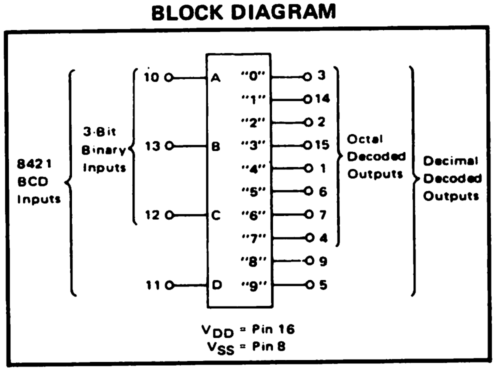
- C 16-pin Cerdip
- D 16-pin Ceramic
- E 16-pin Epoxy
- F 16-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

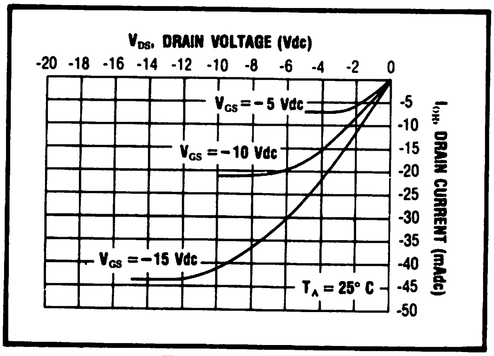
STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[2] Min.	T_{LOW}[2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH}[2] Min.	T_{HIGH}[2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5 10 15	$V_{IN}=V_{SS}$ or V_{DD} All valid input combinations	– – –	5 10 20	— — —	0.05 0.1 0.2	5 10 20	– – –	150 300 600	μAdc

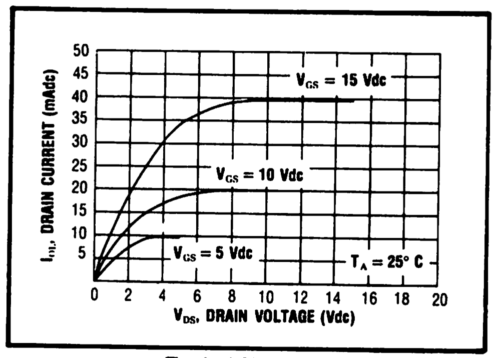
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}	5 10 15	– – –	150 60 50	300 120 100	ns
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5 10 15	– – –	90 50 40	180 100 80	ns

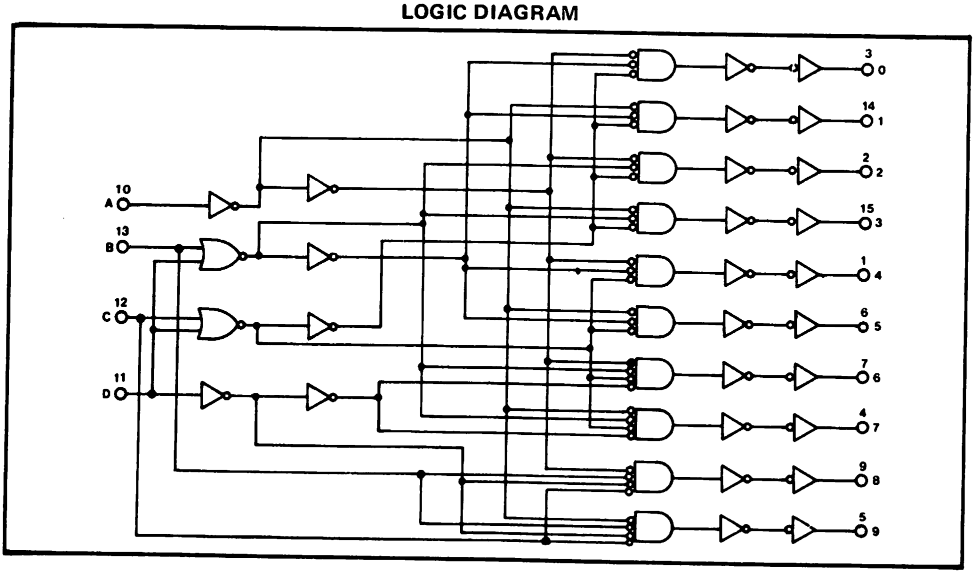


Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

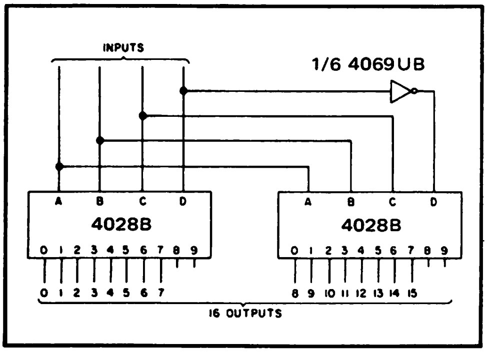
LOGIC DIAGRAM



APPLICATIONS INFORMATION

CODE CONVERSION CIRCUIT

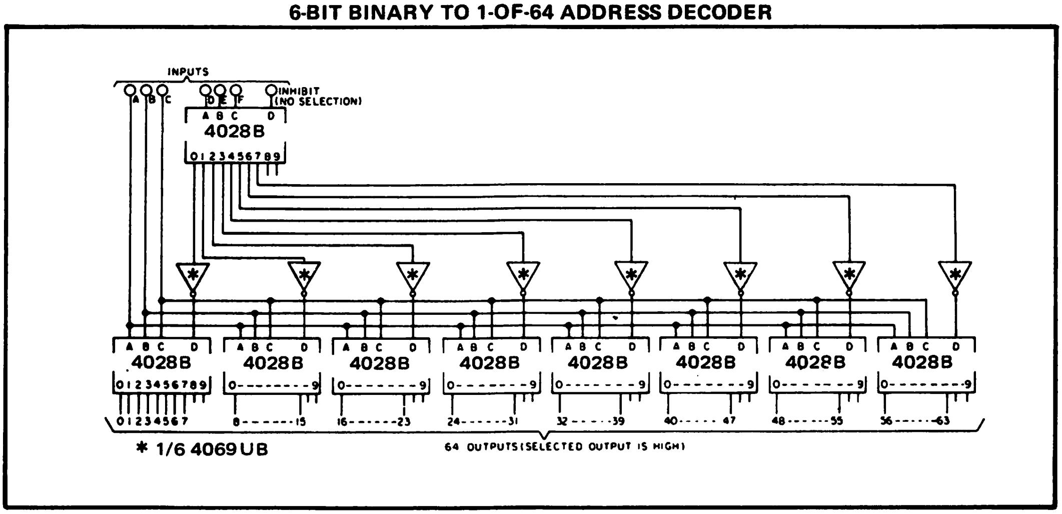
The circuit shown here converts any 4-bit code to a decimal or hexadecimal code. The table shows a number of codes and the decimal or hexadecimal number in these codes which must be applied to the input terminals of the 4028B to select a particular output. For example: in order to get a "high" on output No. 8 the input must be either an 8 expressed in 4-Bit Binary code, a 15 expressed in 4-Bit Gray code, or a 5 expressed in Excess-3 code.



INPUTS				INPUT CODES: Hexa Decimal		INPUT CODES: Decimal				OUTPUT NUMBER															
				4-BIT BINARY	4-BIT GRAY	EXCESS-3	EXCESS-3 GRAY	AIKEN	4-2-2-1																
D	C	B	A							0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0			0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	1			1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	2	3		0	2	2	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	3	2	0	3	3		0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	4	7	1	4	4		0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	1	0	1	5	6	2			3	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
0	1	1	0	6	4	3	1		4	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	1	1	1	7	5	4	2			0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	0	8	15	5				0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	9	14	6			5	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
1	0	1	0	10	12	7	9		6	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
1	0	1	1	11	13	8		5		0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
1	1	0	0	12	8	9	5	6		0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
1	1	0	1	13	9		6	7	7	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
1	1	1	0	14	11		8	8	8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
1	1	1	1	15	10		7	9	9	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Code Conversion Chart

6-BIT BINARY TO 1-OF-64 ADDRESS DECODER



CMOS PRESETTABLE UP/DOWN COUNTER

FEATURES

- Binary or Decade Up/Down Counting
- BCD Outputs in Decade Mode
- Asynchronous Preset Enable
- Internally Synchronous for High Speed
- Logic Edge-Clocked Design
- 6MHz Counting Rate @ 10Vdc
- Carry Output for Cascading Stages

DESCRIPTION

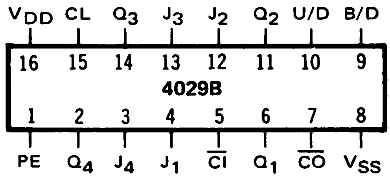
The 4029B consists of a four-stage Binary or BCD Decade Up/Down Counter with provisions for look-ahead carry in both counting modes. The inputs consist of a single Clock, Carry-in (Clock Enable), Binary/Decade, Up/Down, Preset Enable, and four individual Jam signals. Four separate buffered Q signals and a Carry-out signal are provided as outputs.

A high Preset Enable signal allows information on the Jam inputs to preset the counter to any state asynchronously with the Clock. A low on each Jam line, when the Preset/Enable signal is high, resets the counter to its zero count. The counter is advanced one count at the positive transition of the Clock when the Carry-in and Preset Enable signals are low. Advancement is inhibited when the Carry-in or Preset Enable signals are high. The Carry-out signal is normally high and goes low when the counter reaches its maximum count in the Up mode or the minimum count in the Down mode provided the Carry-in signal is low. The Carry-in signal in the low state can thus be considered a "Clock Enable". The Carry-in terminal must be connected to V_{SS} when not in use.

Binary counting is accomplished when the Binary/Decade input is high; the counter counts in the Decade mode when the Binary/Decade input is low. The counter counts up when the Up/Down input is high, and Down when the Up/Down input is low. Multiple packages can be connected in either a parallel-clocking or a ripple-clocking arrangement. Parallel-clocking provides synchronous control and hence faster response from all counting outputs. Ripple-clocking allows for longer clock input rise and fall times.

This counter finds primary use in up/down and difference counting and programmable frequency synthesizer applications. It is also useful in A/D and D/A conversion techniques and for magnitude and sign generation.

CONNECTION DIAGRAM
(all packages)



RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

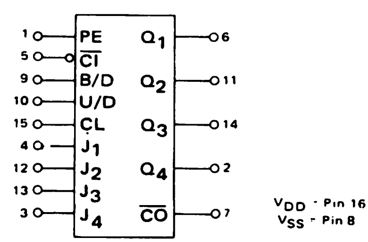
DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

TRUTH TABLE

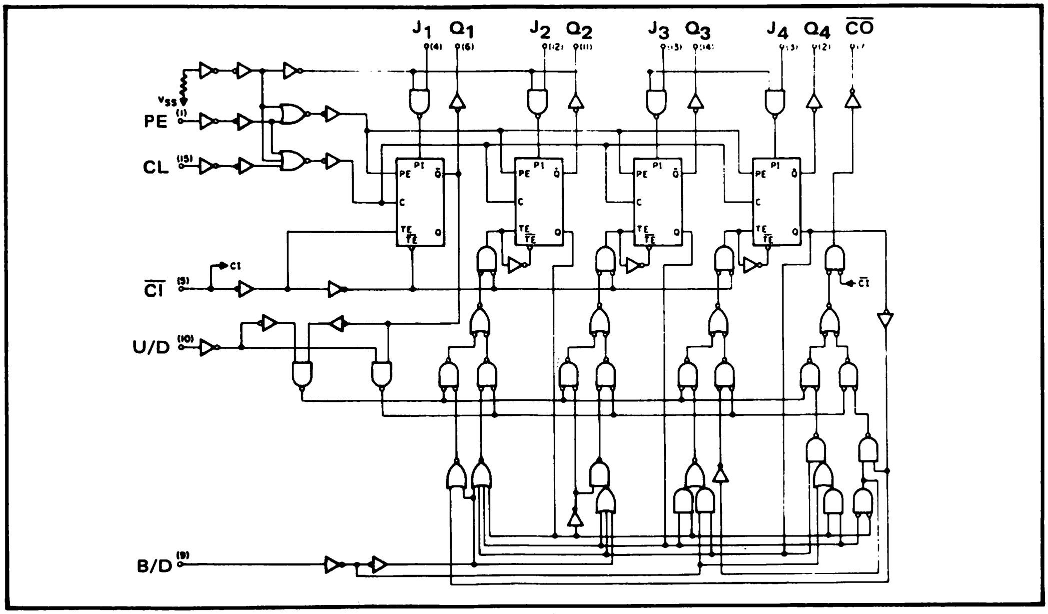
$\overline{CI}$	U/D	PE	B/D	Action
1	X	0	X	No Count
0	1	0	0	Count Up (Decade)
0	1	0	1	Count Up (Binary)
0	0	0	0	Count Down (Decade)
0	0	0	1	Count Down (Binary)
X	X	1	X	Preset

X = Don't Care

BLOCK DIAGRAM

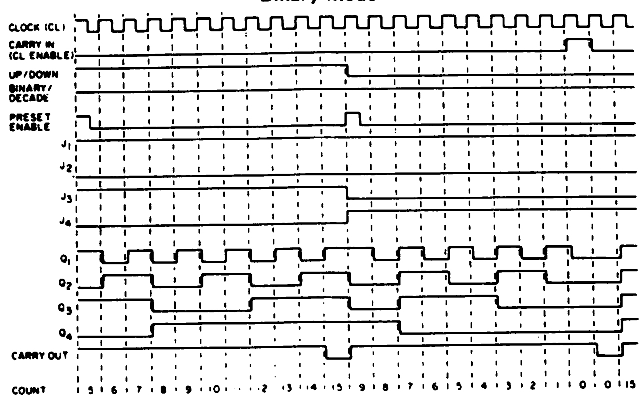


LOGIC DIAGRAM

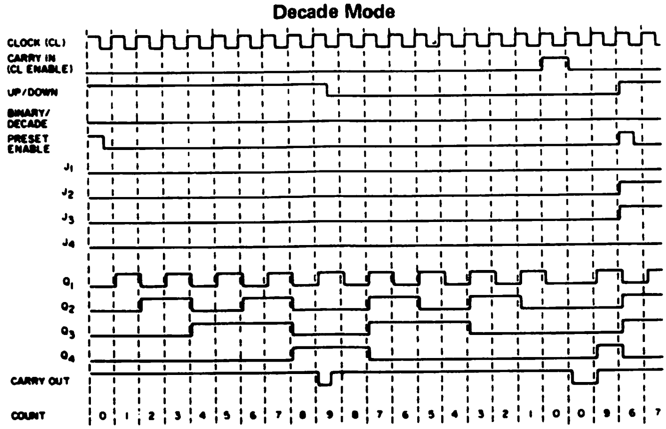


TIMING DIAGRAMS

Binary Mode



Decade Mode



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS [1]

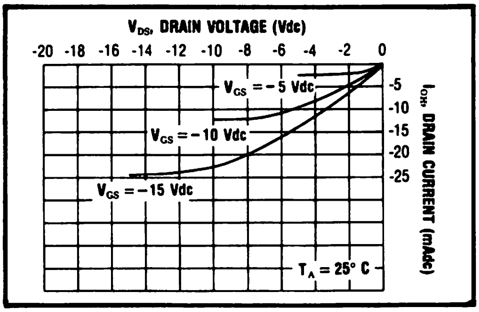
PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[2] Min.	T_{LOW}[2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH}[2] Min.	T_{HIGH}[2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN}=V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	μAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		15	combinations	–	20	–	0.2	20	–	600	

NOTES: [1] Remaining Static Characteristics are listed under "4000B Series Family Specifications"
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

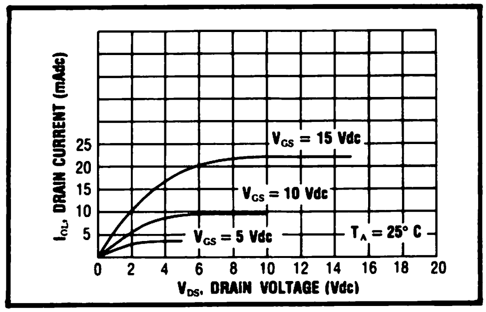
DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME Clock to Q	t_{PLH}, t_{PHL}	5	–	250	500	ns
		10	–	120	240	
		15	–	90	180	
Clock to $\overline{\text{Carry Out}}$		5	–	280	560	ns
		10	–	130	260	
		15	–	95	190	
$\overline{\text{Carry In}}$ to $\overline{\text{Carry Out}}$		5	–	170	340	ns
		10	–	70	140	
		15	–	50	100	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
MINIMUM CLOCK PULSE WIDTH	PW_{CL}	5	–	170	340	ns
		10	–	85	170	
		15	–	70	140	
MAXIMUM CLOCK FREQUENCY	f_{CL}	5	2.0	4	–	MHz
		10	4.0	8	–	
		15	5.5	11	–	
MAXIMUM CLOCK RISE AND FALL TIME [1]	t_{rCL}, t_{fCL}	5	15	–	–	μs
		10	15	–	–	
		15	15	–	–	
MINIMUM SETUP TIME Carry In	t_{setup}	5	–	150	300	ns
		10	–	65	130	
		15	–	50	100	
Up/Down, B/D		5	–	325	650	ns
		10	–	115	230	
		15	–	85	170	
PRESET OPERATION						
PROPAGATION DELAY TIME Preset Enable to Q	t_{PLH}, t_{PHL}	5	–	360	720	ns
		10	–	140	280	
		15	–	110	220	
Preset Enable to $\overline{\text{Carry Out}}$		5	–	410	820	ns
		10	–	165	330	
		15	–	130	260	
MINIMUM PRESET ENABLE PULSE WIDTH	PW_{PE}	5	–	170	340	ns
		10	–	85	170	
		15	–	70	140	
PRESET ENABLE REMOVAL TIME	t_{rem}	5	–	325	650	ns
		10	–	110	220	
		15	–	90	180	

[1] When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.



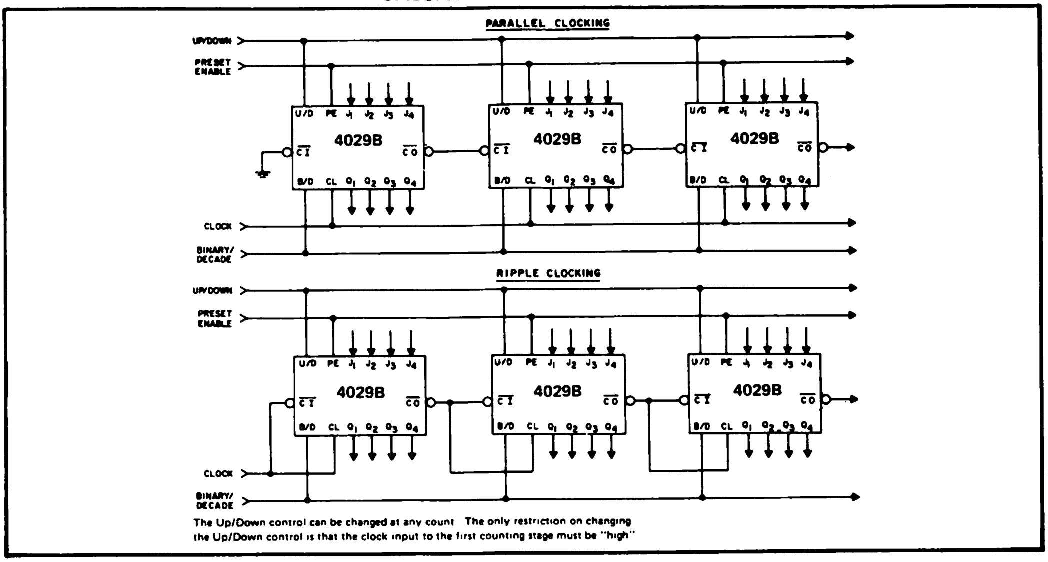
Typical P-Channel
Source Current Characteristics



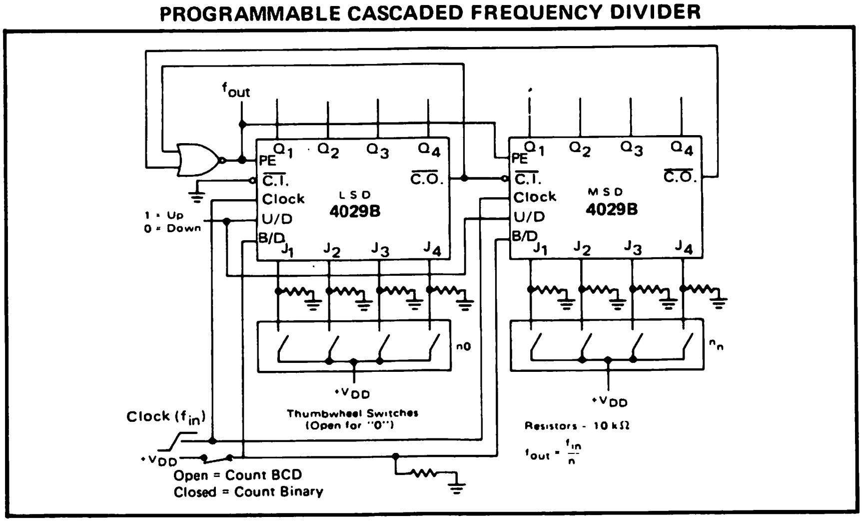
Typical N-Channel
Sink Current Characteristics

APPLICATIONS INFORMATION

CASCADING CONNECTIONS



PROGRAMMABLE CASCADED FREQUENCY DIVIDER



CMOS QUAD EXCLUSIVE-OR GATE

FEATURES

- Buffered Outputs
- Diode Protection on all Inputs
- Fully "B"-Series Compatible
- Pin Compatible with 4070 types, MC14507, 74C86

DESCRIPTION

The 4030B contains four independent exclusive-OR gates integrated on a single monolithic silicon chip. Each exclusive-OR gate consists of five N-Channel and five P-Channel enhancement-mode transistors, plus output buffering devices.

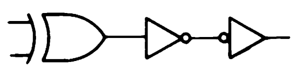
TRUTH TABLE
(one of four gates)

A	B	Y
0	0	0
1	0	1
0	1	1
1	1	0

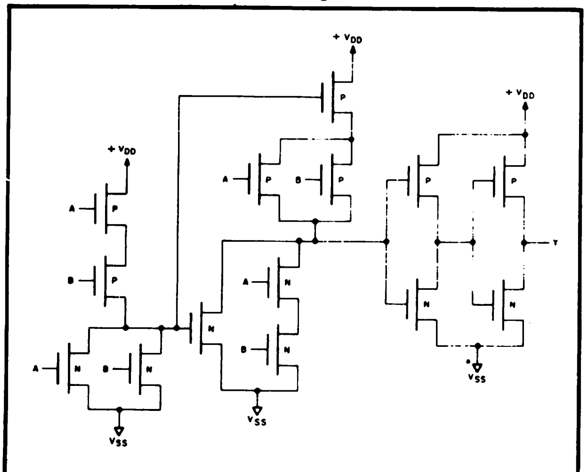
Where 1 = High Level
0 = Low Level

LOGIC DIAGRAM

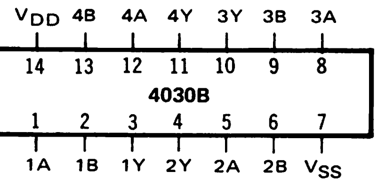
4030B



SCHEMATIC DIAGRAM
(one of four gates)



CONNECTION DIAGRAM
(all packages)



Add suffix for package:

C 14-pin Cerdip
D 14-pin Ceramic
E 14-pin Epoxy
F 14-pin Flat
H Chip

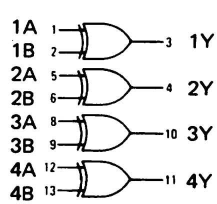
RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

Note: The 4030B is identical to the 4070B; the devices are fully interchangeable in all applications.

FUNCTION DIAGRAM



$Y = A \oplus B$

V_{DD} = Pin 14
V_{SS} = Pin 7

ELECTRICAL CHARACTERISTICS

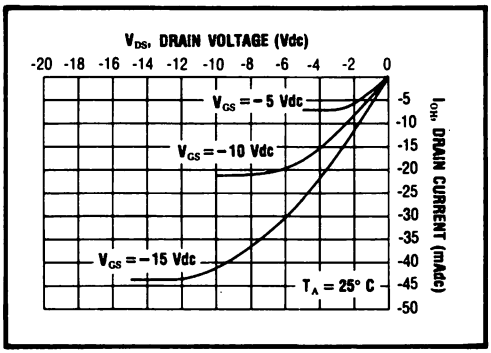
STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[2] Min.	T_{LOW}[2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH}[2] Min.	T_{HIGH}[2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN}=V_{SS}$ or V_{DD}	–	0.05	–	0.0005	0.05	–	1.5	μAdc
		10	All valid input	–	0.10	–	0.001	0.10	–	3.0	
		15	combinations	–	0.20	–	0.002	0.20	–	6.0	

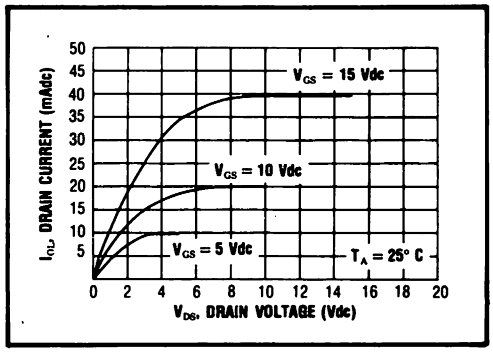
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}	5	–	140	280	ns
		10	–	65	130	
		15	–	50	100	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	

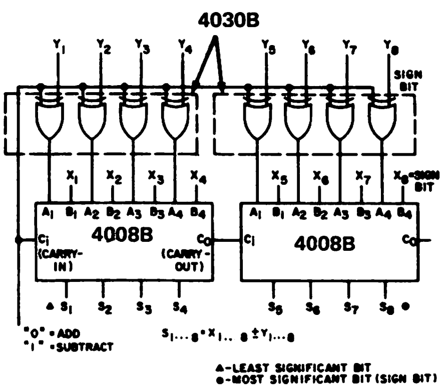


Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

APPLICATIONS INFORMATION
8-BIT TWO'S COMPLEMENT ADDER/SUBTRACTOR



X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1		X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	
0	0	0	0	0	0	0	0	= 0	1	1	1	1	1	1	1	1	= −1
0	0	0	0	0	0	0	1	= 1	1	1	1	1	1	1	1	0	= −2
0	0	0	0	0	0	1	0	= 2	1	1	1	1	1	1	0	1	= −3
0	0	0	0	0	0	1	1	= 3	1	1	1	1	1	1	0	0	= −4
.	.	.	.	.	.	.	.	.	1	1	1	1	1	0	1	1	= −5
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
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0	1	1	1	1	1	1	0	= 126	1	0	0	0	0	0	0	1	= −127
0	1	1	1	1	1	1	1	= 127	1	0	0	0	0	0	0	0	= −128

Two's complement numbers and their equivalent decimal values.

SOLID STATE SCIENTIFIC

SCL4034B

CMOS 8-BIT UNIVERSAL BUS REGISTER

FEATURES

- Bidirectional Parallel Data Inputs
- Parallel or Serial Inputs/Parallel Outputs
- Asynchronous or Synchronous Parallel Data Loading
- Data Recirculation for Register Storage
- Parallel Enable on Data Lines for Bus Connection
- Static Operation - DC to 5MHz @ 10Vdc

DESCRIPTION

The 4034 B is a Static Eight-Stage Parallel- or Serial-Input/Parallel-Output Register. It can be used to:

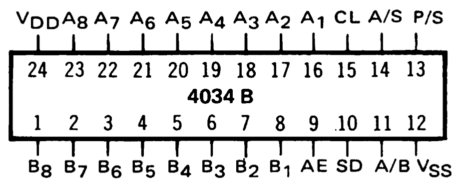
1. bidirectionally transfer parallel information between two buses,
2. convert serial data to parallel form and direct the parallel data to either of two buses,
3. store (recirculate) parallel data, or
4. accept parallel data from either of two buses and convert that data to serial form.

Inputs that control the operations include a single phase Clock (CL), "A" Data Enable (AE), Asynchronous/Synchronous (A/S), "A" bus to "B" bus/"B" bus to "A" bus (A/B), and Parallel/Serial (P/S). Data inputs include 16 bidirectional Parallel Data lines of which the eight "A" Data lines are inputs (outputs) and the "B" Data lines are outputs (inputs) depending on the signal level on the A/B input. In addition, an input for Serial data is also provided.

All register stages are D-type master/slave flip-flops with separate master and slave clock inputs generated internally to allow synchronous or asynchronous data transfer from master to slave. Isolation from external noise and the effects of loading is provided by output buffering.

Useful applications for this device include pseudo-random code generation, sample-and-hold register, frequency and phase comparators, address or buffer register, and serial/parallel input/output conversion.

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

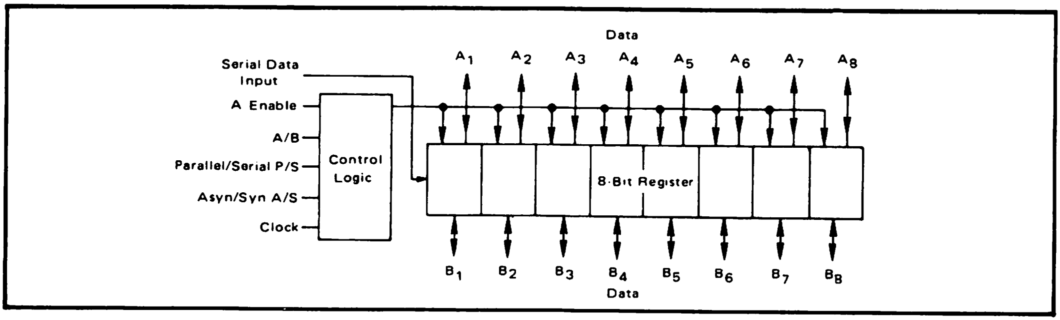
D 24-pin Ceramic
E 24-pin Epoxy
H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
D, H Device		-55 to +125	°C
E Device		-40 to +85	°C

BLOCK DIAGRAM



OPERATING INFORMATION

The 4034 B is composed of eight register cells connected in cascade with additional control logic. Each register cell is composed of one "D' master-slave flip-flop with separate internal clocks, and two data transfer gates allowing the data to be transferred bidirectionally from bus A to bus B and from bus B to bus A, and to be memorized. Besides the single phase clock and the serial data inputs, the control logic provides four other features:

A Enable Input — When high, this input enables the bus A data lines.

A/B Input (Data A or B) — This input controls the direction of data flow: when high, the data flows from bus A to bus B; when low, the data flows from bus B to bus A.

P/S Input (Parallel/Serial) — This input controls the data input mode (Parallel or Serial). When high, the data is transferred to the register in a parallel asynchronous mode or a parallel synchronous mode (positive clock transition). When low, the data is entered into the register in a serial synchronous mode (positive clock transition).

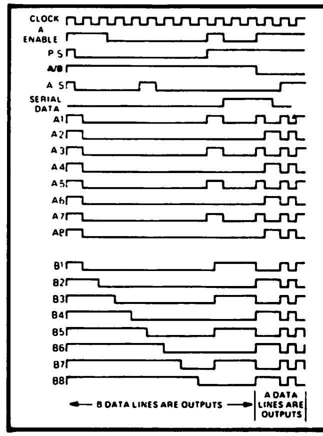
A/S Input (Asynchronous/Synchronous to the Clock) — When this input is high, the data is transferred independently from the clock rate; when low, the clock is enabled and the data is transferred synchronously.

Truth Table for Register Input-Levels and the Resulting Operation (L = Low Level, H = High, X = Don't Care)

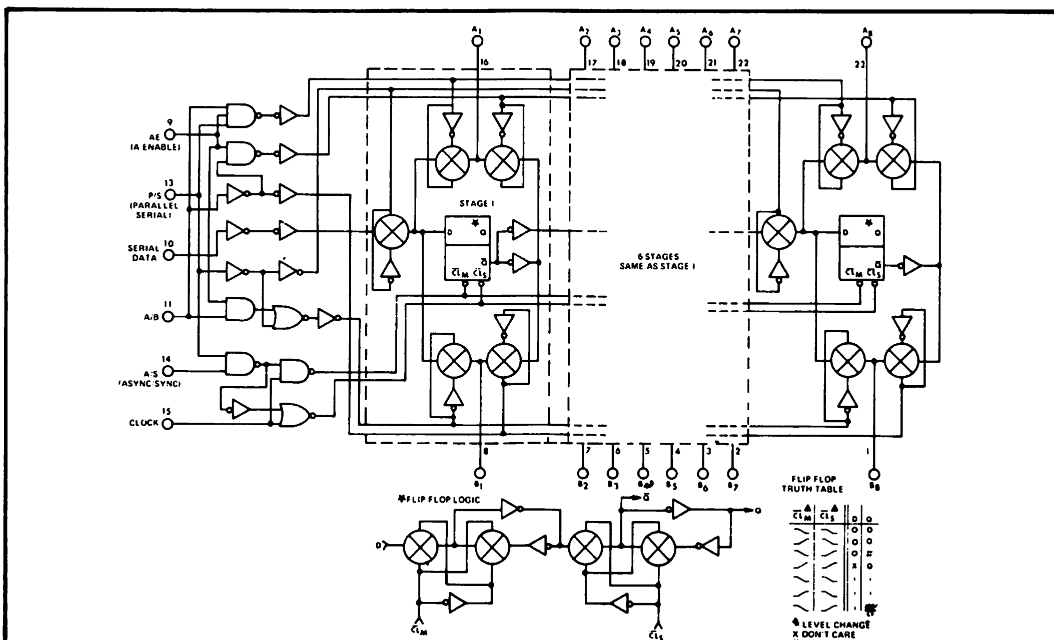
"A" Enable	P/S	A/B	A/S	Operation*
L	L	L	X	Serial Mode; Synch. Serial Data Input, "A" Parallel Data Outputs Disabled
L	L	H	X	Serial Mode; Synch. Serial Data Input, "B" Parallel Data Output
L	H	L	L	Parallel Mode; "B" Synch. Parallel Data Inputs, "A" Parallel Data Outputs Disabled
L	H	L	H	Parallel Mode; "B" Asynch. Parallel Data Inputs, "A" Parallel Data Outputs Disabled
L	H	H	L	Parallel Mode; "A" Parallel Data Inputs Disabled, "B" Parallel Data Outputs, Synch Data Recirculation
L	H	H	H	Parallel Mode; "A" Parallel Data Inputs Disabled, "B" Parallel Data Outputs, Asynch Data Recirculation
H	L	L	X	Serial Mode; Synch. Serial Data Input, "A" Parallel Data Output
H	L	H	X	Serial Mode; Synch. Serial Data Input, "B" Parallel Data Output
H	H	L	L	Parallel Mode; "B" Synch. Parallel Data Input, "A" Parallel Data Output
H	H	L	H	Parallel Mode; "B" Asynch. Parallel Data Input, "A" Parallel Data Output
H	H	H	L	Parallel Mode; "A" Synch. Parallel Data Input, "B" Parallel Data Output
H	H	H	H	Parallel Mode; "A" Asynch. Parallel Data Input, "B" Parallel Data Output

* Outputs change at positive transition of clock in the serial mode and when the A/S control input is "low" in the parallel mode.

TIMING DIAGRAM



LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS[1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[2]		+25°C			T_{HIGH}[2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5 10 15	$V_{IN}=V_{SS}$ or V_{DD} All valid inputs combinations	– – –	5 10 20	– – –	0.05 0.1 0.2	5 10 20	– – –	150 300 600	μAdc
3-STATE OUTPUT LEAKAGE CURRENT	I_{ZL}	15		–	±0.1	–	$\pm10^{-4}$	±0.1	–	±1.0	μAdc

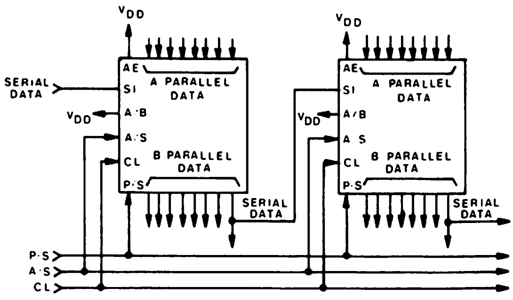
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for D, H device.
= -40°C for E device.
T_{HIGH} = +125°C for D, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

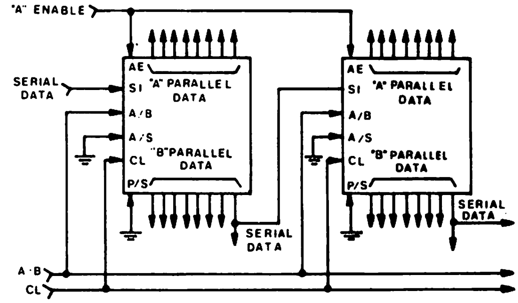
PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}	5 10 15	– – –	350 120 100	700 240 200	ns
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5 10 15	– – –	180 90 70	360 180 140	ns
MINIMUM CLOCK PULSE WIDTH	PW_{CL}	5 10 15	– – –	125 50 40	250 100 80	ns
MAXIMUM CLOCK FREQUENCY	f_{CL}	5 10 15	2 4 6	4 8 12	– – –	MHz
MAXIMUM CLOCK RISE AND FALL TIME[1]	t_{rCL}, t_{fCL}	5 10 15	15 15 15	– – –	– – –	μs
MINIMUM HIGH-LEVEL PULSE WIDTH AE, P/S, A/S Inputs	PW_{AE}, $PW_{P/S}$, $PW_{A/S}$	5 10 15	– – –	180 90 70	360 180 140	ns
MINIMUM SETUP TIME A, B; Serial Inputs	t_{setup}	5 10 15	– – –	140 70 50	280 140 100	ns

[1] When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.

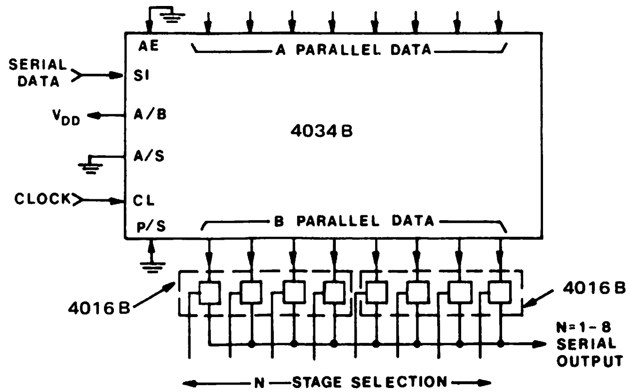
APPLICATIONS INFORMATION



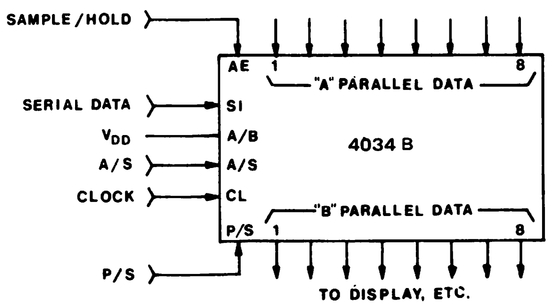
16-Bit parallel in/parallel out, parallel in/serial out, serial in/parallel out, serial in/serial out register.



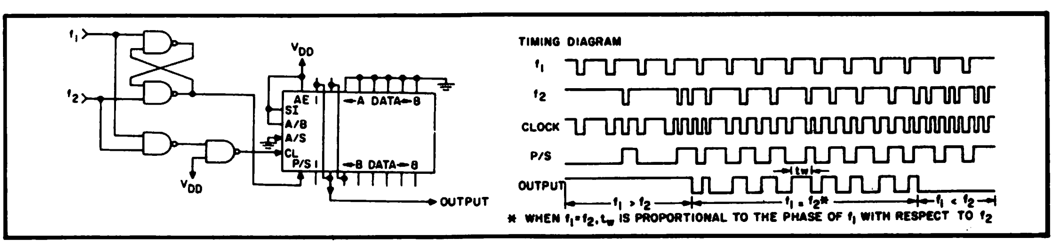
16-Bit Serial in/gated parallel out register



N-stage shift register with fixed serial output line.

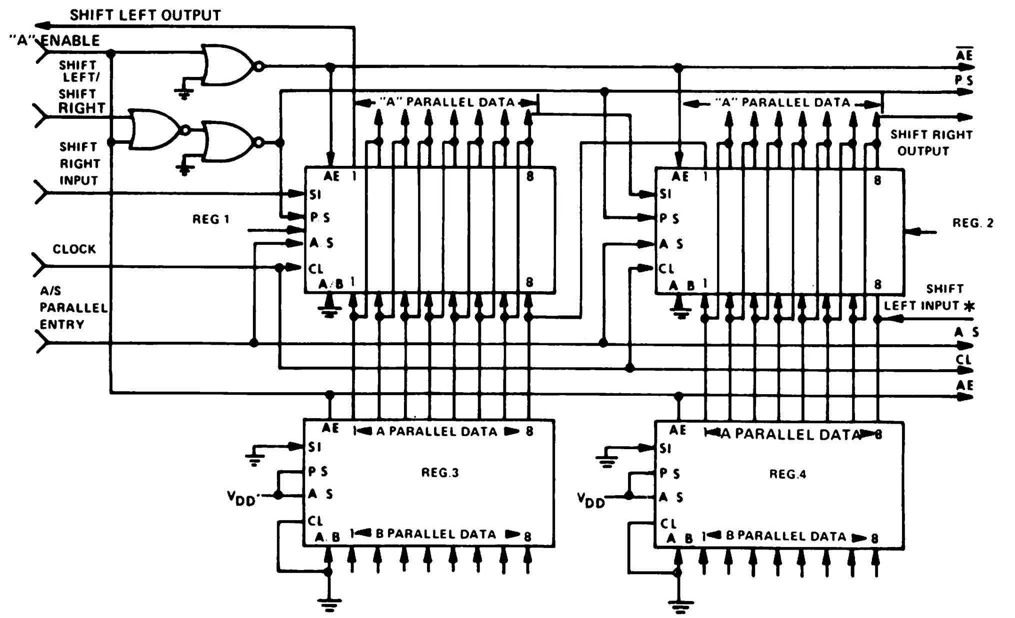


Sample and hold register — serial/parallel in parallel out.



Frequency and phase comparator

APPLICATIONS INFORMATION (Continued)

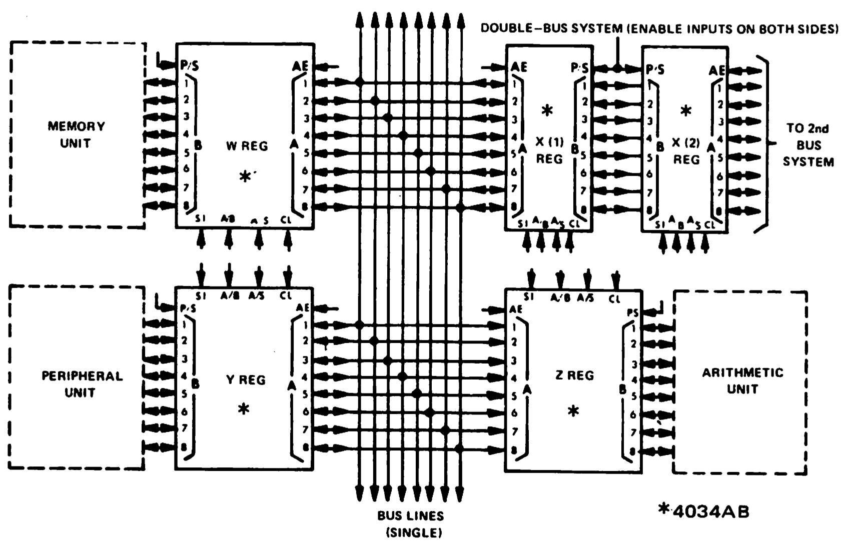


A "High" ("Low") on the Shift Left/Shift Right input allows serial data on the Shift Left Input (Shift Right Input) to enter the register on the positive transition of the clock signal. A "high" on a "A" Enable Input disables the "A" parallel data lines on Reg. 1 and 2 and enables the "A" data lines on register 3 and 4 and allows parallel data into registers 1 and 2. Other logic schemes may be used in place of registers 3 and 4 for parallel loading.

When parallel inputs are not used Reg. 3 and 4 and associated logic are not required.

*Shift Left input must be disabled during parallel entry.

Shift right/shift left with parallel inputs



*4034AB

The "A" enable (AE) and A/B signals control all combinations of transfer between the registers and bus systems.

Single and double-bus systems

CMOS 4-BIT PARALLEL-IN/PARALLEL-OUT SHIFT REGISTER

FEATURES

- 4-Stage Clocked Serial-Shift Operation
- Synchronous Parallel Loading of All Stages
- J-$\overline{K}$ Serial Inputs to First Stage
- Asynchronous True/Complement Control of all Outputs
- Asynchronous Reset
- Static Operation — DC to 6MHz @ 10Vdc

DESCRIPTION

The 4035B is a Four-Stage Clocked Serial Register having provisions for synchronous parallel inputs to each stage and serial inputs to the first stage via J$\overline{K}$ logic. Register stages 2, 3, and 4 are coupled in a serial "D" flip-flop configuration when the register is in the serial mode (Parallel/Serial control low).

Parallel entry via the "D" line of each register stage is permitted only when the Parallel/Serial control is high. In the parallel or serial mode information is transferred on positive Clock transitions.

When the True/Complement control is high, the true contents of the register are available at the output terminals. When the True/Complement control is low, the outputs are the complements of the data in the register. The True/Complement control functions asynchronously with respect to the Clock signal.

J$\overline{K}$ input logic is provided on the first stage serial input to minimize logic requirements, particularly in counting and sequence-generation applications. With J$\overline{K}$ inputs connected together, the first stage becomes a "D" flip-flop. An asynchronous common Reset is also provided.

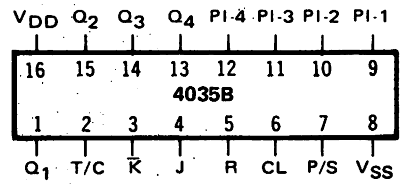
This device may be used for shift-right/shift-left registers, parallel-to-serial/serial-to-parallel conversion, sequence generation, up/down Johnson or ring counters, pseudo-random code generation, frequency and phase comparators, and sample-and-hold registers.

TRUTH TABLE

	t_{n-1} (Inputs)				t_n (Outputs)
CL	J	$\overline{K}$	R	Q_{n-1}	Q_n
↑	0	X	0	0	0
↑	1	X	0	0	1
↑	X	0	0	1	0
↑	1	0	0	Q_{n-1}	$\overline{Q}_{n-1}$ Toggle Mode
↑	X	1	0	1	1
↓	X	X	0	Q_{n-1}	Q_{n-1}
X	X	X	1	X	0

X = Don't Care

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

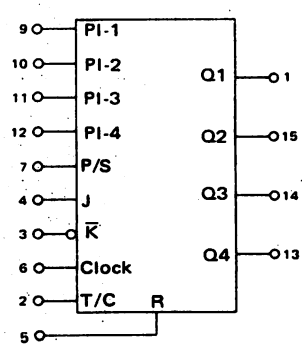
C	16-pin Cerdip
D	16-pin Ceramic
E	16-pin Epoxy
F	16-pin Flat
H	Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS [1]

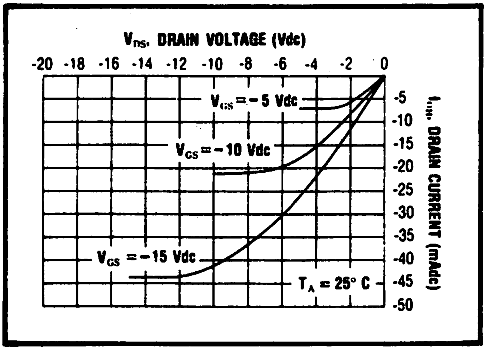
PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[2] Min.	T_{LOW}[2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH}[2] Min.	T_{HIGH}[2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN}=V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	µAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		15	combinations	–	20	–	0.2	20	–	600	

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

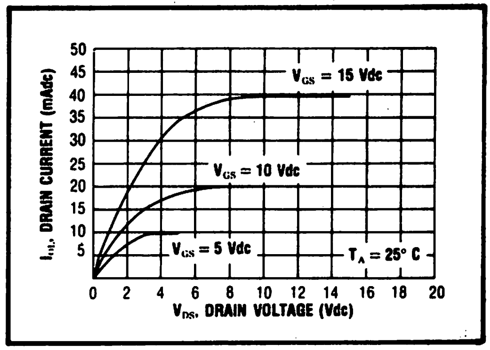
DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME From Clock Input	t_{PLH}, t_{PHL}	5	–	250	500	ns
		10	–	100	200	
		15	–	75	150	
From T/C Input	t_{PLH}, t_{PHL}	5	–	150	300	ns
		10	–	60	120	
		15	–	45	90	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	80	160	ns
		10	–	40	80	
		15	–	30	60	
MINIMUM CLOCK PULSE WIDTH	PW_{CL}	5	–	100	200	ns
		10	–	45	90	
		15	–	30	60	
MAXIMUM CLOCK FREQUENCY	f_{CL}	5	2.0	4.0	–	MHz
		10	5.0	10.0	–	
		15	6.0	12.0	–	
MAXIMUM CLOCK RISE & FALL TIME[1]	t_{rCL}, t_{fCL}	5	15	–	–	µs
		10	15	–	–	
		15	15	–	–	
MINIMUM SETUP TIME J, $\overline{K}$ Inputs	t_{setup}	5	–	110	220	ns
		10	–	40	80	
		15	–	30	60	
P/S, Parallel Inputs	t_{setup}	5	–	70	140	ns
		10	–	25	50	
		15	–	20	40	
MINIMUM HOLD TIME J, $\overline{K}$ inputs	t_{hold}	5	–	-25	25	ns
		10	–	-10	10	
		15	–	- 5	5	
P/S, Parallel Inputs	t_{hold}	5	–	-25	25	ns
		10	–	-10	10	
		15	–	- 5	5	
RESET OPERATION						
PROPAGATION DELAY TIME	t_{PHL}	5	–	230	460	ns
		10	–	120	240	
		15	–	90	180	
MINIMUM RESET PULSE WIDTH	PW_R	5	–	125	250	ns
		10	–	55	110	
		15	–	40	80	

[1] When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.

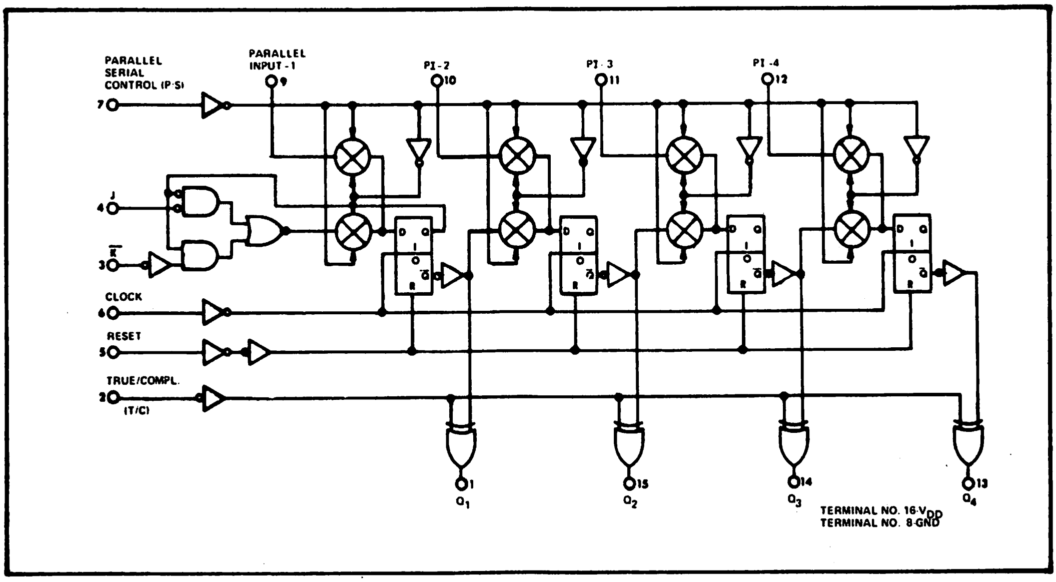


Typical P-Channel
Source Current Characteristics

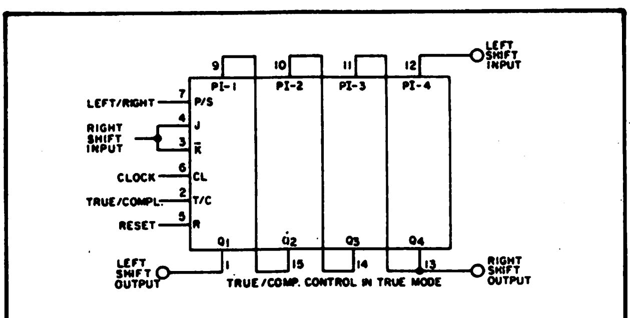


Typical N-Channel
Sink Current Characteristics

LOGIC DIAGRAM



APPLICATIONS INFORMATION



Shift Left/Shift Right Register

CMOS 12-STAGE BINARY COUNTER

FEATURES

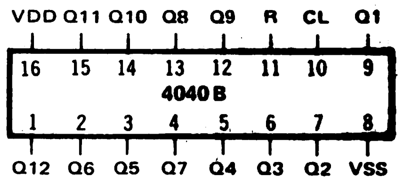
- 12 Fully Static Stages
- All 12 Buffered Outputs Available
- Common Reset Line
- 8MHz Counting Rate @ 10Vdc
- All Inputs Buffered

DESCRIPTION

The 4040 B consists of 12-ripple-carry binary counter stages with appropriate input buffers and reset circuitry. The counter is reset to its "all 0's" state by a high level on the Reset input. The counter is advanced one count on the negative-going transition of each input pulse. Isolation from external noise and the effects of loads is provided by output buffering.

Applications include time delay circuits, counter controls, and frequency dividers.

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

C	16-pin Cerdip
D	16-pin Ceramic
E	16-pin Epoxy
F	16-pin Flat
H	Chip

TRUTH TABLE

Clock	Reset	Output State
↑	0	No Change
↓	0	Advance to next state
x	1	All Outputs are low

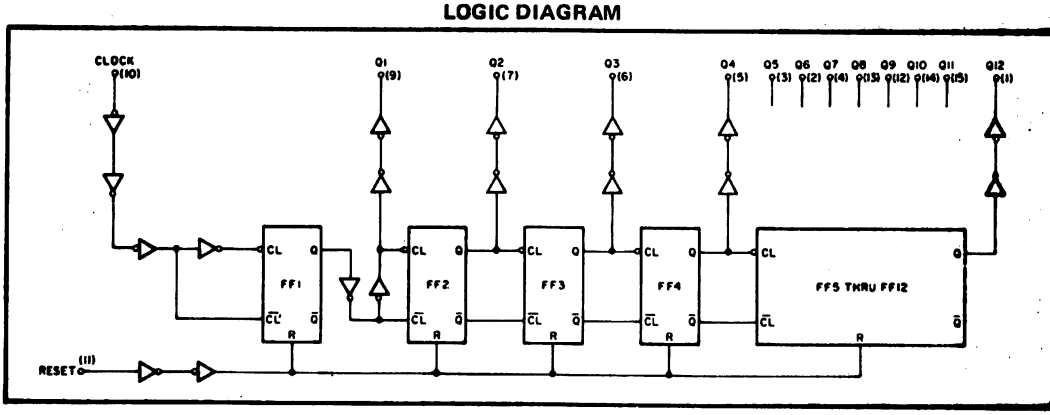
X = Don't Care

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} \cdot V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

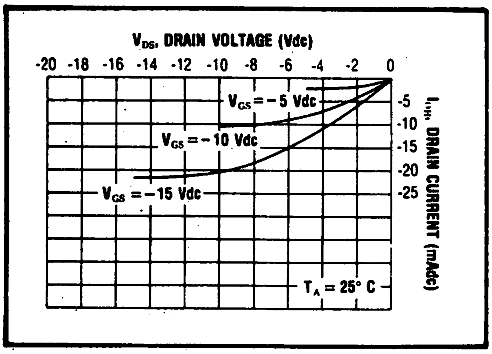
STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2]		+25°C			T_{HIGH} [2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN}=V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	μAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		15	combinations	–	20	–	0.2	20	–	600	

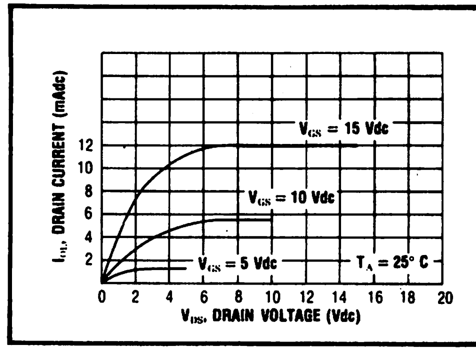
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME Clock to Q1	t_{PLH}, t_{PHL}	5	–	180	320	ns
		10	–	80	160	
		15	–	65	130	
Q_i to Q_{i+1}	t_{PLH}, t_{PHL}	5	–	100	200	ns
		10	–	40	60	
		15	–	30	30	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	40	80	
		15	–	30	60	
MINIMUM CLOCK PULSE WIDTH	PW_{CL}	5	–	70	140	ns
		10	–	30	60	
		15	–	20	40	
MAXIMUM CLOCK FREQUENCY	f_{CL}	5	3.0	4.5	–	MHz
		10	6.0	9.0	–	
		15	7.5	11.0	–	
MAXIMUM CLOCK RISE AND FALL TIME	t_{rCL}, t_{fCL}	5	50	100	–	μs
		10	50	100	–	
		15	50	100	–	
RESET OPERATION						
PROPAGATION DELAY TIME	t_{PHL}	5	–	200	400	ns
		10	–	100	200	
		15	–	75	150	
MINIMUM RESET PULSE WIDTH	PW_R	5	–	100	200	ns
		10	–	40	80	
		15	–	30	60	
RESET REMOVAL TIME	t_{rem}	5	–	150	300	ns
		10	–	65	125	
		15	–	40	75	

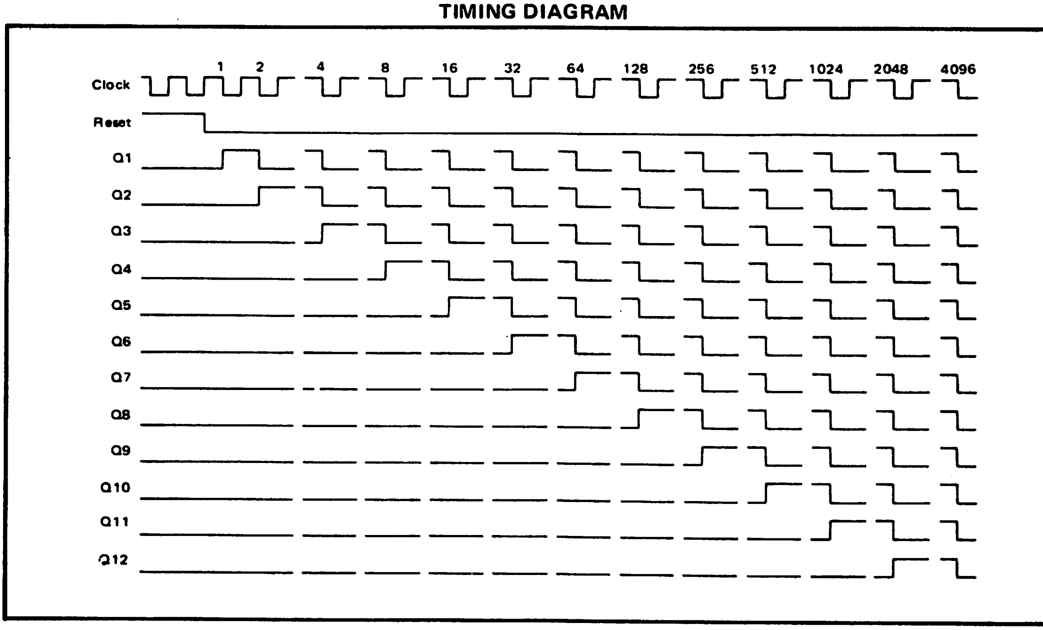


Typical P-Channel
Source Current Characteristics

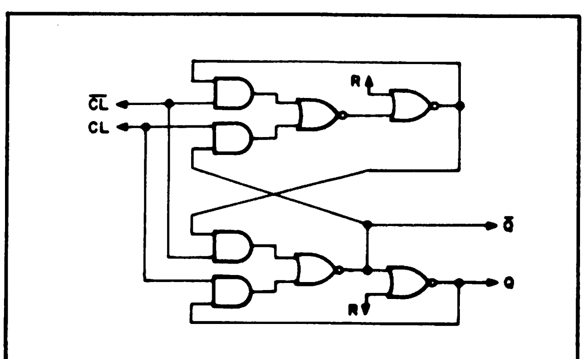


Typical N-Channel
Sink Current Characteristics

TIMING DIAGRAM



TYPICAL COUNTER STAGE



CMOS QUAD TRUE/COMPLEMENT BUFFER

FEATURES

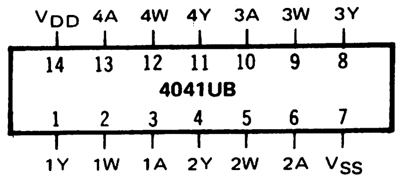
- Both True and Complement Outputs Available Simultaneously
- High Source and Sink Current
- Diode Protection on All Inputs

DESCRIPTION

The 4041UB Quad True/Complement Buffer is a monolithic integrated circuit constructed with P-Channel and N-Channel enhancement-mode devices. The outputs have low resistance and are capable of sinking or sourcing high currents for use in driver applications where high noise immunity and low power dissipation are required.

This device is useful as a line-driver, CMOS-to-TTL driver, low-power resistor-network driver for A/D and D/A conversion, display and clock drivers.

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

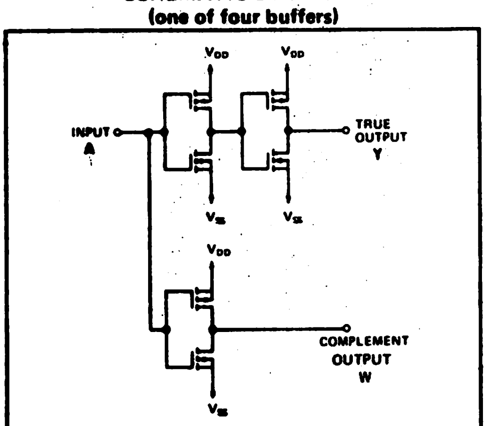
C	14-pin Cerdip
D	14-pin Ceramic
E	14-pin Epoxy
F	14-pin Flat
H	Chip

RECOMMENDED OPERATING CONDITIONS

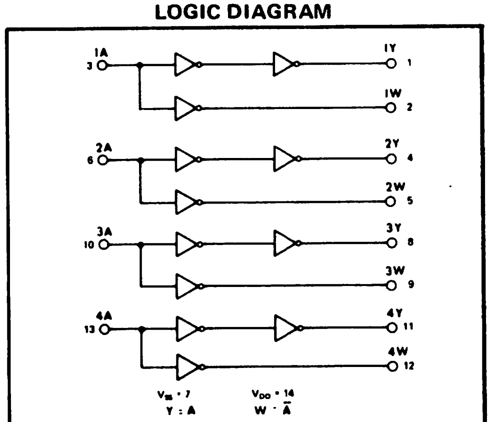
For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

SCHEMATIC DIAGRAM
(one of four buffers)



LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2]		+25°C			T_{HIGH} [2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN}=V_{SS}$ or V_{DD}	–	1.0	–	0.005	1.0	–	30	μAdc
		10	All valid input	–	2.0	–	0.01	2.0	–	60	
		15	combinations	–	4.0	–	0.02	4.0	–	120	
MINIMUM INPUT HIGH VOLTAGE	V_{IH}										
Non-Inverting Outputs		5	$V_{OH}=4.5V$	–	3.5	–	2.75	3.5	–	3.5	Vdc
		10	$V_{OH}=9.0V$	–	7.0	–	5.5	7.0	–	7.0	
		15	$V_{OH}=13.5V$	–	11.0	–	8.25	11.0	–	11.0	
			$\|I_O\| \leq 1\mu A$								
Inverting Outputs		5	$V_{OL}=0.5V$	–	4.0	–	2.75	4.0	–	4.0	Vdc
		10	$V_{OL}=1.0V$	–	8.0	–	5.5	8.0	–	8.0	
		15	$V_{OL}=1.5V$	–	12.0	–	8.25	12.0	–	12.0	
			$\|I_O\| \leq 1\mu A$								
MAXIMUM INPUT LOW VOLTAGE	V_{IL}										
Non-Inverting Outputs		5	$V_{OL}=0.5V$	1.5	–	1.5	2.25	–	1.5	–	Vdc
		10	$V_{OL}=1.0V$	3.0	–	3.0	4.5	–	3.0	–	
		15	$V_{OL}=1.5V$	4.0	–	4.0	6.75	–	4.0	–	
			$\|I_O\| \leq 1\mu A$								
Inverting Outputs		5	$V_{OH}=4.5V$	1.0	–	1.0	2.25	–	1.0	–	Vdc
		10	$V_{OH}=9.0V$	2.0	–	2.0	4.5	–	2.0	–	
		15	$V_{OH}=13.5V$	3.0	–	3.0	6.75	–	3.0	–	
			$\|I_O\| \leq 1\mu A$								
OUTPUT HIGH (SOURCE) CURRENT	I_{OH}										
Non-Inverting Outputs		5	$V_{OH}=4.6V$	-1.7	–	-1.4	-2.8	–	-1.0	–	mAdc
		10	$V_{OH}=9.5V$	-5.0	–	-4.0	-8.0	–	-2.8	–	
		15	$V_{OH}=13.5V$	-16	–	-13	-26	–	-9	–	
			$V_{IN}=V_{DD}$								
Inverting Outputs		5	$V_{OH}=4.6V$	-0.75	–	-0.6	-1.0	–	-0.42	–	mAdc
		10	$V_{OH}=9.5V$	-2.2	–	-1.8	-3.6	–	-1.3	–	
		15	$V_{OH}=13.5V$	-8.0	–	-6.5	-13	–	-4.5	–	
			$V_{IN}=V_{SS}$								
OUTPUT LOW (SINK) CURRENT	I_{OL}										
Non-Inverting Outputs		5	$V_{OL}=0.4V$	2.0	–	1.6	3.2	–	1.1	–	mAdc
		10	$V_{OL}=0.5V$	6.2	–	5.0	10	–	3.5	–	
		15	$V_{OL}=1.5V$	23	–	18.5	38	–	13	–	
			$V_{IN}=V_{SS}$								
Inverting Outputs		5	$V_{OL}=0.4V$	1.0	–	0.8	1.3	–	0.56	–	mAdc
		10	$V_{OL}=0.5V$	2.5	–	2.0	4.0	–	1.4	–	
		15	$V_{OL}=1.5V$	11	–	8.5	17	–	5.8	–	
			$V_{IN}=V_{DD}$								

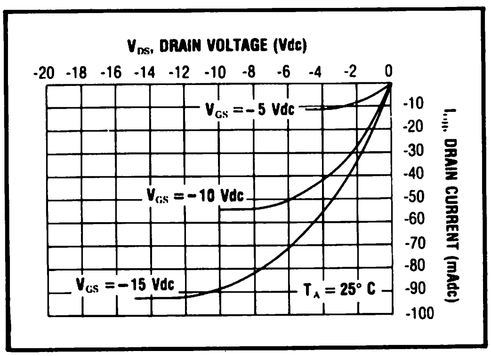
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

ELECTRICAL CHARACTERISTICS (Continued)

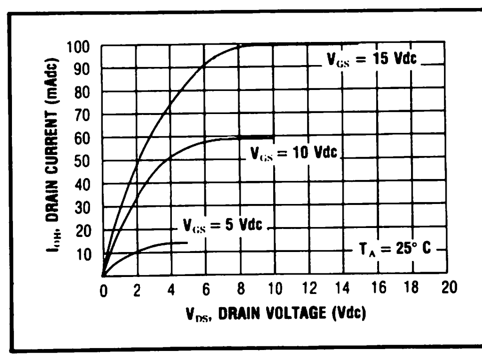
DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME Non-Inverting Outputs	t_{PLH}, t_{PHL}	5 10 15	– – –	60 35 25	120 70 50	ns
Inverting Outputs	t_{PLH}, t_{PHL}	5 10 15	– – –	60 35 25	120 70 50	ns
OUTPUT TRANSITION TIME Non-Inverting Outputs	t_{TLH}, t_{THL}	5 10 15	– – –	40 20 15	80 40 30	ns
Inverting Outputs	t_{TLH}, t_{THL}	5 10 15	– – –	35 20 15	70 40 30	ns
INPUT CAPACITANCE	C_{IN}	–	–	10	15	pF

NON-INVERTING (TRUE) OUTPUT

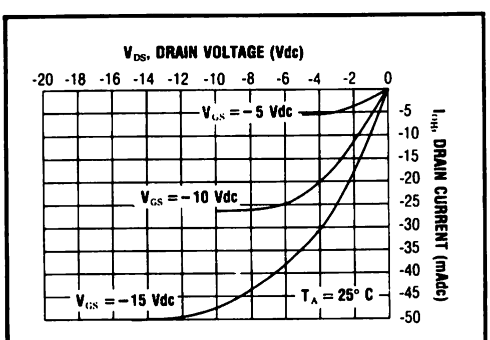


Typical P-Channel
Source Current Characteristics

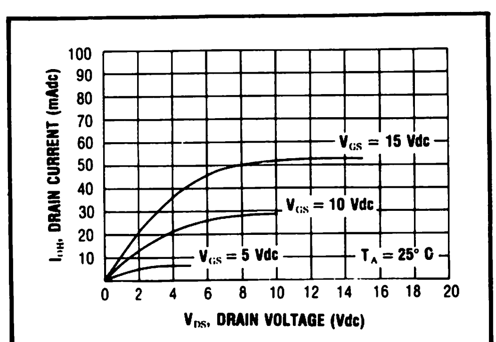


Typical N-Channel
Sink Current Characteristics

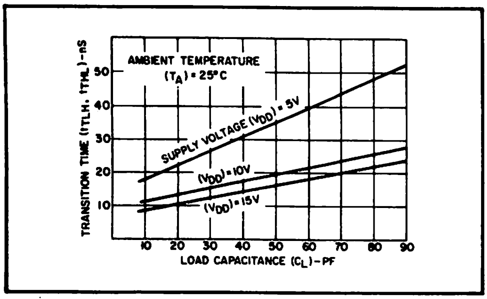
INVERTING (COMPLEMENT) OUTPUT



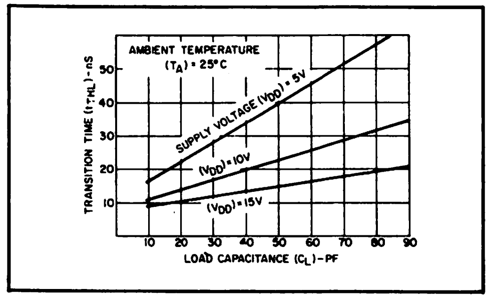
Typical P-Channel
Source Current Characteristics



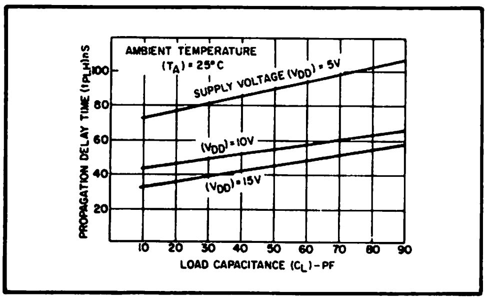
Typical N-Channel
Sink Current Characteristics



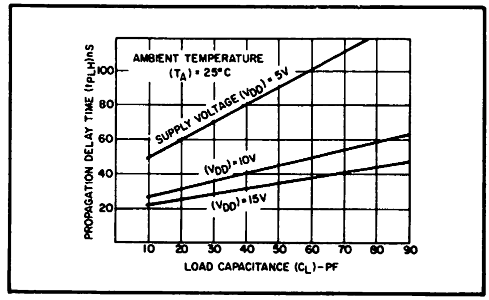
Typical transition time vs. C_L-true output.



Typical transition time vs. C_L-complement output.



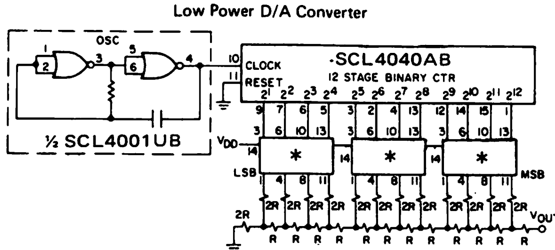
Typical propagation delay time vs. C_L-true output.



Typical propagation delay time vs. C_L-complement output.

APPLICATIONS INFORMATION

Low Power D/A Converter



*4041UB

For resolution and accuracy of ± ½ least significant bit (LSB), choose the values for R (shown in Table I) where R equals the value of the external ladder resistor plus the switch source impedance.

The values have been tabulated for V_{DD} = 5V and V_{SS} = 0V. For different supply (reference) voltages, the switch source impedance must be computed and added to the value of R shown in Table I).

TABLE I. RESISTANCE VALUES AT $V_{DD}-V_{SS}$ = 5V, T_A = 25°C

RESOLUTION	ACCURACY OF 1/2 LSB	R_{min} (Ω)
4 bit	± 3.25% of full scale	3.5 k
6 bit	± 0.8% of full scale	14 k
8 bit	± 0.2% of full scale	56 k
10 bit	± 0.05% of full scale	224 k
12 bit	± 0.0125% of full scale	896 k

TABLE II. ON RESISTANCE VALUES AT V_{DS} = 0.1V, T_A = 25°C

$V_{DD}-V_{SS}$ (Volts)	R_N (Ω)	R_P (Ω)
5	175 ± 50	200 ± 75
10	75 ± 25	90 ± 30

CMOS QUAD LATCH

FEATURES

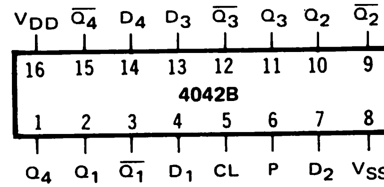
- **Common Clock**
- **Positive- or Negative-Edge Clocking**
- **Q and $\overline{Q}$ Outputs Available from Each Latch**

DESCRIPTION

4042B devices contain four Latch circuits, each strobed by a common Clock. Complementary buffered outputs are available from each circuit.

Information present at the Data input is transferred to outputs Q and $\overline{Q}$ during the Clock level which is programmed by the Polarity input. For Polarity = 0 the transfer occurs during the 0 Clock level and for Polarity = 1 the transfer occurs during the 1 Clock level. The outputs follow the Data inputs providing the Clock and Polarity levels defined above are present. When a Clock transition occurs (positive for Polarity = 0 and negative for Polarity = 1) the information present at the input during the Clock transition is retained at the outputs until an opposite Clock transition occurs.

CONNECTION DIAGRAM
(all packages)



RECOMMENDED OPERATING CONDITIONS

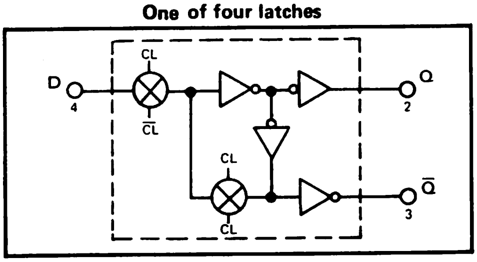
For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

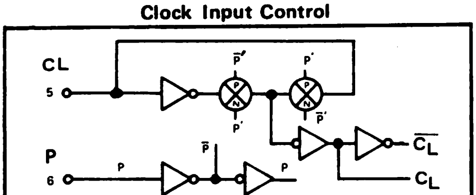
TRUTH TABLE

CLOCK	POLARITY	Q
0	0	D
↑	0	LATCH
1	1	D
↓	1	LATCH

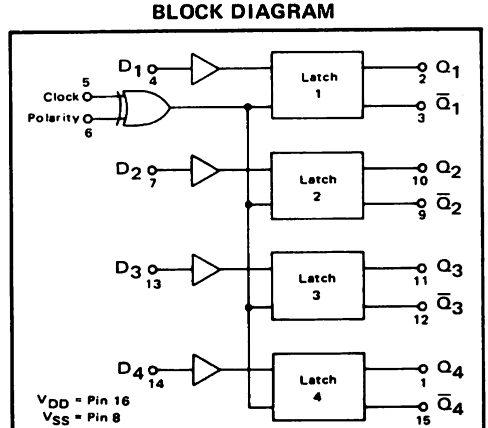
LOGIC DIAGRAMS
One of four latches



Clock Input Control



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

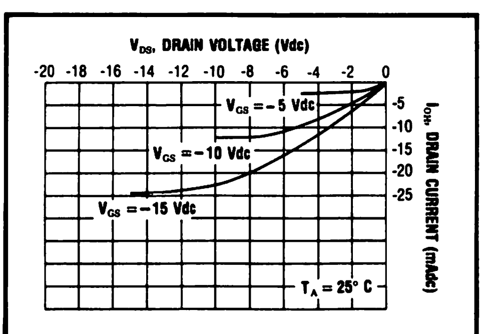
STATIC CHARACTERISTICS[1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[2] Min.	T_{LOW}[2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH}[2] Min.	T_{HIGH}[2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN}=V_{SS}$ or V_{DD}	–	5	–	1.0	5	–	150	μAdc
		10	All valid input	–	10	–	2.0	10	–	300	
		15	combinations	–	20	–	4.0	20	–	600	

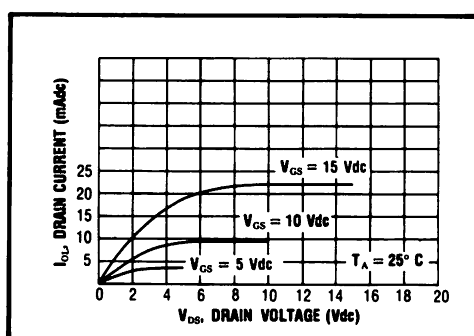
NOTES: [1] Remaining Static Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME From Data Inputs	t_{PLH}, t_{PHL}	5	–	110	220	ns
		10	–	55	110	
		15	–	40	80	
From Clock Polarity Inputs	t_{PLH}, t_{PHL}	5	–	150	300	ns
		10	–	75	150	
		15	–	50	100	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
MINIMUM CLOCK PULSE WIDTH	PW_{CL}	5	–	100	200	ns
		10	–	50	100	
		15	—	30	60	
MAXIMUM CLOCK RISE AND FALL TIME	t_{rCL}, t_{fCL}	5	15	–	–	μs
		10	5	–	–	
		15	3	–	–	
MINIMUM DATA INPUT SETUP TIME	t_{setup}	5	–	-20	50	ns
		10	–	-10	30	
		15	–	-5	25	
MINIMUM DATA INPUT HOLD TIME	t_{hold}	5	–	0	100	ns
		10	–	0	50	
		15	–	0	40	



Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

CMOS QUAD 3-STATE R-S LATCHES

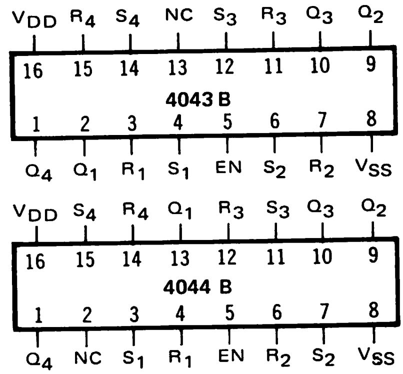
FEATURES

- Separate Set and Reset Inputs for each Latch
- Active-High (4043 B) or Active-Low (4044 B) Inputs
- 3-State Outputs with Common Enable

DESCRIPTION

4043B types are Quad cross-coupled 3-state CMOS NOR Latches, and the 4044 B types are Quad cross-coupled 3-state CMOS NAND Latches. Each latch has a separate Q output and individual Set and Reset inputs. The Q outputs are gated through transmission gates controlled by a common Enable input. A logic "1" or "high" on the Enable input connects the latch states to the Q outputs. A logic "0" or "low" on the Enable input disconnects the latch states from the Q outputs, resulting in an open circuit condition on the Q outputs. The open circuit feature allows common bussing of the outputs. The logic operation of the latches is summarized in the truth table below.

CONNECTION DIAGRAMS
(all packages)



Add suffix for package:

C	16-pin Cerdip	F	16-pin Flat
D	16-pin Ceramic	H	Chip
E	16-pin Epoxy		

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

TRUTH TABLES

4043 B

S	R	E	Q
X	X	0	OC*
0	0	1	NC+
1	0	1	1
0	1	1	0
1	1	1	△

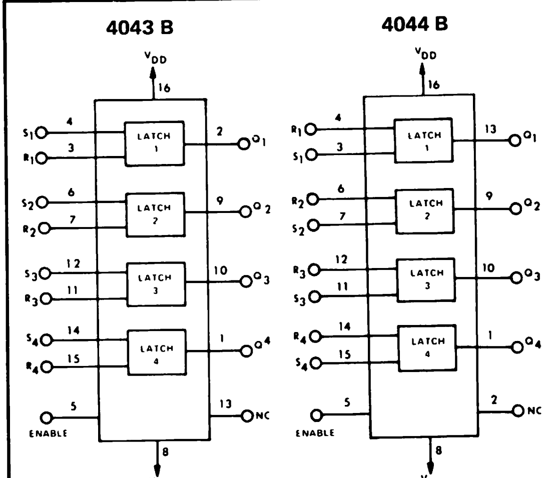
* OPEN CIRCUIT
\+ NO CHANGE
△ DOMINATED BY S = 1 INPUT

4044 B

S	R	E	Q
X	X	0	OC*
1	1	1	NC+
0	1	1	1
1	0	1	0
0	0	1	△△

* OPEN CIRCUIT
\+ NO CHANGE
△△ DOMINATED BY R = 0 INPUT

BLOCK DIAGRAMS



ELECTRICAL CHARACTERISTICS

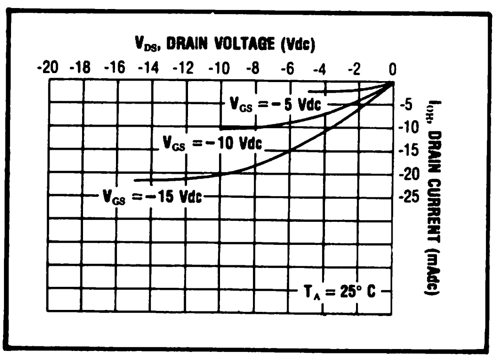
STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[2] Min.	T_{LOW}[2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH}[2] Min.	T_{HIGH}[2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5 10 15	$V_{IN}=V_{SS}$ or V_{DD} All valid input combinations	– – –	1.0 2.0 4.0	– – –	0.005 0.01 0.02	1.0 2.0 4.0	– – –	30 60 120	μAdc
3-STATE OUTPUT LEAKAGE CURRENT	I_{ZL}	15	Enable = V_{SS}	–	±0.1	–	$\pm10^{-4}$	±0.1	–	±1.0	μAdc

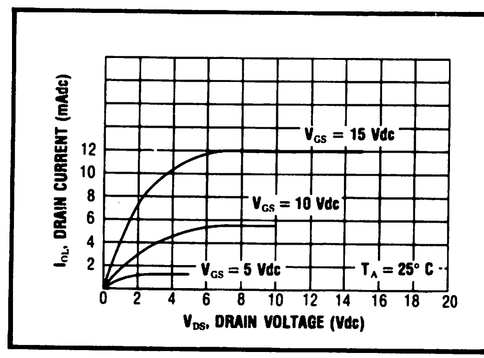
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME From S or R Inputs	t_{PLH}, t_{PHL}	5 10 15	– – –	150 70 50	300 140 100	ns
From Enable Input	t_{PHZ}, t_{PLZ} t_{PZH}, t_{PZL}	5 10 15	– – –	75 35 30	150 70 60	ns
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5 10 15	– – –	100 50 40	200 100 80	ns
MINIMUM SET OR RESET PULSE WIDTH	PW_S, PW_R	5 10 15	– – –	80 40 30	160 80 60	ns
SET OR RESET REMOVAL TIME	t_{rem}	5 10 15	– – –	25 15 10	50 30 20	ns

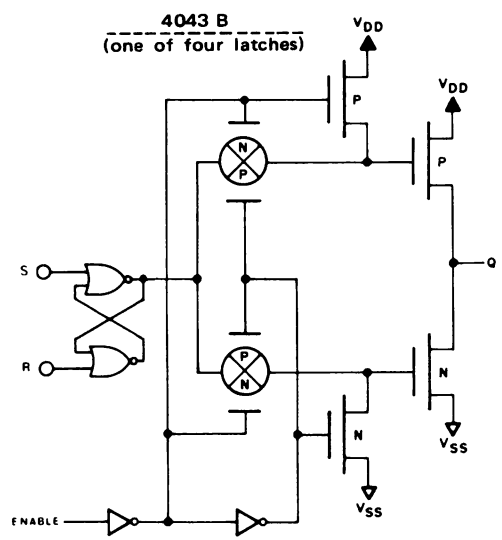


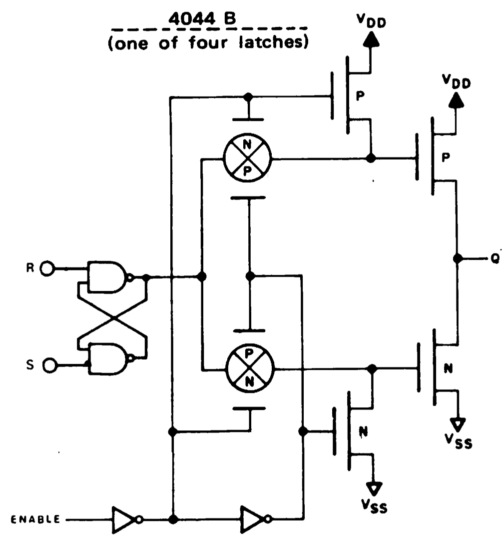
Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

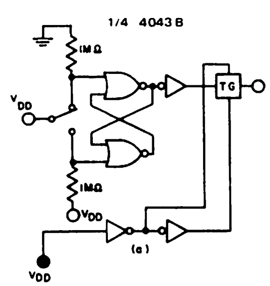
LOGIC DIAGRAMS

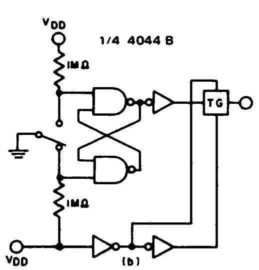




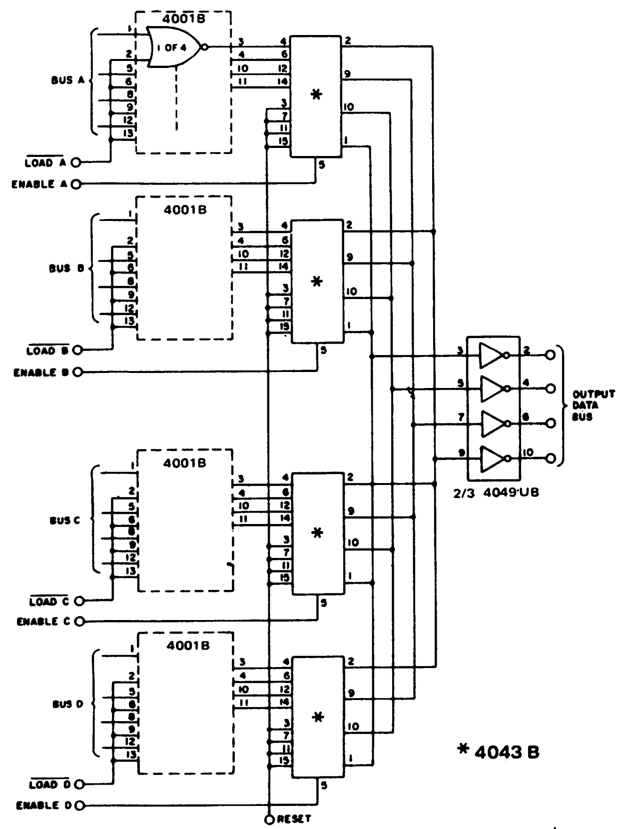
APPLICATIONS INFORMATION

Switch bounce eliminator





Multiple bus storage



CMOS PHASE-LOCKED LOOPS

FEATURES

- Very low power consumption – 70 μW (typ) @ f_o = 10kHz, 5Vdc
- Operating frequency range (no offset) – Up to 3MHz (typ) @ 10Vdc (4046B) Up to 4MHz (typ) @ 10Vdc (4446B)
- Low frequency drift – 0.04%/°C (typ) @ 10Vdc
- Choice of two phase comparators:
  1. Exclusive-OR network
  2. Edge-controlled memory network with phase-pulse output for lock indication
- VCO Inhibit control for ON-OFF keying and ultra-low standby power consumption
- High VCO linearity 1% (typ)
- Source-follower output of VCO control input (Demodulator Output)
- Zener Diode to assist Supply Regulation

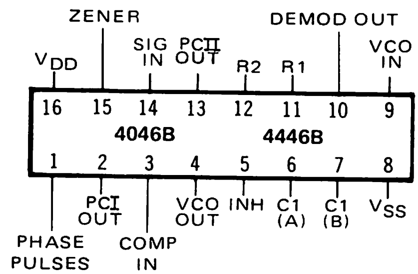
APPLICATIONS

- FM demodulator and modulator
- Frequency synthesis and multiplication
- Frequency discriminator
- Data synchronization
- Voltage-to-frequency conversion
- Tone decoding
- FSK-Modems
- Signal conditioning

DESCRIPTION

The 4046B and 4446B phase-locked loops contain two phase comparators, a voltage-controlled oscillator (VCO), source follower, and zener diode. The comparators have two common inputs. The Signal input can be used directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. The self-bias circuit adjusts small voltage signals in the linear region of the amplifier. Phase comparator I (an exclusive-OR gate) provides a digital error signal PCI_{out}, and maintains 90° phase shift at the center frequency between Signal and Comparator inputs (both at 50% duty cycle). Phase comparator II (with leading edge sensing logic) provides digital error signals $PCII_{out}$ and Phase Pulses, and maintains a 0° phase shift between input signals (duty cycle is immaterial). The linear VCO produces an output signal VCO_{out} whose frequency is determined by the voltage of input VCO_{in} and the capacitor and resistors connected to pins $C1_A$, $C1_B$, R1, and R2. The source follower output, Demod Out, with an external resistor is used where the VCO_{in} signal is needed but no loading can be tolerated. The inhibit input Inh, when high, disables the VCO and source follower to minimize standby power consumption. The zener diode can be used to assist in power supply regulation.

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

C	16-pin Cerdip
D	16-pin Ceramic
E	16-pin Epoxy
F	16-pin Flat
H	Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

BLOCK DIAGRAM

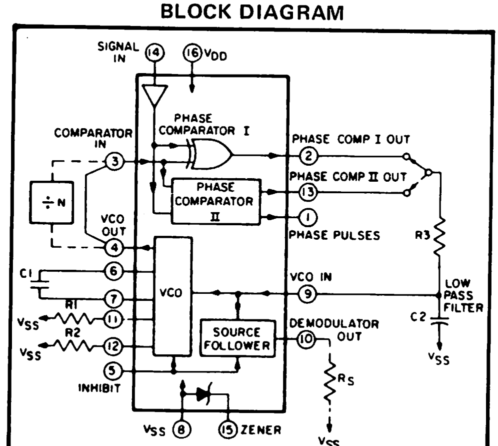


Fig. 1

VCO SECTION

The VCO requires one external capacitor (C1) and one to two external resistors (R1 or R1 and R2). Resistor R1 and capacitor C1 determine the frequency range of the VCO and resistor R2 enables the VCO to have a frequency offset if required. The high input impedance ($10^{12}\Omega$) of the VCO simplifies the design of low-pass filters by permitting the designer a wide choice of resistor-to-capacitor ratios. In order not to load the low-pass filter, a source-follower output of the VCO input voltage is provided at terminal 10 (DEMODULATOR OUTPUT). If this terminal is used, a load resistor (R_S) of 50kΩ or more should be connected from this terminal to V_{SS}. If unused, this terminal should be left open. The VCO can be connected directly or through frequency dividers to the comparator input of the phase comparators. A full CMOS logic swing is available at the output of the VCO. A logic 0 on the INHIBIT input "enables" the VCO and the source follower, while a logic 1 "turns off" both to minimize stand-by power consumption.

PHASE COMPARATORS

The phase-comparator signal input (terminal 14) can be direct-coupled provided the signal swing is within CMOS logic levels [logic "0" $\leqslant$ 30% (V_{DD}-V_{SS}), logic "1" $\geqslant$ 70% (V_{DD}-V_{SS})]. For smaller swings the signal must be capacitively coupled to the self-biasing amplifier at the signal input.

Phase comparator I is an exclusive-OR network; it operates analogously to an over-driven balanced mixer. To maximize the lock range, the signal and comparator-input frequencies must have a 50% duty cycle. With no signal or noise on the signal input, this phase comparator has an average output voltage equal to $V_{DD}/2$. The low-pass filter connected to the output of phase comparator I supplies the averaged voltage to the VCO input, and causes the VCO to oscillate at the center frequency (f_o).

The frequency range of input signals on which the PLL will lock, if it was initially out of lock, is defined as the frequency capture range ($2f_c$).

The frequency range of input signals on which the loop will stay locked if it was initially in lock is defined as the frequency lock range ($2f_L$). The capture range can not exceed the lock range.

With phase comparator I, the range of frequencies over which the PLL can acquire lock (capture range) is dependent on the low-pass-filter characteristics, and can be made as large as the lock range. Phase-comparator I enables a PLL system to remain in lock in spite of high amounts of noise in the input signal.

One characteristic of this type of phase comparator is that it may lock onto input frequencies that are close to harmonics of the VCO center-frequency. A second characteristic is that the phase angle between the signal and the comparator input varies between 0° and 180°, and is 90° at the center frequency. Figure 2 shows the (typical) triangular phase-to-output response characteristic of phase-comparator I. Typical waveforms for a CMOS phase-locked-loop employing phase comparator I in locked condition is shown in Figure 3.

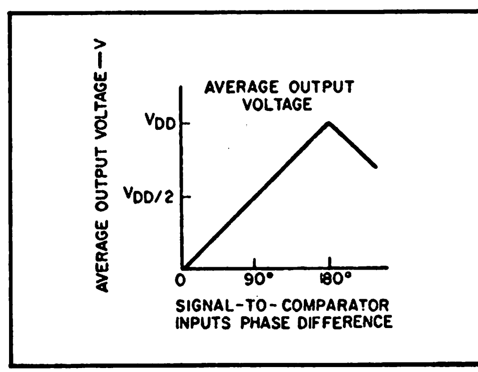


Fig. 2 — Phase-comparator I characteristics at low-pass filter output.

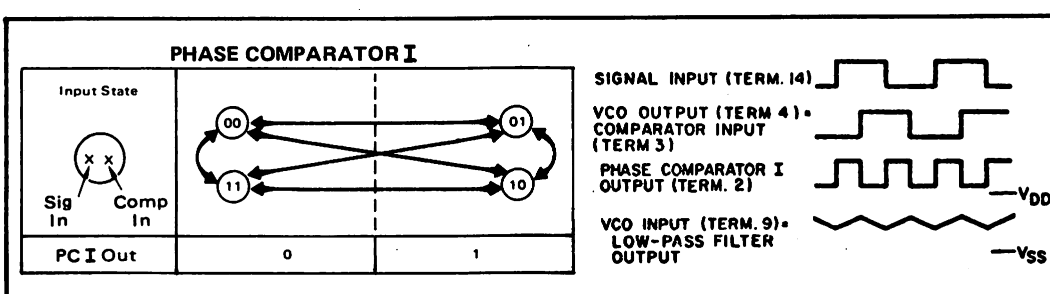
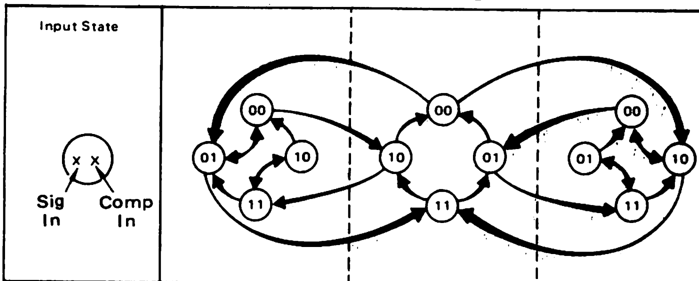
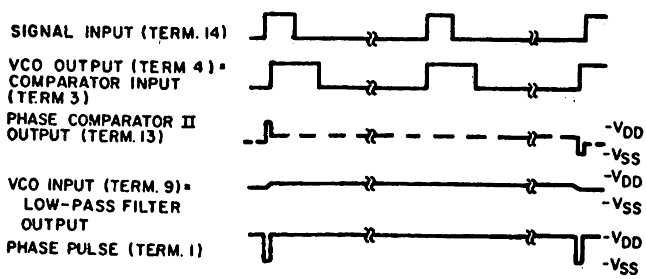


Fig. 3 — Typical waveforms employing phase comparator I in locked condition

PHASE COMPARATOR II



PC II Out	0	3 State Output Disconnected	1
Phase Pulses	0	1	0



NOTE: DASHED LINE IS AN OPEN-CIRCUIT CONDITION

Fig. 4 — Typical waveforms employing phase comparator II in locked condition.

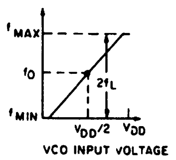
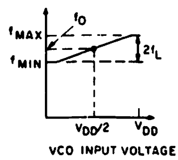
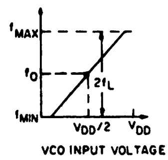
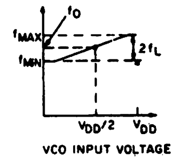
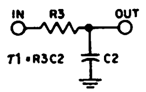
Phase-comparator II is an edge-controlled digital memory network. It consists of several flip-flop stages, control gating, and a three state output circuit comprising p- and n-type drivers having a common output node. When the p-MOS or n-MOS drivers are ON, they pull the output up to V_{DD} or down to V_{SS}, respectively. This type of phase comparator acts only on the positive edges of the signal and comparator inputs. The duty cycles of the signal and comparator inputs are not important since positive transitions control the PLL system utilizing this type of comparator. If the signal lags the comparator input in phase, the n-type output driver is maintained ON for a time corresponding to the phase difference. If the comparator input lags the signal in phase, the p-type output driver is maintained ON for a time corresponding to the phase difference. Subsequently, the capacitor voltage of the low-pass filter connected to this phase comparator is adjusted until the signal and comparator inputs are equal in both phase and frequency. At this stable point, both p- and n-type output drivers remain OFF. Thus, the phase comparator output becomes an open circuit and holds the voltage on the capacitor of the low-pass filter constant. Moreover, the signal at the "phase pulses" output is a high level which can be used for indicating a locked condition. Thus, for phase comparator II, no phase difference exists between signal and comparator input over the full VCO frequency range. Moreover, the power dissipation due to the low-pass filter is reduced when this type of phase comparator is used because both the p- and n-type output drivers are OFF for most of the signal input cycle.

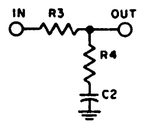
It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range, independent of the low-pass filter. With no signal present at the signal input, the VCO is adjusted to its lowest frequency for phase comparator II. Figure 4 shows typical waveforms for a CMOS PLL employing phase comparator II in a locked condition.

DESIGN INFORMATION

This information is a guide for approximating the values of external components for the 4046B and 4446B in a Phase-Locked Loop system. The selected external components must be within the following ranges:

$R1, R2 \geqslant 2k\Omega$, $R_S \geqslant 10k\Omega$
$C1 \geqslant 15pF$
In addition to the given design information refer to Figure 5 for R1, R2, and C1 component selections.

<table>
<tr><th rowspan="2">CHARACTERISTICS</th><th colspan="2">USING PHASE COMPARATOR I</th><th colspan="2">USING PHASE COMPARATOR II</th></tr>
<tr><th>VCO WITHOUT OFFSET $R_2 = \infty$</th><th>VCO WITH OFFSET</th><th>VCO WITHOUT OFFSET $R_2 = \infty$</th><th>VCO WITH OFFSET</th></tr>
<tr><td>VCO Frequency</td><td>
</td><td>
</td><td>
</td><td>
</td></tr>
<tr><td>For No Signal Input</td><td colspan="2">VCO in PLL system will adjust to center frequency, f_o</td><td colspan="2">VCO in PLL system will adjust to lowest operating frequency, f_{min}</td></tr>
<tr><td>Frequency Lock Range, $2f_L$</td><td colspan="4">$2f_L$ = full VCO frequency range
$2f_L = f_{max} - f_{min}$</td></tr>
<tr><td>Frequency Capture Range, $2f_C$</td><td colspan="2">

$2f_C \approx \frac{1}{\pi}\sqrt{\frac{2\pi f_L}{\tau 1}}$</td><td colspan="2" rowspan="2">$f_C = f_L$</td></tr>
<tr><td>Loop Filter Component Selection</td><td colspan="2">

For $2f_C$, see Ref.</td></tr>
<tr><td>Phase Angle between Signal and Comparator</td><td colspan="2">90° at center frequency (f_o), approximating 0° and 180° at ends of lock range ($2f_L$)</td><td colspan="2">Always 0° in lock</td></tr>
<tr><td>Locks on Harmonics of Center Frequency</td><td colspan="2">Yes</td><td colspan="2">No</td></tr>
<tr><td>Signal Input Noise Rejection</td><td colspan="2">High</td><td colspan="2">Low</td></tr>
<tr><td>VCO Component Selection</td><td>– Given: f_o
– Use f_o with Fig.5a to determine R1 and C1</td><td>– Given: f_o and f_L
– Calculate f_{min} from the equation $f_{min} = f_o - f_L$
– Use f_{min} with Fig. 5b to determine R2 and C1
– Calculate $\frac{f_{max}}{f_{min}}$ from the equation $\frac{f_{max}}{f_{min}} = \frac{f_o + f_L}{f_o - f_L}$
– Use $\frac{f_{max}}{f_{min}}$ with Fig.5c to determine ratio R2/R1 to obtain R1</td><td>– Given: f_{max}
– Calculate f_o from the equation $f_o = \frac{f_{max}}{2}$
– Use f_o with Fig.5a to determine R1 and C1</td><td>– Given: f_{min} & f_{max}
– Use f_{min} with Fig.5b to determine R2 and C1
– Calculate $\frac{f_{max}}{f_{min}}$
– Use $\frac{f_{max}}{f_{min}}$ with Fig.5c to determine ratio R2/R1 to obtain R1</td></tr>
</table>

REF. G. S. Moschytz, "Miniaturized RC Filters Using Phase-Locked Loop", BSTJ, May, 1965.

ELECTRICAL CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2] Min.	T_{LOW} [2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH} [2] Min.	T_{HIGH} [2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5	Inhibit = V_{DD} Signal Input = V_{DD}	–	5	–	0.05	5	–	150	μAdc
		10		–	10	–	0.01	10	–	300	
		15		–	20	–	0.2	20	–	600	
TOTAL POWER DISSIPATION	P_T	5	Inh = V_{SS}, $VCO_{IN} = \frac{V_{DD}}{2}$, f_o = 10kHz, C_L = 15pF, R1 = 1MΩ, R2 = R_S = ∞	–	–	–	0.07	–	–	–	mW
		10		–	–	–	0.6	–	–	–	
		15		–	–	–	2.4	–	–	–	

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

PARAMETER		CONDITIONS		V_{DD}	25°C Min.	25°C Typ.	25°C Max.	UNIT
VCO SECTION								
MAXIMUM OPERATING FREQUENCY 4046B	f_{max}	R2 = ∞ VCO_{IN} = V_{DD}	R1 C1: 10k 50pF	5	0.5	0.8	–	MHz
				10	1.0	1.5	–	
				15	1.3	1.9	–	
			5k 50pF	5	0.6	1.0	–	MHz
				10	1.4	2.1	–	
				15	1.8	2.7	–	
			2k 50pF	5	–	1.3	–	MHz
				10	–	2.9	–	
				15	–	3.8	–	
4446B		R2 = ∞ VCO_{IN} = V_{DD}	R1 C1: 10k 50pF	5	0.7	1.0	–	MHz
				10	1.3	2.0	–	
				15	1.9	2.8	–	
			5k 50pF	5	0.9	1.3	–	MHz
				10	1.9	2.9	–	
				15	2.6	3.9	–	
			2k 50pF	5	–	1.8	–	MHz
				10	–	3.9	–	
				15	–	5.4	–	
LINEARITY		R2 = ∞ VCO_{IN} = 2.5±0.3V, R1 ⩾ 10kΩ		5	–	1	–	%
		VCO_{IN} = 5.0±2.5V, R1 ⩾ 400kΩ		10	–	1	–	
		VCO_{IN} = 7.5±5.0V, R1 ⩾ 1MΩ		15	–	1	–	
INPUT CAPACITANCE	C_{IN}	Pin 14 Only		–	–	–	10	pF
		All Other Inputs		–	–	–	7.5	

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER		CONDITIONS	V_{DD}	+25°C Min.	Typ.	Max.	UNIT
VCO SECTION (Continued)							
TEMPERATURE-FREQUENCY STABILITY No Offset		R2 = ∞	5 10 15	– – –	0.12-0.24 0.04-0.08 0.015-0.03	– – –	%/°C
With Offset		R2⩽ 10X R1	5 10 15	– – –	0.06-0.12 0.05-0.1 0.03-0.06	– – –	%/°C
INPUT RESISTANCE (VCO_{IN})	R_{IN}		5, 10, 15	–	10^6	–	MΩ
OUTPUT DUTY CYCLE		All valid input combinations and voltages		–	50	—	%
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	C_L = 50pF	5 10 15	– – –	100 50 40	200 100 80	ns
PHASE COMPARATORS							
INPUT RESISTANCE Signal Input	R_{IN}		5 10 15	1 0.2 0.1	3 0.7 0.3	– – –	MΩ
Comparator Input	R_{IN}		5, 10, 15	–	10^6	–	MΩ
AC-COUPLED INPUT SENSITIVITY Signal Input	V_{IN}		5 10 15	– – –	200 400 700	400 800 1400	mV
OUTPUT TRANSITION TIME PCI, PCII Outputs	t_{TLH}, t_{THL}	C_L = 50pF	5 10 15	– – –	100 50 40	200 100 80	ns
Phase Pulses Output	t_{TLH}, t_{THL}		5 10 15	– – –	130 65 50	260 130 100	ns
DEMODULATOR OUTPUT							
OFFSET VOLTAGE	VCO_{IN}-V_{DEM}	R_S⩾50kΩ	5 10 15	– – –	1.4 1.6 1.8	2.2 2.2 2.2	Vdc
LINEARITY		R_S⩾50kΩ VCO_{IN} = 2.5±0.3V VCO_{IN} = 5.0±2.5V VCO_{IN} = 7.5±5.0V	 5 10 15	 – – –	 0.1 0.6 0.8	 – – –	%
ZENER DIODE							
ZENER VOLTAGE	V_Z	I_Z = 50μA	–	6.3	7.0	7.7	V
DYNAMIC RESISTANCE	R_Z	I_Z = 1mA	–	–	100	–	Ω

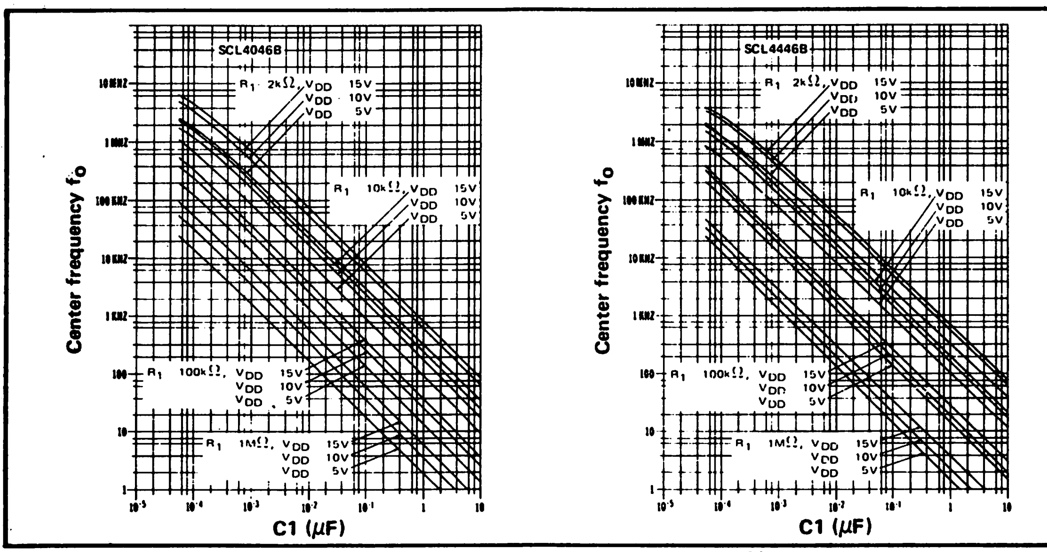


Fig. 5 (a) Typical center frequency (f_O) vs C1 (R2 = ∞, $VCO_{IN} = \frac{V_{DD}}{2}$, T_A = 25°C)

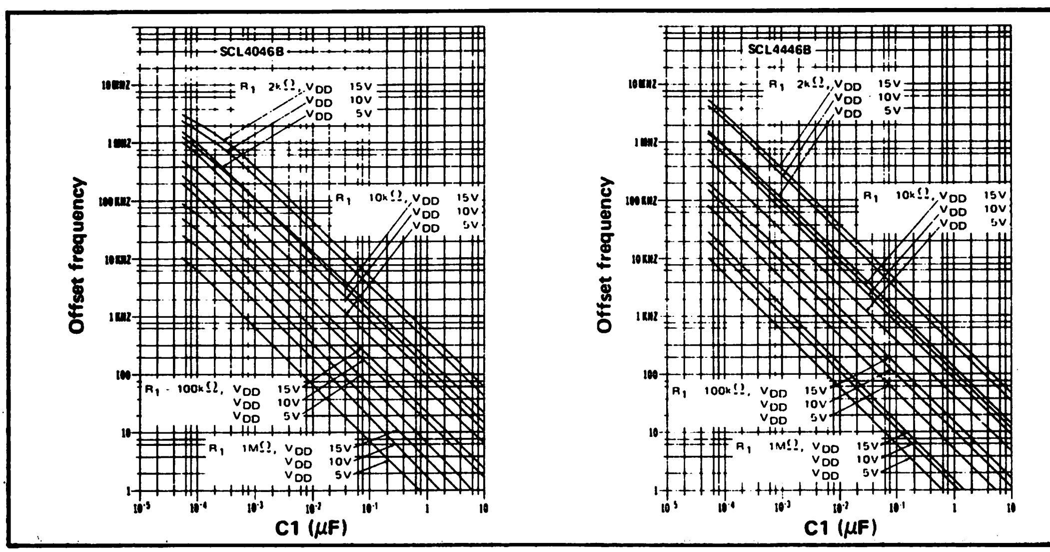


Fig. 5 (b) Typical frequency offset vs C1 ($VCO_{IN} = V_{SS}$, T_A = 25°C)

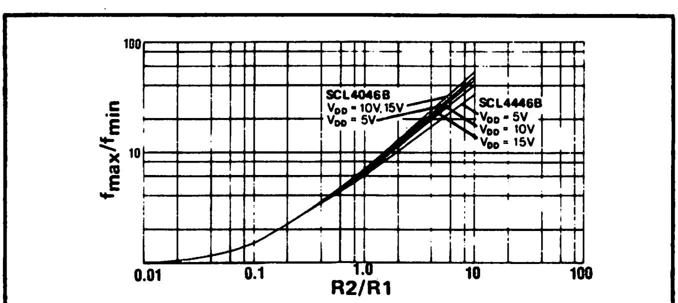


Fig. 5 (c) Typical f_{max}/f_{min} vs R2/R1

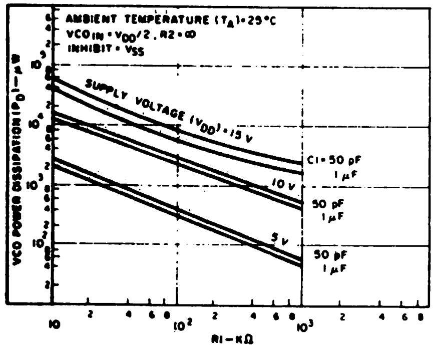


Fig. 6 (a) - Typical VCO power dissipation at center frequency vs R1.

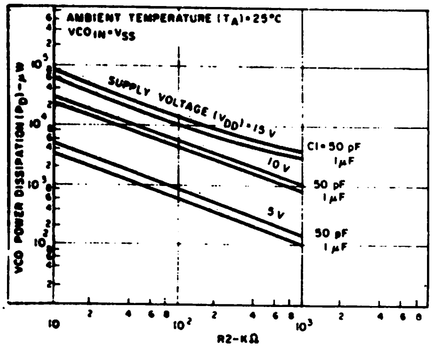


Fig. 6 (b) - Typical VCO power dissipation at f_{min} vs R2.

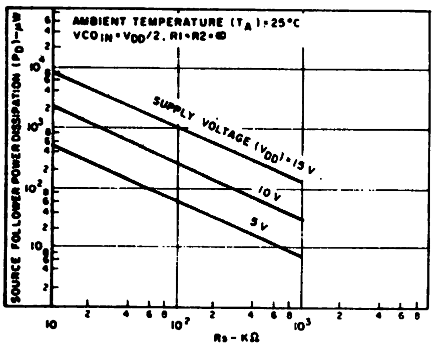


Fig. 6 (c) - Typical source follower power dissipation vs R_S.

NOTE: To obtain approximate total power dissipation of PLL system for no-signal input

P_D (Total) = $P_D(f_o) + P_D(f_{MIN}) + P_D(R_S)$
– Phase Comparator I

P_D (Total) = $P_D(f_{MIN})$
– Phase Comparator II

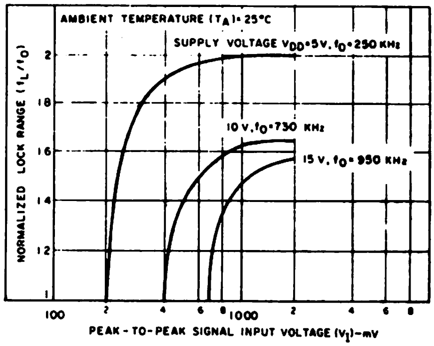
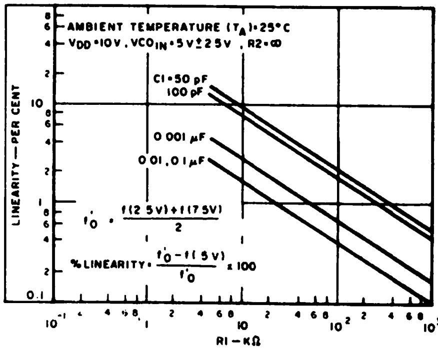


Fig. 7 — Typical lock range vs signal input amplitude



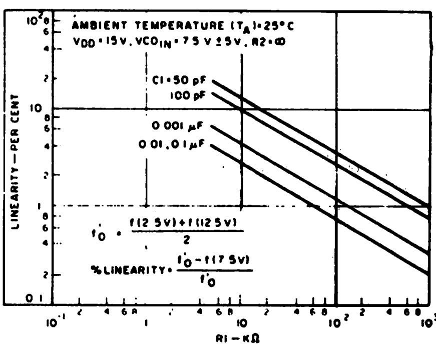


Fig. 8(a, b) — Typical VCO linearity vs R1 and C1

SOLID STATE SCIENTIFIC

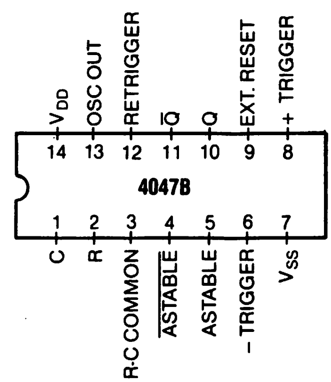
SCL4047B

CMOS MONOSTABLE/ASTABLE MULTIVIBRATOR

FEATURES

- Low Power Consumption
- Monostable (one-shot) or (Astable) Operation
- True and Complementary Buffered Outputs
- Only One External R and C Required
- Enabled with either a Low or a High Level in Astable Mode
- Triggered on either a Low to High or High to Low Transition in Monostable Mode
- Asynchronous Master Reset
- Output Pulse Width Independent of Trigger Pulse, in Monostable Mode
- May Be Utilized as Free Running or Gated Oscillator, in Astable Mode

CONNECTION DIAGRAM



DESCRIPTION

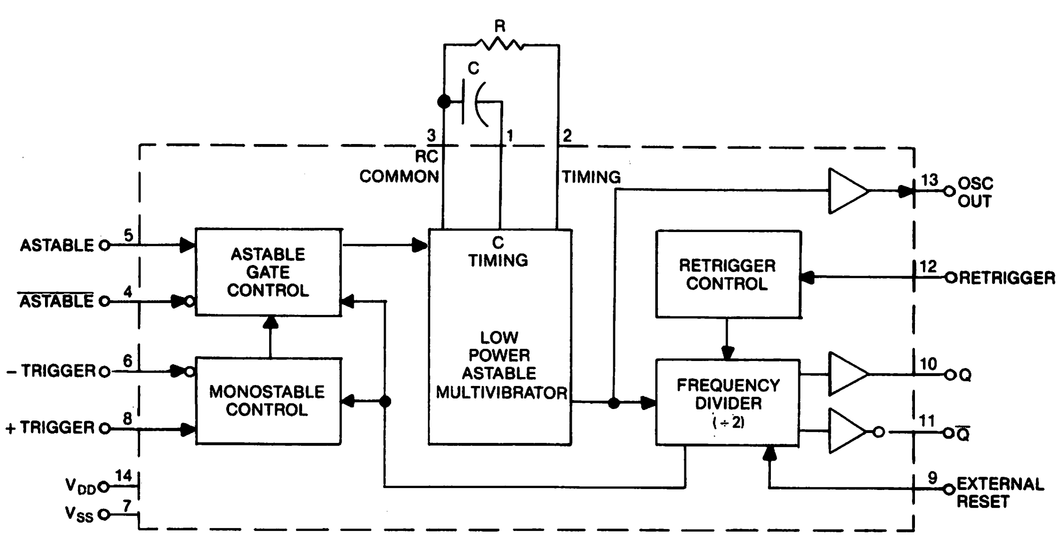
4047B is capable of operating in either the monostable or astable mode. It requires an external capacitor (between pins 1 and 3) and an external resistor (between pins 2 and 3) to determine the output pulse width in the monostable mode, and the output frequency in the astable mode.

Astable operation is enabled by a high level on the astable input or low level on the $\overline{\text{astable}}$ input. The output frequency (at 50% duty cycle) at Q and $\overline{Q}$ outputs is determined by the timing components. A frequency twice that of Q is available at the Oscillator Output; a 50% duty cycle is not guaranteed.

Monostable operation is obtained when the device is triggered by low-to-high transition at + trigger input or high-to-low transition at —trigger input. The device can be retriggered by applying a simultaneous low-to-high transition to both the + trigger and retrigger inputs.

A high level on Reset input resets the outputs Q to low, $\overline{Q}$ to high.

BLOCK DIAGRAM



Absolute Maximum Ratings

V_{DD} DC Supply Voltage	-0.5 to $+18V_{DC}$
V_{IN} Input Voltage	-0.5 to V_{DD} $+0.5V_{DC}$
T_S Storage Temperature Range	$-65°C$ to $+150°C$
P_D Package Dissipation	500mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

V_{DD} DC Supply Voltage	3 to $15V_{DC}$
V_{IN} Input Voltage	0 to $V_{DD}V_{DC}$
T_A Operating Temperature Range	
SCL4047BC, D, F, H	$-55°C$ to $+125°C$
SCL4047BE	$-40°C$ to $+85°C$

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS [1]

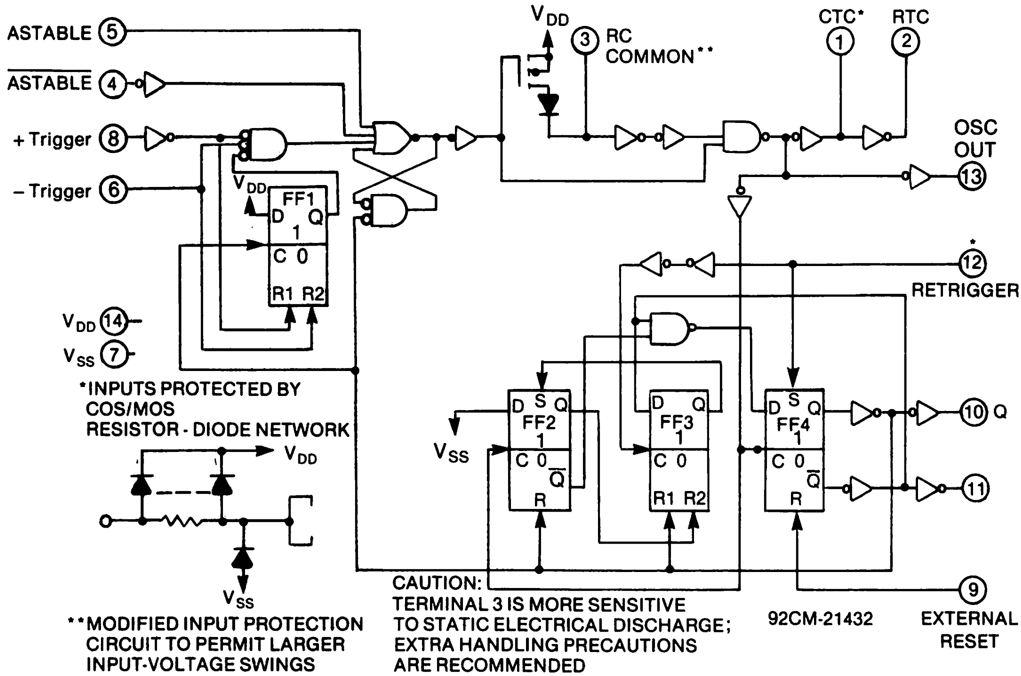
PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2]		+25°C			T_{HIGH} [2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN}=V_{SS}$ or V_{DD}	–	1.0	–	0.0005	1.0	–	30	μAdc
		10	All valid input	–	2.0	–	0.001	2.0	–	60	
		15	combinations	–	4.0	–	0.002	4.0	–	120	

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

AC ELECTRICAL CHARACTERISTICS

$T_A = 25°C, C_L = 50\,pF$

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}, t_{PLH}	Propagation Delay Time Astable, Astable to OSC Out	V_{DD} = 5V		200	400	ns
		V_{DD} = 10V		100	200	ns
		V_{DD} = 15V		80	160	ns
t_{PHL}, t_{PLH}	Astable, Astable to Q Q	V_{DD} = 5V		550	900	ns
		V_{DD} = 10V		250	500	ns
		V_{DD} = 15V		200	400	ns
t_{PHL}, t_{PLH}	+ Trigger, – Trigger to Q Q	V_{DD} = 5V		700	1200	ns
		V_{DD} = 10V		300	600	ns
		V_{DD} = 15V		240	480	ns
t_{PHL}, t_{PLH}	+ Trigger, Retrigger to Q Q	V_{DD} = 5V		300	600	ns
		V_{DD} = 10V		175	300	ns
		V_{DD} = 15V		150	250	ns
t_{PHL}, t_{PLH}	Reset to Q Q	V_{DD} = 5V		300	500	ns
		V_{DD} = 10V		125	250	ns
		V_{DD} = 15V		100	200	ns
t_{THL}, t_{TLH}	Transition Time Q, Q, OSC Out	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{WL}, t_{WH}	Minimum Input Pulse Duration	Any Input				
		V_{DD} = 5V		500	1000	ns
		V_{DD} = 10V		200	400	ns
		V_{DD} = 15V		160	320	ns
t_{RCL}, t_{FCL}	+ Trigger, Retrigger, Rise and Fall Time	V_{DD} = 5V			15	μs
		V_{DD} = 10V			5	μs
		V_{DD} = 15V			5	μs
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF

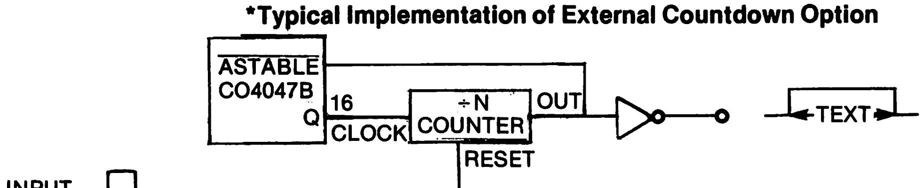


TRUTH TABLE

FUNCTION	TERMINAL CONNECTIONS TO V_{DD}	TO V_{SS}	INPUT PULSE TO	OUTPUT PULSE FROM	TYPICAL OUTPUT PERIOD OR PULSE WIDTH
Astable Multivibrator					
Free-Running	4, 5, 6, 14	7, 8, 9, 12		10, 11, 13	$t_A(10, 11) = 4.40$ RC
True Gating	4, 6, 14	7, 8, 9, 12	5	10, 11, 13	
Complement Gating	6, 14	5, 7, 8, 9, 12	4	10, 11, 13	$t_A(13) = 2.20$ RC
Monostable Multivibrator					
Positive-Edge Trigger	4, 14	5, 6, 7, 9, 12	8	10, 11	
Negative-Edge Trigger	4, 8, 14	5, 7, 9, 12	6	10, 11	$t_M(10, 11) = 2.48$ RC
Retriggerable	4, 14	5, 6, 7, 9	8, 12	10, 11	
External Countdown*	14	5, 6, 7, 8, 9, 12	(See Figure)	(See Figure)	(See Figure)

Note: External resistor between terminals 2 and 3. External capacitor between terminals 1 and 3.

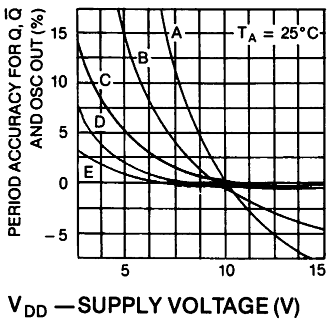
*Typical Implementation of External Countdown Option



$t_{EXT} = (N - 1)\,t_A + (t_M + t_A/2)$

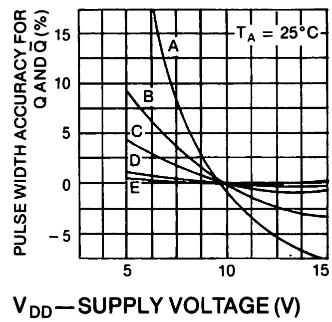
TYPICAL PERFORMANCE CHARACTERISTICS

Typical Q, $\bar{Q}$, Osc Out Period
Accuracy vs Supply Voltage
(Astable Mode Operation)



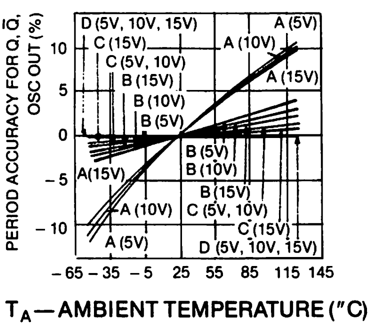
	$f_{Q,\bar{Q}}$	R	C
A	1000 kHz	22k	10 pF
B	100 kHz	22k	100 pF
C	10 kHz	220k	100 pF
D	1 kHz	220k	1000 pF
E	100 Hz	2.2M	1000 pF

Typical Q, $\bar{Q}$, Pulse Width
Accuracy vs Supply Voltage
Monostable Mode Operation



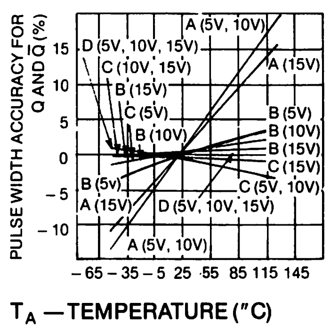
	t_M	R	C
A	2μs	22K	10 pF
B	7μs	22k	100 pF
C	60μs	220k	100 pF
D	550μs	220k	1000 pF
E	5.5ms	2.2M	1000 pF

Typical Q, $\bar{Q}$ and Osc Out
Period Accuracy vs Temperature
Astable Mode Operation



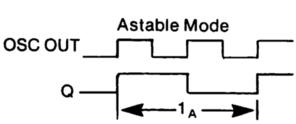
	$f_{Q,\bar{Q}}$	R	C
A	1000 kHz	22k	10 pF
B	100 kHz	22k	100 pF
C	10 kHz	220k	100 pF
D	1 kHz	220k	1000 pF

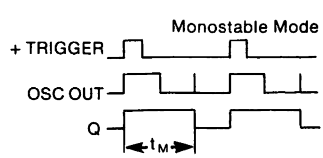
Typical Q and $\bar{Q}$ Pulse Width
Accuracy vs Temperature
Monostable Mode Operation

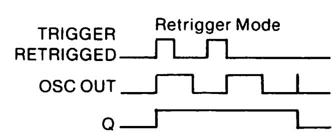


	t_M	R	C
A	2μs	22K	10 pF
B	7μs	22k	100 pF
C	60μs	220k	100 pF
D	550μs	220k	1000 pF

TIMING DIAGRAMS







SOLID STATE SCIENTIFIC

SCL4049UB
SCL4050B

CMOS HEX BUFFERS/CONVERTERS

FEATURES

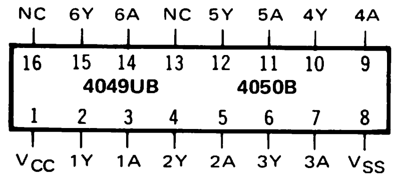
- ◆ Direct Drive of 2 TTL/DTL Loads
- ◆ Operation from Single Supply
- ◆ Pin-for Pin Replacements for 4009UB 4010B

DESCRIPTION

The 4049UB and 4050B are Inverting and Non-Inverting Hex Buffers, respectively, and feature logic-level conversions using only one supply voltage (V_{CC}). The Input-signal high level (V_{IH}) can exceed the V_{CC} supply voltage when these devices are used for logic-level conversions. These devices are intended for use as CMOS-to-DTL/TTL converters and can drive directly two DTL/TTL Loads.

The 4049UB and 4050B are interchangeable with 4009 UB and 4010B devices, respectively. In these applications the 4049UB and 4050B are pin-compatible with the 4009UB and 4010B, respectively, and can be substituted for these devices in existing as well as in new designs. Terminal No. 16 is not connected internally on the 4049UB or 4050B; therefore, connection to this terminal is of no consequence to circuit operation.

CONNECTION DIAGRAM
(all packages)



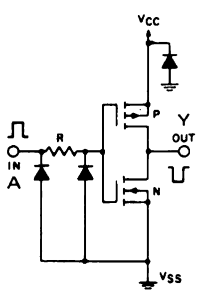
RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

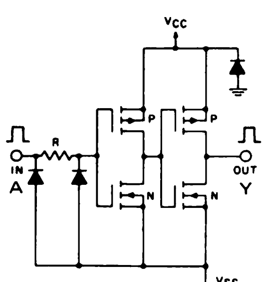
DC Supply Voltage	$V_{CC} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

Note: These devices contain input protection networks to V_{SS} only. Therefore, V_{IH} (max) may exceed V_{CC} without damage (subject to absolute maximum ratings).

SCHEMATIC DIAGRAMS

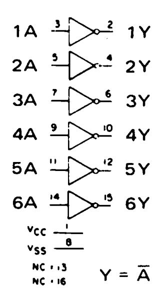


4049UB

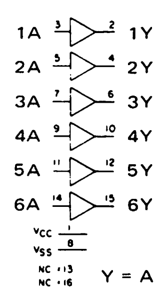


4050B

LOGIC DIAGRAMS



4049UB



4050B

ELECTRICAL CHARACTERISTICS

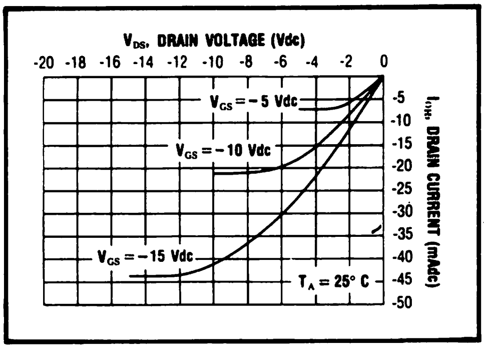
STATIC CHARACTERISTICS [1]

PARAMETER		Vcc (Vdc)	CONDITIONS	T_{LOW} [2] Min.	T_{LOW} [2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH} [2] Min.	T_{HIGH} [2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{CC}	5 10 15	$V_{IN}=V_{SS}$ or V_{DD} All valid input combinations	– – –	1.0 2.0 4.0	– – –	0.005 0.01 0.02	1.0 2.0 4.0	– – –	30 60 120	μAdc
OUTPUT LOW (SINK) CURRENT	I_{OL}	5 10 15	V_{OL}=0.4V V_{OL}=0.5V V_{OL}=1.5V $V_{IN}=V_{SS}$ or V_{DD}	3.7 10 30	– – –	3.0 8.0 24.0	6.4 16 40	– – –	2.1 5.6 16.8	– – –	mAdc

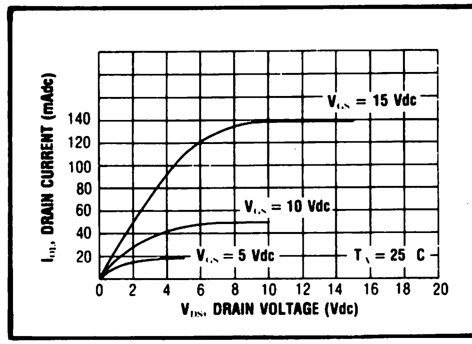
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

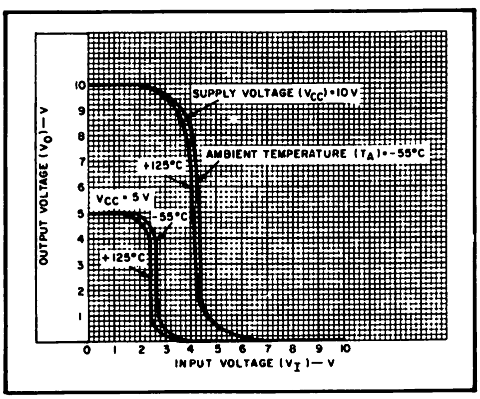
PARAMETER		V_{IN} (Vdc)	Vcc (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME 4049UB	t_{PLH}	5 10 15	5 10 15	– – –	60 32 25	120 65 50	ns
		10 15	5 5	– –	45 45	90 90	ns
4050B		5 10 15	5 10 15	– – –	70 40 30	140 80 60	ns
		10 15	5 5	– –	45 40	90 80	ns
4049UB	t_{PHL}	5 10 15	5 10 15	– – –	32 20 15	65 40 30	ns
		10 15	5 5	– –	15 10	30 20	ns
4050B		5 10 15	5 10 15	– – –	55 27 15	110 55 30	ns
		10 15	5 5	– –	50 50	100 100	ns
OUTPUT TRANSITION TIME	t_{TLH}	5 10 15	5 10 15	– – –	80 40 30	160 80 60	ns
	t_{THL}	5 10 15	5 10 15	– – –	30 20 15	60 40 30	ns
INPUT CAPACITANCE 4049UB	C_{IN}	–	–	–	15	22.5	pF



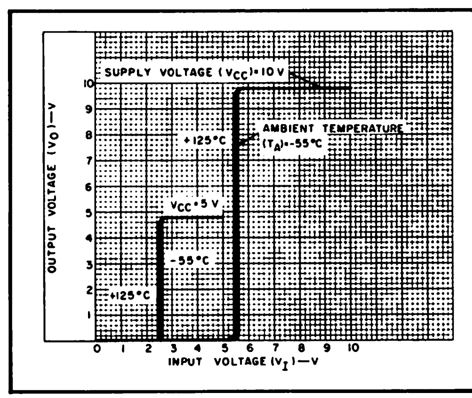
Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics



Typical voltage transfer characteristics as a function of temperature for 4049UB.



Typical voltage transfer characteristics as a function of temperature for 4050B.

SOLID STATE SCIENTIFIC

SCL4051B
SCL4052B
SCL4053B

CMOS ANALOG MULTIPLEXERS/DEMULTIPLEXERS

FEATURES

- **Wide Range of Digital and Analog Signal Levels: Digital-3 to 15V, Analog-to $15V_{p\text{-}p}$**
- **Low ON-Resistance: 80Ω (typ.) over entire $15V_{p\text{-}p}$ Signal-Input Range for $V_{DD}\text{-}V_{EE}$ = 15V**
- **High OFF-Resistance: Input Leakage ± 10pA (typ) @ $V_{DD}\text{-}V_{EE}$ = 10V**
- **Logic-Level Conversion for Digital Addressing Signals of 3 to 15V ($V_{DD}\text{-}V_{SS}$= 3V to 15V) to Switch Analog Signals to $15V_{p\text{-}p}$ ($V_{DD}\text{-}V_{EE}$ = 15V)**
- **Matched Switch Characteristics: ΔR_{ON} = 5Ω (typ.) for $V_{DD}\text{-}V_{EE}$ = 18V**
- **Very Low Quiescent Power Dissipation under all Digital Control Input and Supply Conditions: 1μW typ. @ $V_{DD}\text{-}V_{SS}$ = $V_{DD}\text{-}V_{EE}$ = 10V**
- **Binary Address Decoding on Chip**

DESCRIPTION

The 4051B, 4052B, and 4053B are Digitally-Controlled Analog Switches having low ON-impedance and very low OFF leakage current. Control of analog signals up to $15V_{p\text{-}p}$ can be achieved by digital signal amplitudes of 3 to 15V. For example, if V_{DD} = +5V, V_{SS} = 0V, and V_{EE} = -5V, analog signals from -5V to +5V can be controlled by digital inputs of 0 to 5V. The multiplexer circuits dissipate extremely low quiescent power over the full V_{DD} - V_{SS} and V_{DD} - V_{EE} supply-voltage ranges, independent of the logic state of the control signals. When a logic "1" is present at the Inhibit input terminal all channels are OFF.

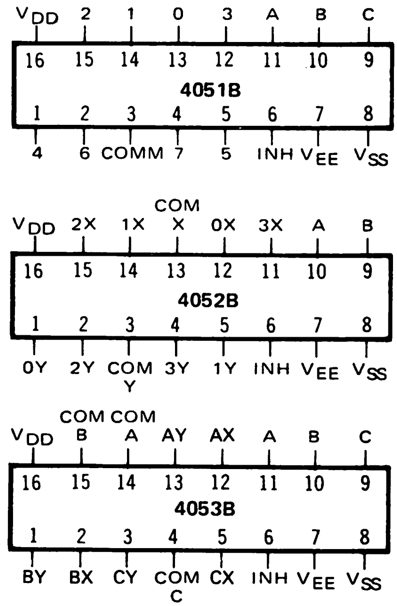
4051B is a Single 8-Channel Multiplexer having three binary Control inputs, A, B, and C, and an Inhibit input. The three binary signals select 1 of 8 channels to be turned ON and connect the input to the output.

4052B is a Differential 4-Channel Multiplexer having two binary Control inputs, A and B, and an Inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the differential analog inputs to the differential outputs.

4053B is a Triple 4-Channel Multiplexer having three separate digital Control inputs, A, B, and C and an Inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole double-throw configuration.

When the devices are used as demultiplexers, the "CHANNEL IN/OUT" terminals are the outputs and the "COMMON OUT/IN" terminal(s) is (are) the input(s).

CONNECTION DIAGRAMS
(all packages)



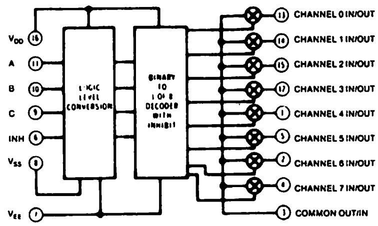
RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

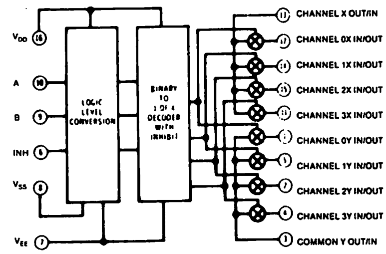
DC Supply Voltage	V_{DD} - V_{SS}	3 to 15	Vdc
	V_{DD} - V_{EE}	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

NOTE: There are no restrictions on the relative magnitudes of V_{SS} and V_{EE}, providing Absolute Maximum Ratings are observed.

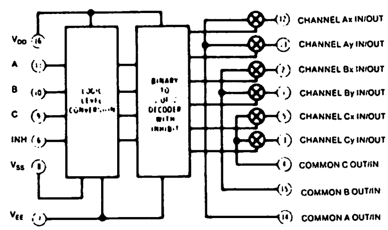
LOGIC DIAGRAMS



4051B
Single 8-Channel Multiplexer



4052B
Differential 4-Channel Multiplexer



4053B
Triple 2-Channel Multiplexer

TRUTH TABLE

INPUT STATES				"ON" CHANNELS		
INHIBIT	C	B	A	4051	4052	4053
0	0	0	0	0	Ox, Oy	cx, bx, ax
0	0	0	1	1	1x, 1y	cx, bx, ay
0	0	1	0	2	2x, 2y	cx, by, ax
0	0	1	1	3	3x, 3y	cx, by, ay
0	1	0	0	4		cy, bx, ax
0	1	0	1	5		cy, bx, ay
0	1	1	0	6		cy, by, ax
0	1	1	1	7		cy, by, ay
1	*	*	*	NONE	NONE	NONE

* = Don't care

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS [1]

PARAMETER		CONDITIONS	V_{SS} (Vdc)	V_{DD} (Vdc)	V_{EE} (Vdc)	T_{LOW} [2] Min.	T_{LOW} [2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH} [2] Min.	T_{HIGH} [2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	$V_{IN}=V_{SS}$ or V_{DD} All valid input combinations	0	+5	0	–	5	–	0.05	5	–	150	μAdc
			0	+10	0	–	10	–	0.1	10	–	300	
				+5	-5								
			0	+15	0	–	20	–	0.2	20	–	600	
				+7.5	-7.5								
MINIMUM INPUT HIGH VOLTAGE (Control and Inhibit Inputs)	V_{IH}	$V_{is}=V_{EE}$ $V_{os}=V_{DD}$ $I_{os}=10\mu A$	0	5	0	–	3.5	–	2.75	3.5	–	3.5	Vdc
			0	10	0	–	7.0	–	5.5	7.0	–	7.0	
			0	15	0	–	11.0	–	8.25	11.0	–	11.0	
MAXIMUM INPUT LOW VOLTAGE (Control and Inhibit Inputs)	V_{IL}	$V_{is}=V_{EE}$ $V_{os}=V_{DD}$ $I_{os}=10\mu A$	0	5	0	1.5	–	1.5	2.25	–	1.5	–	Vdc
			0	10	0	3.0	–	3.0	4.5	–	3.0	–	
			0	15	0	4.0	–	4.0	6.75	–	4.0	–	
SWITCH INPUT/ OUTPUT LEAKAGE Any channel OFF	I_{OFF}	$V_{IN}=V_{SS}$ or V_{DD} $V_{is}=\pm 7.5$Vdc	0	+7.5	-7.5	–	±100	–	±0.01	±100	–	± 1000	nAdc
All channels OFF	I_{OFF}	Inh = 7.5Vdc $V_{is}=\pm 7.5$Vdc	0	+7.5	-7.5								
		4051B				–	±400	–	±0.08	±400	–	±1000	nAdc
		4052B				–	±200	–	±0.04	±200	–	±1000	
		4053B				–	±100	–	±0.02	±100	–	±1000	
ON-RESISTANCE	R_{ON}	$V_{IN}=V_{SS}$ or V_{DD} $V_{EE}\leqslant V_{is}\leqslant V_{DD}$ $R_L=10k\Omega$	-7.5	+7.5	-7.5								
			0	+15	0	–	220	–	125	280	–	400	Ω
			-5	+5	-5	–	310	–	180	400	–	590	Ω
			0	+10	0								
			-2.5	+2.5	-2.5	–	2000	–	470	2500	–	3500	Ω
			0	+5	0								
ON-RESISTANCE MATCH (Same Package)	ΔR_{ON}	$V_{IN}=V_{SS}$ or V_{DD} $V_{EE}\leqslant V_{is}\leqslant V_{DD}$ $R_L=10k\Omega$	-7.5	+7.5	-7.5	–	–	–	5	–	–	–	Ω
			0	+15	0								
			-5	+10	-5	–	–	–	10	–	–	–	Ω
			0	+10	0								
			-2.5	+2.5	-2.5	–	–	–	50	–	–	–	Ω
			0	+5	0								

NOTES: [1] Remaining Static Characteristics are listed under "4000B Series Family Specifications".

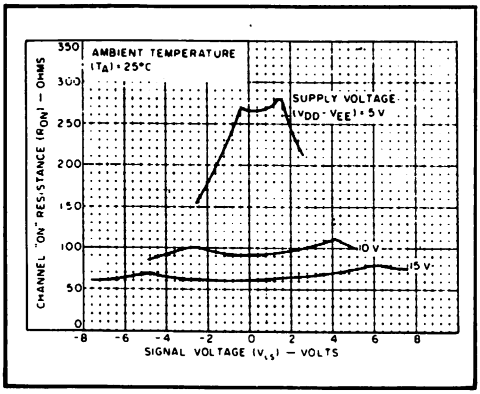
[2] In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into terminals 1, 4, 8, or 11, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from R_{ON} values shown).
No V_{DD} current will flow through R_L if the switch current flows into terminals 2, 3, 9, or 10. Failure to observe this condition may result in distortion of the signal.

ELECTRICAL CHARACTERISTICS (Continued)

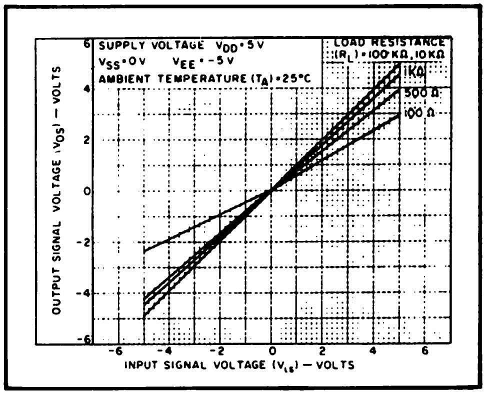
DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		CONDITIONS	V_{SS} (Vdc)	V_{DD} (Vdc)	V_{EE} (Vdc)	Min.	Typ.	Max.	Units
SIGNAL INPUTS (V_{is}) AND OUTPUTS (V_{os})									
PROPAGATION DELAY TIME Signal Input to Signal Output	t_{PLH} t_{PHL}	Inh = V_{SS} V_{IN}=V_{SS} or V_{DD} V_{is}= Square Wave R_L = 10kΩ	0	5	0	–	30	60	ns
			0	10	0	–	15	30	
			0	15	0	–	12.5	25	
BANDWIDTH (-3dB) (Sine Wave)	BW	Inh = V_{SS}, V_{IN} = V_{SS} or V_{DD}, V_{is}=5$V_{p\text{-}p}$ centered @ 0.0Vdc; R_L = 1kΩ	0	+5	-5	–	54	–	MHz
		R_L = 10kΩ				–	40	–	
		R_L = 100kΩ				–	38	–	
		R_L = 1MΩ				–	37	–	
INSERTION LOSS $(= 20 \log_{10} \frac{V_{os}}{V_{is}})$		Inh = V_{SS}, V_{IN}=V_{SS} or V_{DD}, V_{is}=5$V_{p\text{-}p}$ centered @ 0.0Vdc; R_L = 1kΩ	0	+5	-5	–	2.3	–	dB
		R_L = 10kΩ				–	0.2	–	
		R_L = 100kΩ				–	0.1	–	
		R_L = 1MΩ				–	0.05	–	
SIGNAL DISTORTION (Sine Wave)		Inh = V_{SS} V_{IN} = V_{SS} or V_{DD} V_{is} = 5$V_{p\text{-}p}$ centered @ 0.0Vdc f_{is} = 1.0kHz R_L = 10kΩ	-7.5	+7.5	-7.5	–	0.1	–	%
			-5	+5	-5	–	0.2	–	
			-2.5	+2.5	-2.5	–	1.0	–	
FEEDTHROUGH (-40dB)		Inh = V_{SS}, V_{IN}=V_{SS} or V_{DD}, V_{is}=5$V_{p\text{-}p}$ centered @0.0Vdc; R_L = 1kΩ	0	+5	-5	–	1250	–	kHz
		R_L = 10kΩ				–	140	–	
		R_L = 100kΩ				–	18	–	
		R_L = 1MΩ				–	2	–	
CROSSTALK (-40dB) Between two switches		Inh = V_{SS} V_{IN}= V_{SS} or V_{DD} V_{is}= 5$V_{p\text{-}p}$ centered @ 0.0Vdc R_L = 1.0kΩ	0	+5	-5	–	1.0	–	MHz
CAPACITANCE Input	C_{is}	Inh = V_{DD}	0	+5	-5	–	5	–	pF
Common	C_{os}	4051B	0	+5	-5	–	30	–	pF
		4052B				–	18	–	
		4053B				–	10	–	
Feedthrough	C_{ios}		0	+5	-5	–	0.2	–	pF
CONTROL INPUTS									
PROPAGATION DELAY TIME[1] Turn on	t_{PLH}, t_{PHL}	Inh = V_{SS} V_{EE}≤V_{is}≤V_{DD} R_L = 10kΩ	0	+7.5	-7.5	–	160	320	ns
			0	+15	0	–	120	240	
			0	+5	-5	–	225	450	
			0	+10	0	–	160	320	
			-2.5	+2.5	-2.5	–	400	800	
			0	+5	0	–	360	720	
INHIBIT INPUT									
PROPAGATION DELAY TIME Turn on	t_{PLH}, t_{PHL}	V_{IN}=V_{SS} or V_{DD} V_{is} = V_{DD} R_L = 10kΩ	0	+7.5	-7.5	–	160	320	ns
			0	+15	0	–	120	240	
			0	+5	-5	–	200	400	
			0	+10	0	–	160	320	
			-2.5	+2.5	-2.5	–	400	800	
			0	+5	0	–	360	720	
INHIBIT RECOVERY TIME[2]	t_{rel}	V_{IN}=V_{SS} or V_{DD} V_{EE} ≤ V_{is} ≤ V_{DD} R_L = 10kΩ	0	+7.5	-7.5	–	150	300	ns
			0	+15	0	–	80	160	
			0	+5	-5	–	200	400	
			0	+10	0	–	105	210	
			-2.5	+2.5	-2.5	–	300	600	
			0	+5	0	–	225	450	

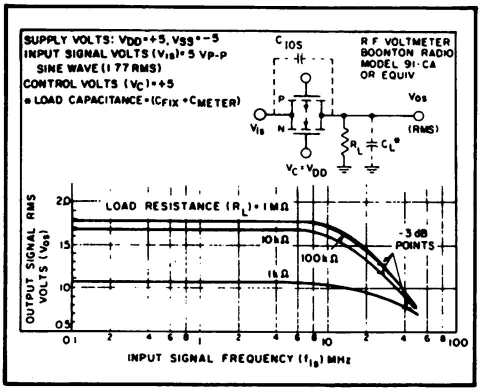
Notes: [1] Channel Overlap time – interval following change of control input during which two channels may be ON simultaneously.
[2] Interval following removal of Inhibit during which channel information is invalid.



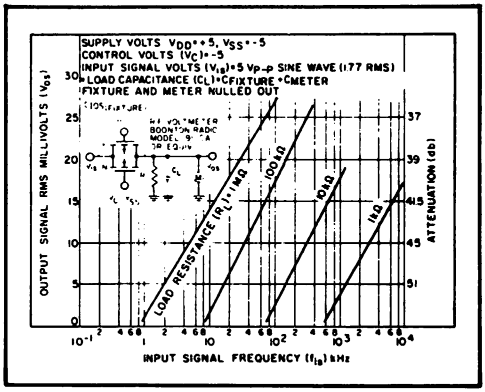
Typical Channel "ON" resistance vs. signal voltage



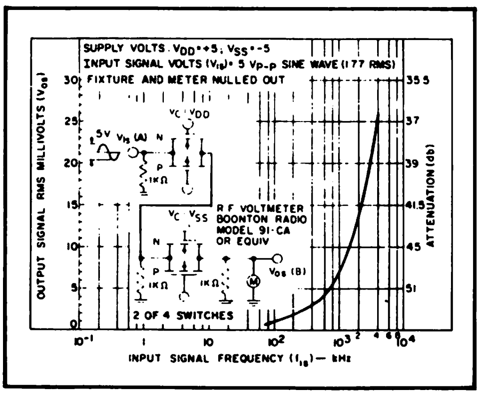
Typical "ON" characteristics



Typ. switch frequency response-switch "ON"

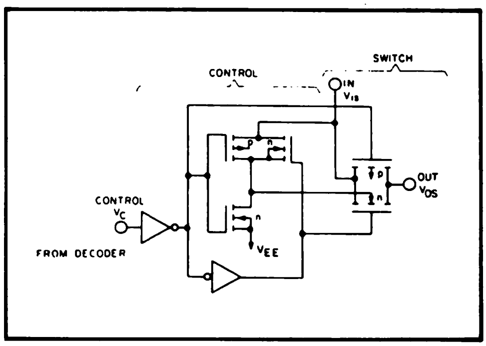


Typ. feedthru vs. freq. — switch "OFF"



Typ. crosstalk between switch circuits in the same package

SCHEMATIC DIAGRAM OF ONE SWITCH



CMOS 14-STAGE COUNTER AND OSCILLATOR

FEATURES

- 14 Fully Static Stages
- 10 Buffered Outputs Available
- Common Reset Line
- 8MHz Counting Rate @ 10Vdc
- All Active Oscillator Components on Chip for R-C or Crystal Control

DESCRIPTION

The 4060 B consists of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either R-C or crystal oscillator circuits. A Reset input is provided which resets the counter to the all-0's state. A high level on the Reset line accomplishes the reset function. The state of the counter is advanced one step in binary order on the negative transition of the Clock input ϕ. All inputs and outputs are fully buffered. Outputs are available from stages 4 through 10 and 12 through 14.

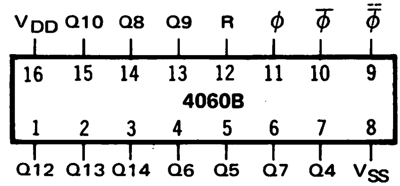
Applications include timers, frequency dividers, delay circuits and counter controls.

TRUTH TABLE

CLOCK	RESET	OUTPUT STATE
_/‾	0	No Change
‾_	0	Advance to next state
X	1	All Outputs are low

X = Don't Care

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

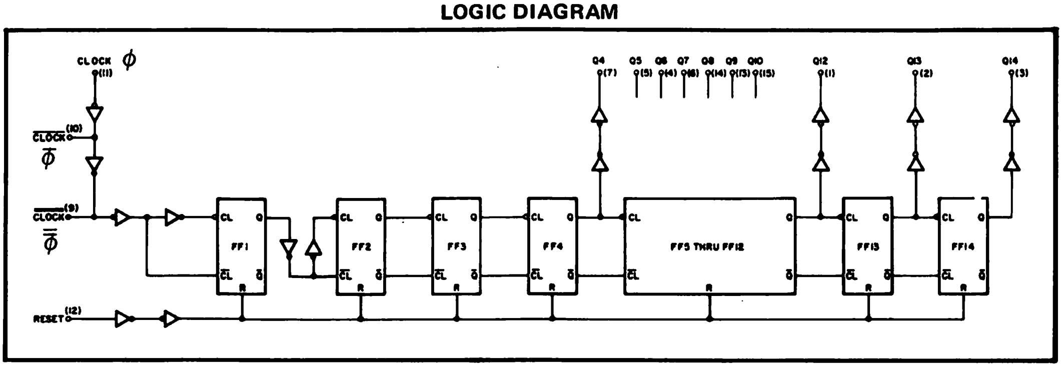
C 16-pin Cerdip
D 16-pin Ceramic
E 16-pin Epoxy
F 16-pin Flat
H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	V_O
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

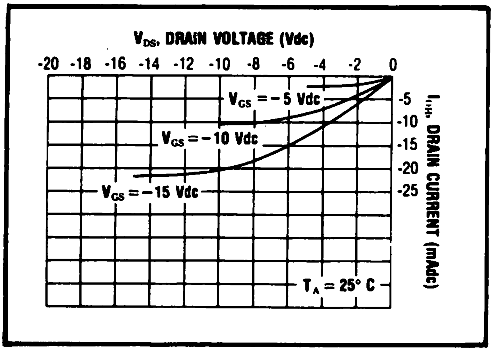
STATIC CHARACTERISTICS[1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[2]		+25°C			T_{HIGH}[2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN} = V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	μAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		15	combinations	–	20	–	0.2	20	–	600	

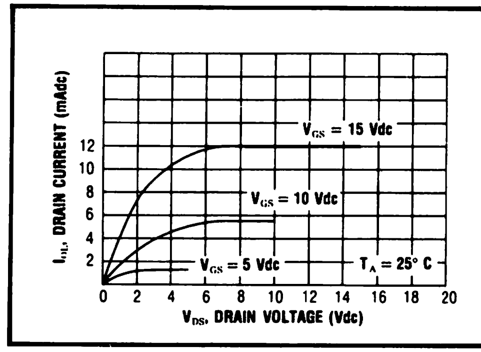
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = –55°C for C, D, F, H device.
= –40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME Clock to Q4	t_{PLH}, t_{PHL}	5	–	400	800	ns
		10	–	200	400	
		15	–	150	300	
Q_i to $Q_i + 1$	t_{PLH}, t_{PHL}	5	–	100	200	ns
		10	–	40	80	
		15	–	30	60	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	40	80	
		15	–	30	60	
MINIMUM CLOCK PULSE WIDTH	PW_{CL}	5	–	70	140	ns
		10	–	30	60	
		15	–	20	40	
MAXIMUM CLOCK FREQUENCY	f_{CL}	5	3.0	4.5	–	MHz
		10	6.0	9.0	–	
		15	7.5	11.0	–	
MAXIMUM CLOCK RISE AND FALL TIME	t_{rCL}, t_{fCL}	5	50	100	–	μs
		10	50	100	–	
		15	50	100	–	
RESET OPERATION						
PROPAGATION DELAY TIME	t_{PHL}	5	–	200	400	ns
		10	–	100	200	
		15	–	75	150	
MINIMUM RESET PULSE WIDTH	PW_R	5	–	100	200	ns
		10	–	40	80	
		15	–	30	60	
RESET REMOVAL TIME	t_{rem}	5	–	150	300	ns
		10	–	65	125	
		15	–	40	75	

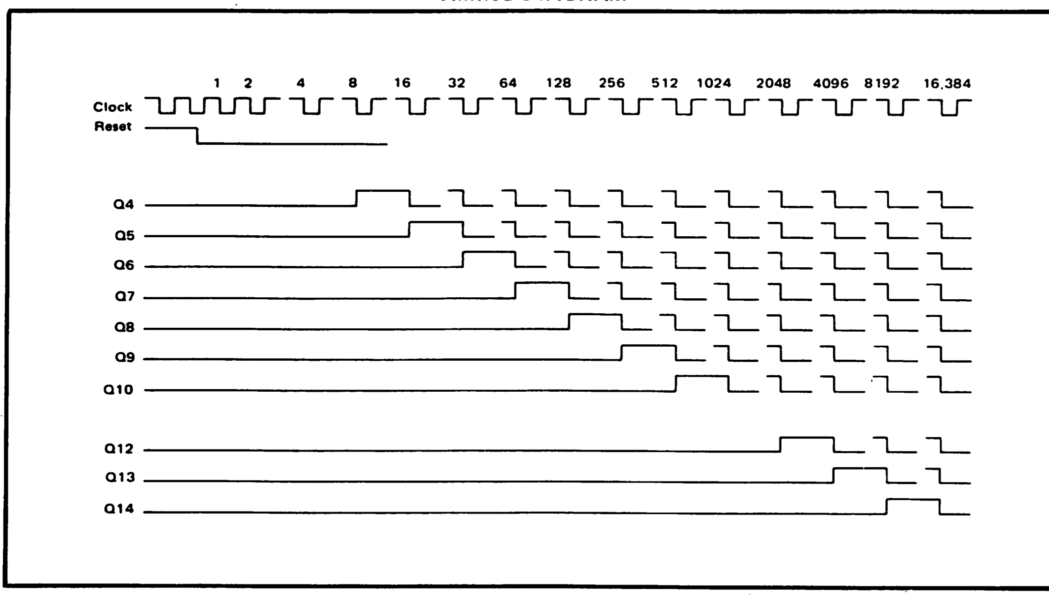


Typical P-Channel
Source Current Characteristics

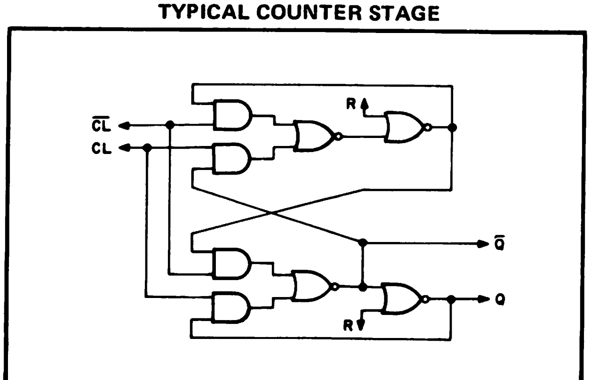


Typical N-Channel
Sink Current Characteristics

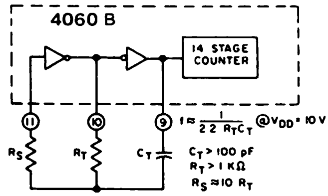
TIMING DIAGRAM



TYPICAL COUNTER STAGE



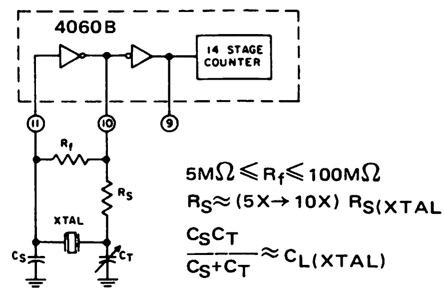
APPLICATIONS INFORMATION



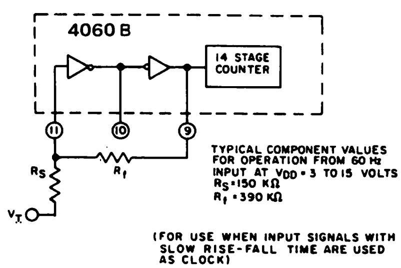
TYPICAL COMPONENT VALUES AND CIRCUIT PERFORMANCE

OSCILLATOR FREQUENCY	R_S KΩ	R_T KΩ	C_T	I_{DD} mA @ V_{DD} = 10 V
10 Hz	450	46	1 μF	0.3
100 Hz	460	46	0.1 μF	0.3
1000 Hz	450	46	0.01 μF	0.4
10 KHz	450	46	0.001 μF	0.5
100 KHz	460	46	100 pF	0.7
1 MHz	46	4.5	100 pF	1

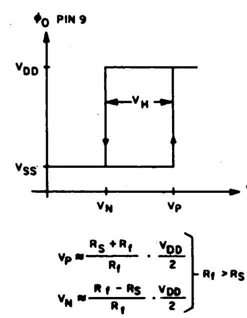
Typical RC oscillator circuit



Typical crystal oscillator circuit



Input pulse-shaping circuit (Schmitt trigger)



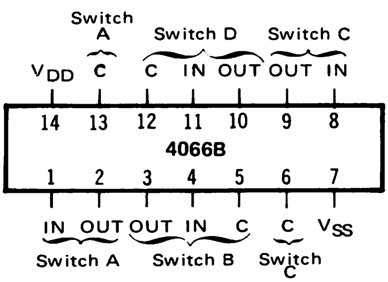
Input circuit characteristics for pulse-shaping circuit.

CMOS QUAD ANALOG SWITCH

FEATURES

- Transmission or Multiplexing of Analog or Digital Signals
- 80Ω Typical ON-Resistance for 15-Volt operation
- Switch ON-Resistance Matched to within 5Ω over 15-Volt Signal-Input Range
- ON-Resistance Flat over Full Peak-to-Peak Signal Range
- High Degree of Linearity:
  $\leqslant$0.5% Distortion (typ) @ f_{is} = 1kHz,
  $V_{is} = 5V_{p\text{-}p}$, $V_{DD}\text{-}V_{SS} \geqslant 10V$, $R_L = 10k\Omega$
- Extremely Low OFF switch Leakage Resulting in very Low Offset Current and High Effective OFF Resistance:
  10pA (typ) @ $V_{DD}\text{-}V_{SS}$= 10V, T_A= 25°C
- Extremely High Control Input Impedance (Control Circuit Isolated from Signal Circuit):
  $10^{12}\,\Omega$ (typ)
- Low Crosstalk between Switches:
  -50dB (typ) @ f_{is} = 0.9MHz, R_L = 1kΩ
- Matched Control-Input to Signal-Output Capacitance Reduces Output Signal Transients
- Frequency Response, Switch ON = 40MHz (typ)

CONNECTION DIAGRAM
(all packages)



RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

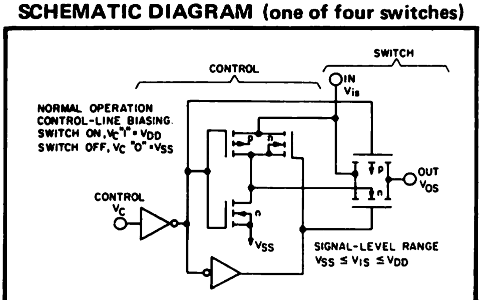
DC Supply Voltage	V_{DD} - V_{SS}	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

DESCRIPTION

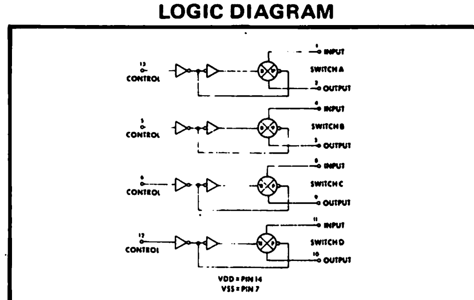
The 4066B is a Quad Bilateral Switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with the 4016B, but exhibits a much lower ON-resistance. In addition, the ON-resistance is relatively constant over the full input signal range. The 4066 consists of four independent bilateral switches. A single control signal is required per switch. Both the P and the N device in a given switch are biased ON or OFF simultaneously by the control signal. As shown below, the well of the N-channel device on each switch is either tied to the input when the switch is ON or to V_{SS} when the switch is OFF. This configuration minimizes the variation of the switch-transistor threshold voltage with input-signal, and thus keeps the ON-resistance low over the full operating range.

The advantages over single-channel switches include peak input-signal voltage swings equal to the full supply voltage, and more constant ON-impedance over the input-signal range. For sample-and-hold applications, the 4016 is recommended. When the control input is high the switch will be ON. When the control input is low the switch will be OFF.

SCHEMATIC DIAGRAM (one of four switches)



LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS

PARAMETER		CONDITIONS	V_{SS} (Vdc)	V_{DD} (Vdc)	T_{LOW}[2] Min.	T_{LOW}[2] Max.	25°C Min.	25°C Typ.	25°C Max.	T_{HIGH}[2] Min.	T_{HIGH}[2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	$V_{IN} = V_{SS}$ or V_{DD}	0	5	–	0.05	–	0.0005	0.05	–	1.5	μAdc
		All valid input	0	10	–	0.1	–	0.001	0.1	–	3.0	
		combinations	0	15	–	0.2	–	0.002	0.2	–	6.0	
MINIMUM INPUT HIGH VOLTAGE (Control Input)	V_{IH}	$V_{IS} = V_{SS}$	0	5	–	3.5	–	2.75	3.5	–	3.5	Vdc
		$V_{OS} = V_{DD}$	0	10	–	7.0	–	5.5	7.0	–	7.0	
		$I_{OS} = 10\mu A$	0	15	–	11.0	–	8.25	11.0	–	11.0	
MAXIMUM INPUT LOW VOLTAGE (Control Input)	V_{IL}	$V_{IS} = V_{SS}$	0	5	1.0	–	1.0	2.25	–	1.0	–	Vdc
		$V_{OS} = V_{DD}$	0	10	2.0	–	2.0	4.5	–	2.0	–	
		$I_{OS} = 10\mu A$	0	15	3.0	–	3.0	6.75	–	3.0	–	
SWITCH INPUT/OUTPUT LEAKAGE	I_{OFF}	$V_C = V_{SS}$, $V_{IS} = \pm 7.5Vdc$	-7.5	+7.5	–	±100	–	±0.01	±100	–	±1000	nAdc
ON-RESISTANCE	R_{ON}	$V_C = V_{DD}$	-7.5 / 0	+7.5 / +15	–	220	–	80	280	–	320	Ω
		$V_{IS} = V_{SS}/V_{DD}$, $V_{OS} = \frac{V_{DD}-V_{SS}}{2}$	-5 / 0	+5 / +10	–	400	–	120	500	–	550	Ω
		$R_L = 10k\Omega$	-2.5 / 0	+2.5 / +5	–	2000	–	270	2500	–	3500	Ω
ON-RESISTANCE MATCH (Same package)	ΔR_{ON}	$V_C = V_{DD}$	-7.5 / 0	+7.5 / +15	–	–	–	5	–	–	–	Ω
		$V_{IS} = V_{SS}/V_{DD}$, $V_{OS} = \frac{V_{DD}-V_{SS}}{2}$	-5 / 0	+5 / +10	–	–	–	10	–	–		Ω
		$R_L = 10k\Omega$	-2.5 / 0	+2.5 / +5	–	–	–	10	–	–		Ω

NOTES: [1] Remaining Static Electrical Characteristics are listed under 4000B Series Family Specifications .

[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

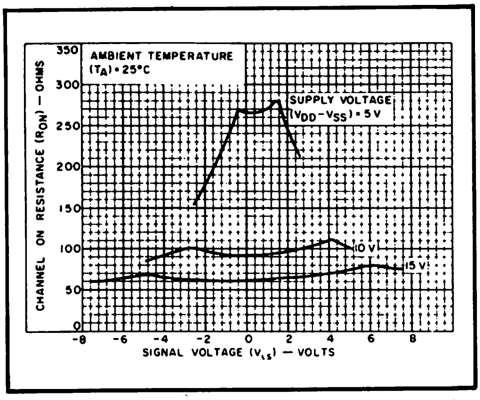
[3] Conditions for measuring V_{IH}:

V_{DD}	V_{OS}	V_{IS}	I_{OS} T_{LOW}	I_{OS} 25°C	I_{OS} T_{HIGH}	UNITS
5	5	4.6	– .25	– .20	– .14	
10	10	9.5	– .62	– .50	– .35	mA
15	15	13.5	– 1.8	– 1.50	– 1.10	

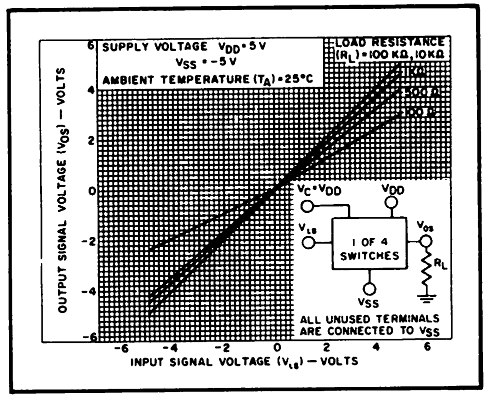
ELECTRICAL CHARACTERISTICS (Continued)

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

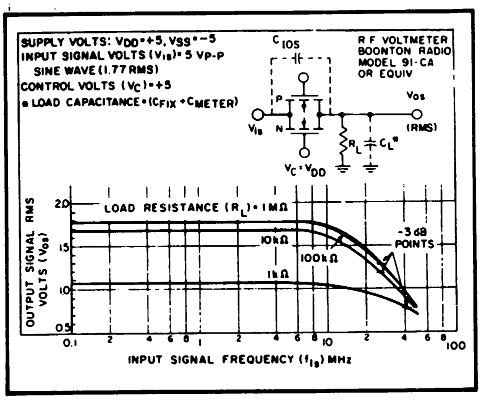
PARAMETER		CONDITIONS		V_{SS} (Vdc)	V_{DD} (Vdc)	Min.	Typ.	Max.	Units
SIGNAL INPUTS (V_{is}) AND OUTPUTS (V_{os})									
PROPAGATION DELAY TIME Signal Input to Signal Output	t_{PLH}, t_{PHL}	V_c=V_{DD} V_{is}=Square Wave R_L = 10kΩ		0 0 0	5 10 15	– – –	20 10 7.5	40 20 15	ns
BANDWIDTH (-3dB) (Sine Wave)	BW	V_c=V_{DD} V_{is}=5$V_{p\text{-}p}$ centered @ 0.0Vdc	R_L 1kΩ 10kΩ 100kΩ 1MΩ	-5	+5	– – – –	54 40 38 37	– – – –	MHz
INSERTION LOSS ($=20\log_{10}\frac{V_{os}}{V_{is}}$)		V_c=V_{DD} V_{is}=5$V_{p\text{-}p}$ centered @ 0.0Vdc	R_L 1kΩ 10kΩ 100kΩ 1MΩ	-5	+5	– – – –	2.3 0.2 0.1 0.05	– – – –	dB
SIGNAL DISTORTION (Sine Wave)		V_c=V_{DD} V_{is}=5$V_{p\text{-}p}$ centered @ 0.0Vdc f_{is}=1.0kHz R_L = 10kΩ		-5	+5	–	0.16	–	%
FEEDTHROUGH (-50dB)		V_c=V_{SS} V_{is}=5$V_{p\text{-}p}$ centered @0.0Vdc	R_L 1kΩ 10kΩ 100kΩ 1MΩ	-5	+5	– – – –	1250 140 18 2	– – – –	kHz
CROSSTALK (-50dB) Between two switches		V_c(A)=V_{DD} V_c(B)=V_{SS} V_{is}(A)=5$V_{p\text{-}p}$ centered @0.0Vdc R_L = 10kΩ		-5	+5	–	0.9	–	MHz
CAPACITANCE Input	C_{is}	V_C = V_{SS}		-5	+5	–	8	--	pF
Output	C_{os}					–	8	–	pF
Feedthrough	C_{ios}					–	0.5	–	pF
CONTROL INPUT (V_C)									
PROPAGATION DELAY TIME Turn on	t_{PC}	V_{SS}≤V_{is}≤V_{DD} R_L = 10kΩ		0 0 0	5 10 15	– – –	50 25 20	100 50 40	ns
MAXIMUM INPUT FREQUENCY	f_c	V_{SS}≤V_{is}≤V_{DD} R_L = 1.0kΩ		0 0 0	5 10 15	– – –	5 10 12	– – –	MHz
CROSSTALK (To signal port)		V_c=Square Wave R_L = 10kΩ R_{in} = 1.0kΩ		0 0 0	5 10 15	– – –	30 50 100	– – –	mV



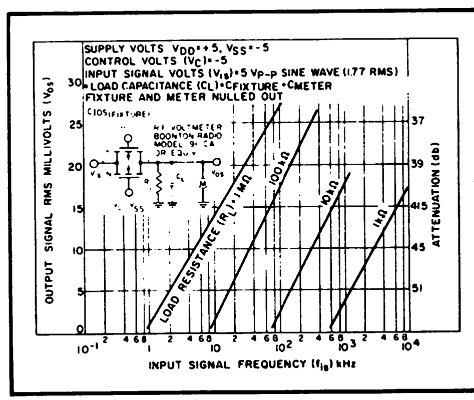
Typical channel ON resistance vs. signal voltage for three values of supply voltage (V_{DD}-V_{SS})



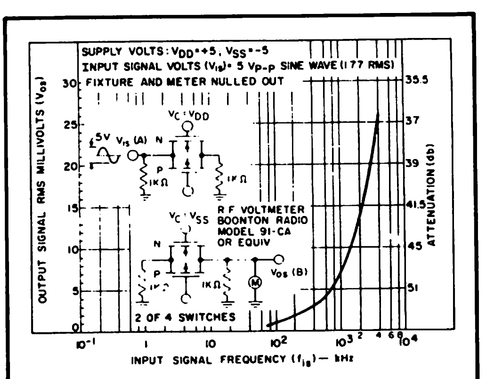
Typical ON characteristics for 1 of 4 channels.



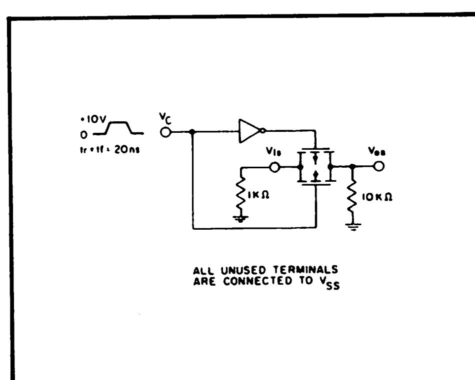
Typ. switch frequency response - switch "ON"



Typ. feedthru vs. freq. – switch "OFF"



Typ. crosstalk between switch circuits in the same package

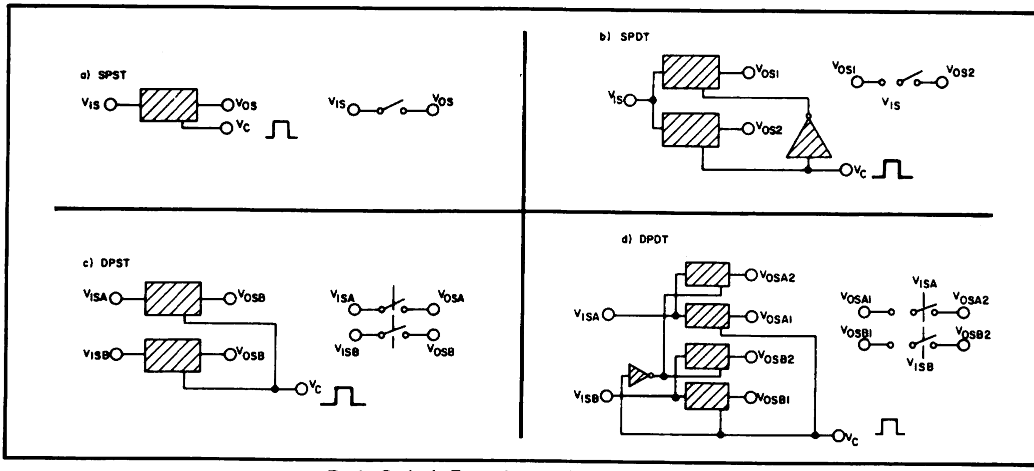


Test circuit, crosstalk-control input to signal output

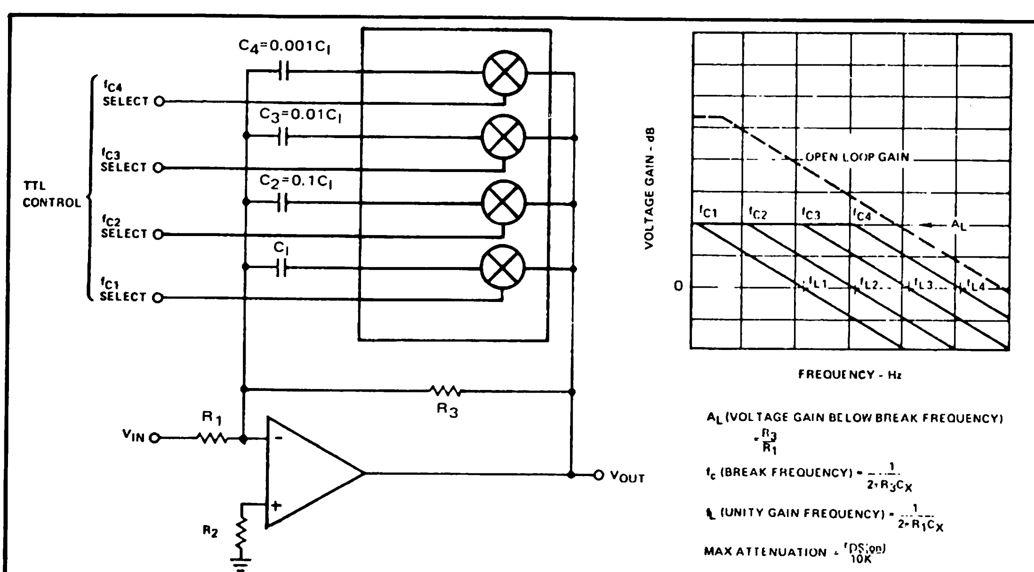
SPECIAL CONSIDERATIONS – 4066B

1. In applications where separate power sources are used to drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load of the 4 4066B bilateral switches). This provision avoids any permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from 4066B.
2. In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into terminals 1, 4, 8, or 11, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from R_{ON} values shown).
   No V_{DD} current will flow through R_L if the switch current flows into terminals 2, 3, 9, or 10. Failure to observe this condition may result in distortion of the signal.

APPLICATIONS INFORMATION



Basic Switch Functions using the 4066B



Active Low Pass Filter with Digitally Selected Break Frequency

SOLID STATE SCIENTIFIC

SCL4069UB

CMOS HEX INVERTER

FEATURES

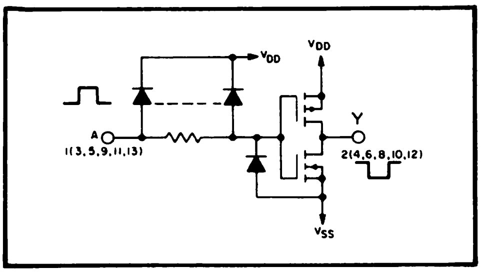
- Fully "B"-Series Compatible
- Diode Protection on all Inputs
- Pin Compatible with 74C04

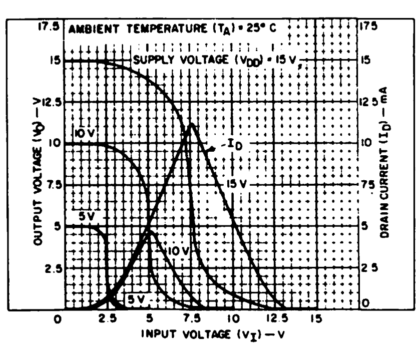
DESCRIPTION

The 4069UB consists of six CMOS inverter circuits. The device is intended for general-purpose inverter applications where the higher output drive and level-shifting feature of the 4009UB and 4049UB are not required.* The 4069UB is particularly useful for quasi-linear circuits such as oscillators (See Applications Information).

*For pin-to-pin compatibility with the 4009UB and 4049UB, the 4449UB is available.

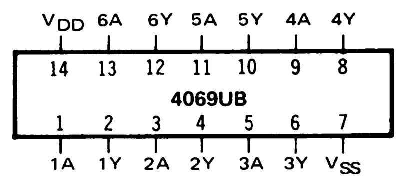
SCHEMATIC DIAGRAM
(one of six inverters)





Typical current and voltage transfer characteristics

CONNECTION DIAGRAM
(all packages)

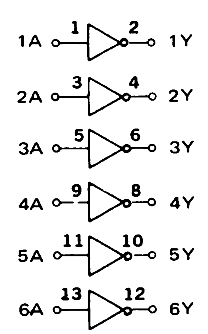


RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

LOGIC DIAGRAM



$V_{SS} = 7$
$V_{DD} = 14$

ELECTRICAL CHARACTERISTICS

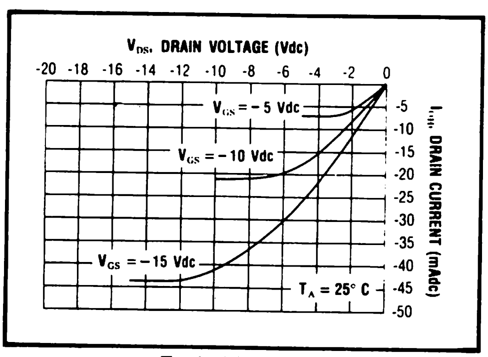
STATIC CHARACTERISTICS[1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[2] Min.	T_{LOW}[2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH}[2] Min.	T_{HIGH}[2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN}=V_{SS}$ or V_{DD}	–	0.05	–	0.0005	0.05	–	1.5	μAdc
		10	All valid input	–	0.10	–	0.001	0.10	–	3.0	
		15	combinations	–	0.20	–	0.002	0.20	–	6.0	

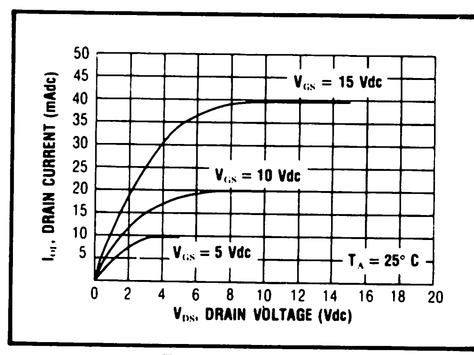
NOTES: 1 Remaining Static Characteristics are listed under "4000B Series Family Specifications".
2 T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}	5	–	50	100	ns
		10	–	25	50	
		15	–	20	40	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	75	150	ns
		10	–	35	70	
		15	–	30	60	

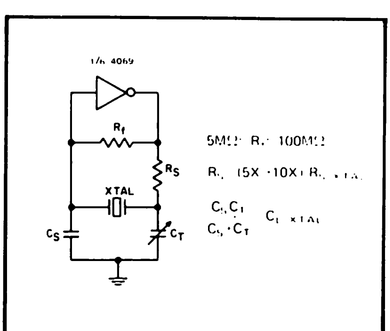


Typical P-Channel
Source Current Characteristics

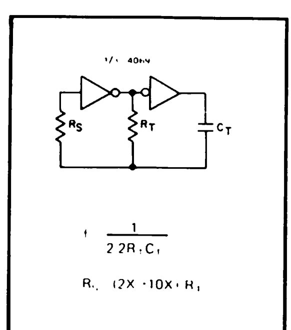


Typical N-Channel
Sink Current Characteristics

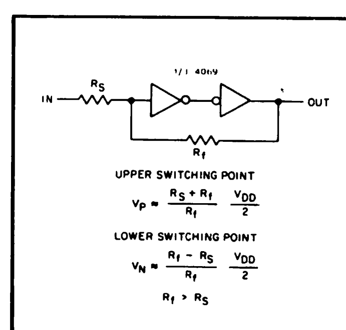
APPLICATIONS INFORMATION



Typical crystal oscillator circuit



Typical RC oscillator circuit



Input pluse shaping circuit (Schmitt Trigger)

CMOS QUAD EXCLUSIVE-OR GATE

FEATURES

- Buffered Outputs
- Diode Protection on all Inputs
- Fully "B"-Series Compatible
- Pin Compatible with 4030 types, MC14507, 74C86

DESCRIPTION

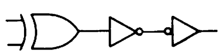
The 4070B contains four independent exclusive-OR gates integrated on a single monolithic silicon chip. Each exclusive-OR gate consists of five N-channel and five P-channel enhancement-mode transistors, plus output buffering devices.

TRUTH TABLE
(one of four gates)

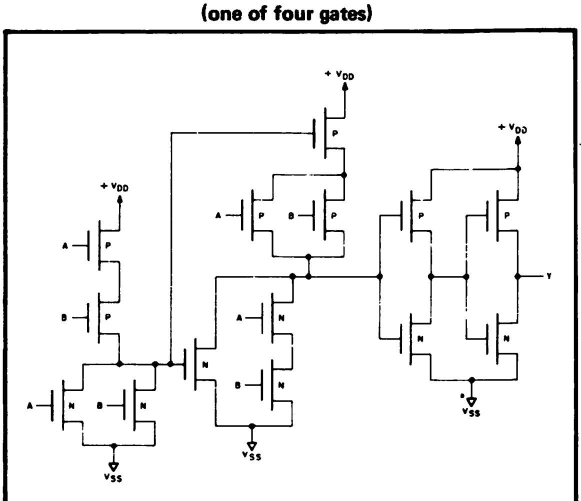
A	B	Y
0	0	0
1	0	1
0	1	1
1	1	0

Where 1 = High Level
0 = Low Level

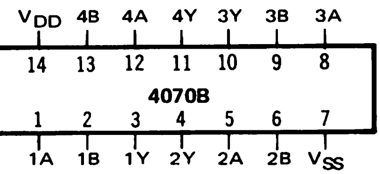
LOGIC DIAGRAM

4070B 

SCHEMATIC DIAGRAM
(one of four gates)



CONNECTION DIAGRAM
(all packages)



Add suffix for package:

C 14-pin Cerdip
D 14-pin Ceramic
E 14-pin Epoxy
F 14-pin Flat
H Chip

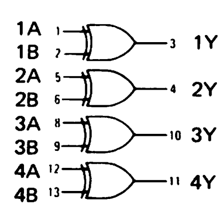
RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

Note: The 4070B is identical to the 4030B; the devices are fully interchangeable in all applications.

FUNCTION DIAGRAM



$Y = A \oplus B$

V_{DD} = Pin 14
V_{SS} = Pin 7

ELECTRICAL CHARACTERISTICS

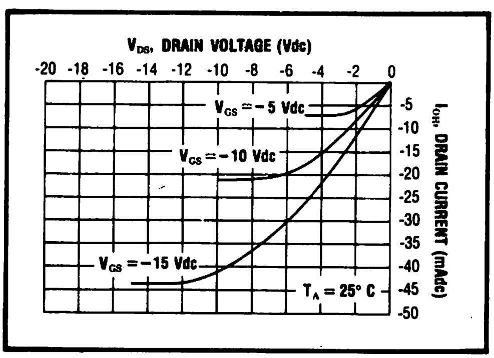
STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2]		+25°C			T_{HIGH} [2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5 10 15	$V_{IN}=V_{SS}$ or V_{DD} All valid input combinations	– – –	0.05 0.10 0.20	– – –	0.0005 0.001 0.002	0.05 0.10 0.20	– – –	1.5 3.0 6.0	μAdc

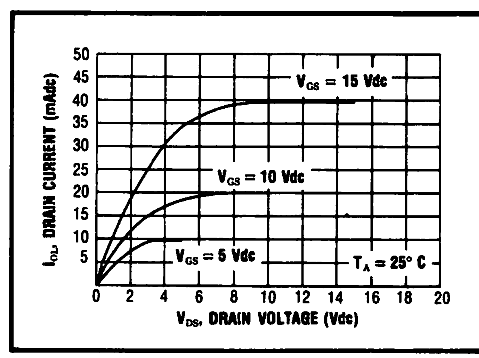
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}	5 10 15	– – –	140 65 50	280 130 100	ns
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5 10 15	– – –	100 50 40	200 100 80	ns



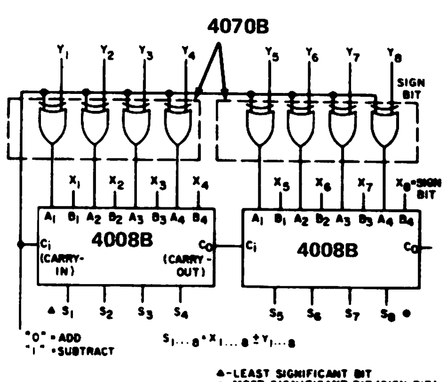
Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

APPLICATIONS INFORMATION

8-BIT TWO'S COMPLEMENT ADDER/SUBTRACTOR



X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1		X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	
0	0	0	0	0	0	0	0	= 0	1	1	1	1	1	1	1	1	= −1
0	0	0	0	0	0	0	1	= 1	1	1	1	1	1	1	1	0	= −2
0	0	0	0	0	0	1	0	= 2	1	1	1	1	1	1	0	1	= −3
0	0	0	0	0	0	1	1	= 3	1	1	1	1	1	1	0	0	= −4
.	.	.	.	.	.	.	.	.	1	1	1	1	1	0	1	1	= −6
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
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.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
0	1	1	1	1	1	1	0	= 126	1	0	0	0	0	0	0	1	= −127
0	1	1	1	1	1	1	1	= 127	1	0	0	0	0	0	0	0	= −128

Two's complement numbers and
their equivalent decimal values

SOLID STATE SCIENTIFIC

SCL4071B
SCL4072B
SCL4075B

CMOS OR GATES

4071B - Quad 2-Input OR
4072B - Dual 4-Input OR
4075B - Triple 3-Input OR

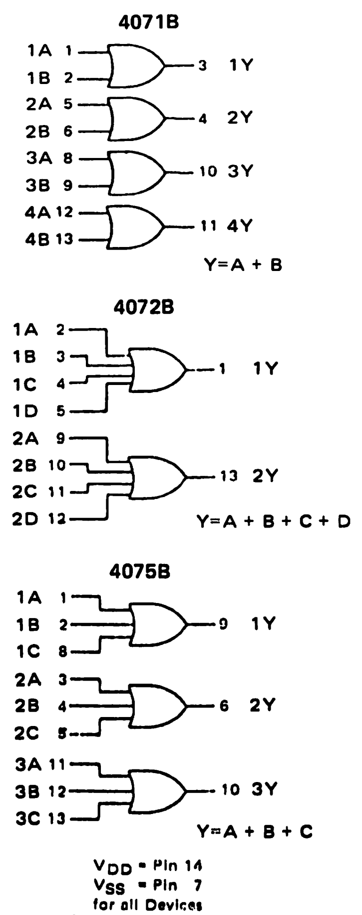
FEATURES

- ♦ Buffered Outputs
- ♦ Diode Protection on all Inputs
- ♦ Fully "B"-Series Compatible

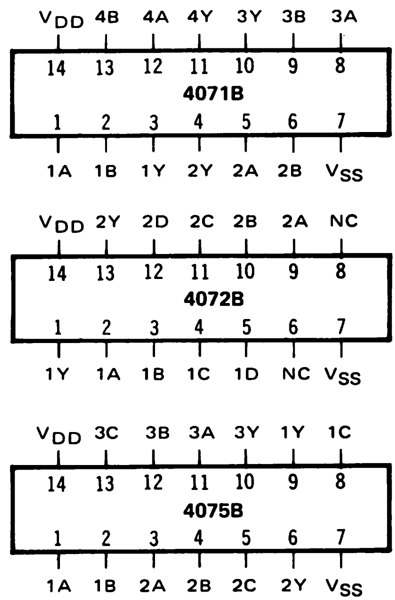
TRUTH TABLE

Inputs	Output
00 . . . 0	0
All other combinations	1

FUNCTION DIAGRAMS



CONNECTION DIAGRAMS
(all packages)



RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

ELECTRICAL CHARACTERISTICS

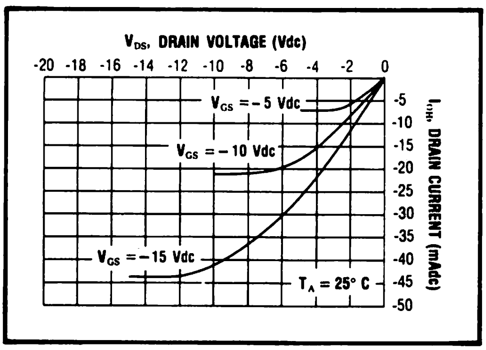
STATIC CHARACTERISTICS[1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[2]		+25°C			T_{HIGH}[2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN}=V_{SS}$ or V_{DD}	–	0.05	–	0.0005	0.05	–	1.5	μAdc
		10	All valid input	–	0.10	–	0.001	0.10	–	3.0	
		15	combinations	–	0.20	–	0.002	0.20	–	6.0	

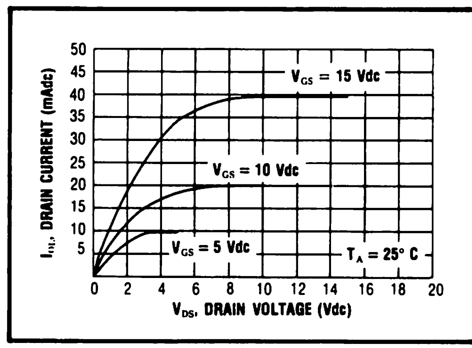
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	90	180	ns
		10	–	45	90	
		15	–	40	80	

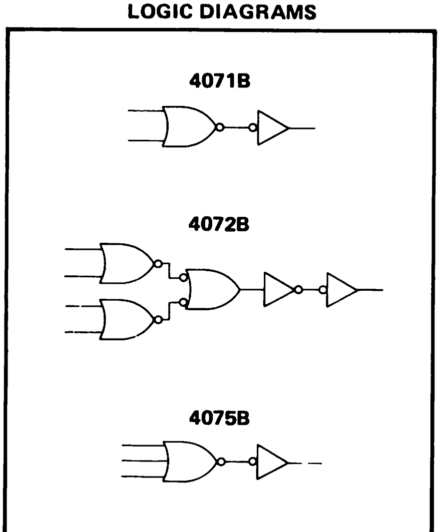


Typical P-Channel
Source Current Characteristics

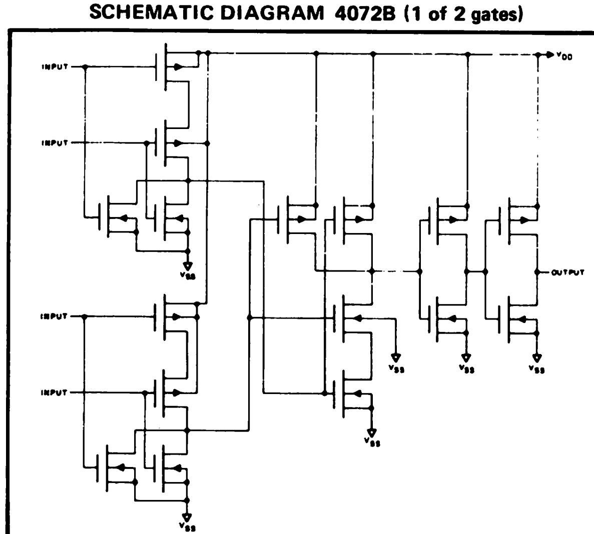


Typical N-Channel
Sink Current Characteristics

LOGIC DIAGRAMS



SCHEMATIC DIAGRAM 4072B (1 of 2 gates)



SOLID STATE SCIENTIFIC

SCL4076B

CMOS 4-BIT D-TYPE REGISTER

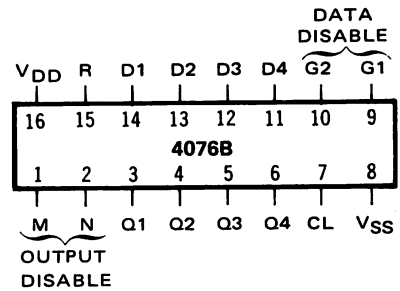
FEATURES

- 3-State Outputs with Gated Control Lines
- Fully Independent Clock
- Asynchronous Reset
- Fully Static Operation - DC to 12MHz @ 10Vdc

DESCRIPTION

The 4076B 4-bit Register consists of four D-Type flip-flops operating synchronously from a common Clock. OR-gated Output Disable inputs force the outputs into a high-impedance state for use in bus-organized systems. OR-gated Data Disable inputs cause the Q outputs to be fed back to the D inputs of the flip-flops. Thus, they are inhibited from changing state while the clocking process remains undisturbed. An asynchronous Master Reset is provided to clear all four flip-flops simultaneously independent of the Clock or Disable inputs.

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

C	16-pin Cerdip
D	16-pin Ceramic
E	16-pin Epoxy
F	16-pin Flat
H	Chip

TRUTH TABLE

Reset	Clock	Data Input Disable G1	Data Input Disable G2	Data D	Next State Output Q	
1	X	X	X	X	0	
0	0	X	X	X	Q	NC
0	↑	1	X	X	Q	NC
0	↑	X	1	X	Q	NC
0	↑	0	0	1	1	
0	↑	0	0	0	0	
0	1	X	X	X	Q	NC
0	↓	X	X	X	Q	NC

When either Output Disable M or N is high, the outputs are disabled (high impedance state); however sequential operation of the flip-flops is not affected.

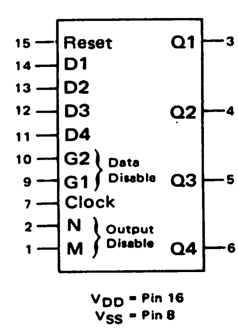
1 ≡ High Level X = Don't Care
0 ≡ Low Level NC = No Change

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS[1]

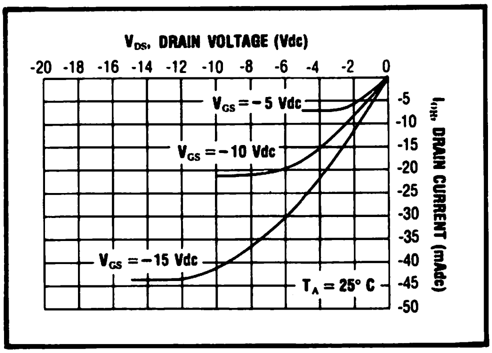
PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[2] Min.	T_{LOW}[2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH}[2] Min.	T_{HIGH}[2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN}=V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	μAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		15	combinations	–	20	–	0.2	20	–	600	
3-STATE OUTPUT LEAKAGE CURRENT	I_{ZL}	15		–	±0.1	–	$\pm10^{-4}$	±0.1	–	±1.0	μAdc

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

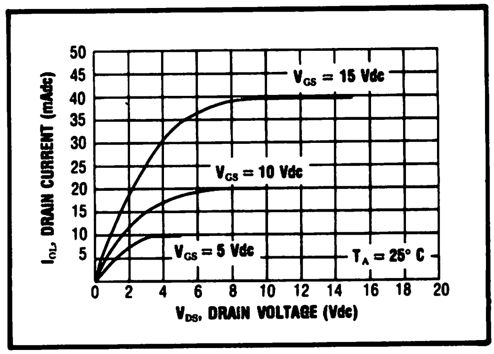
DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME Clock to Q	t_{PLH}, t_{PHL}	5	–	150	300	ns
		10	–	70	140	
		15	–	45	90	
Output Disable to Q	t_{PHZ}, t_{PLZ}	5	–	75	150	ns
		10	–	40	80	
		15	–	30	60	
	t_{PZH}, t_{PZL}	5	–	80	160	ns
		10	–	35	70	
		15	–	25	50	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
MINIMUM CLOCK PULSE WIDTH	PW_{CL}	5	–	80	160	ns
		10	–	40	80	
		15	–	30	60	
MAXIMUM CLOCK FREQUENCY	f_{CL}	5	3.0	6.0	–	MHz
		10	6.0	12	–	
		15	8.0	16	–	
MAXIMUM CLOCK RISE & FALL TIME[1]	t_{rCL}, t_{fCL}	5	15	–	–	μs
		10	15	–	–	
		15	15	–	–	
MINIMUM SETUP TIME Data Inputs	t_{setup}	5	–	75	150	ns
		10	–	40	80	
		15	–	30	60	
Data Disable Inputs	t_{setup}	5	–	100	200	ns
		10	–	60	120	
		15	–	45	90	
MINIMUM HOLD TIME All Inputs	t_{hold}	5	–	75	150	ns
		10	–	35	70	
		15	–	30	60	
RESET OPERATION						
PROPAGATION DELAY TIME	t_{PHL}	5	–	200	400	ns
		10	–	100	200	
		15	–	75	150	
MINIMUM RESET PULSE WIDTH	PW_R	5	–	75	150	ns
		10	–	40	80	
		15	–	30	60	
RESET REMOVAL TIME	t_{rem}	5	–	100	200	ns
		10	–	60	120	
		15	–	45	90	

[1] When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.

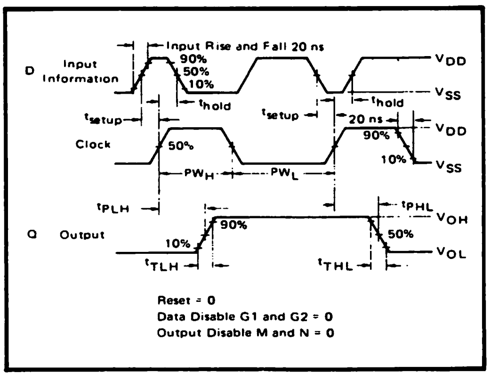


Typical P-Channel
Source Current Characteristics

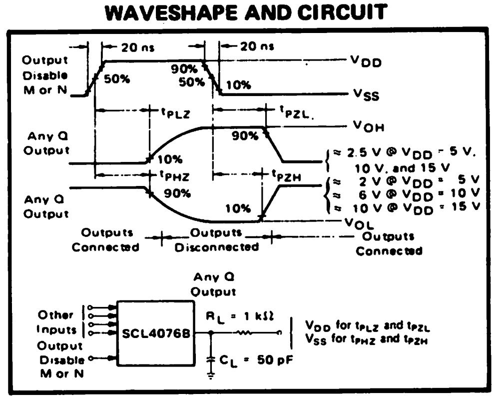


Typical N-Channel
Sink Current Characteristics

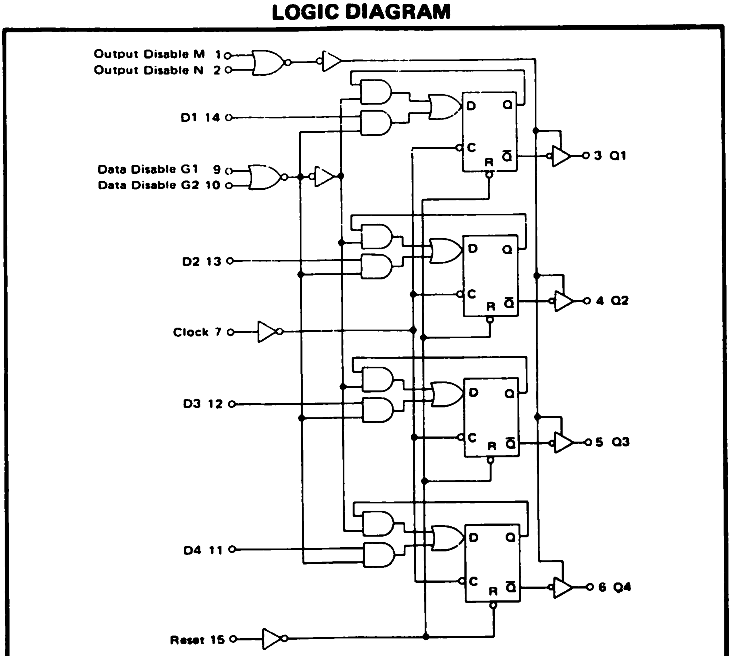
TIMING DIAGRAM



THREE-STATE PROPAGATION DELAY WAVESHAPE AND CIRCUIT



LOGIC DIAGRAM



CMOS QUAD EXCLUSIVE-NOR GATE

FEATURES

- Buffered Outputs
- Diode Protection on all Inputs
- Fully "B"-Series Compatible

DESCRIPTION

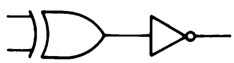
The 4077B contains four independent exclusive-NOR gates integrated on a single monolithic silicon chip. Each exclusive-NOR gate consists of five N-channel and five P-channel enhancement-mode transistors, plus output buffering devices.

TRUTH TABLE
(one of four gates)

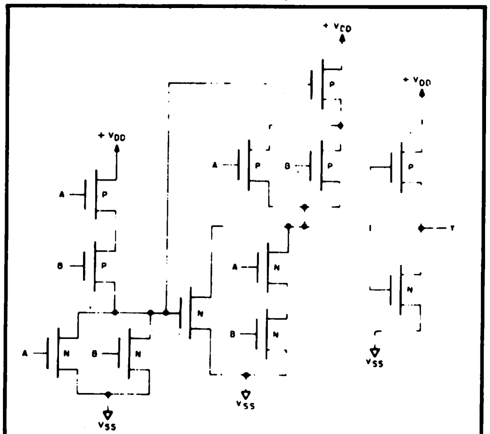
A	B	Y
0	0	1
1	0	0
0	1	0
1	1	1

Where 1 = High Level
0 = Low Level

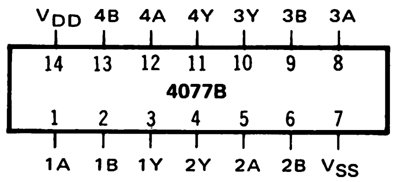
LOGIC DIAGRAM
(one of four gates)

4077B


SCHEMATIC DIAGRAM
(one of four gates)



CONNECTION DIAGRAM
(all packages)



Add suffix for package:

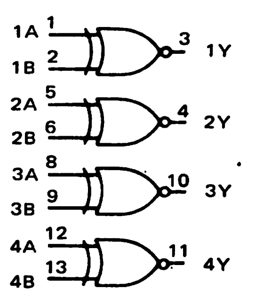
C	14-pin Cerdip
D	14-pin Ceramic
E	14-pin Epoxy
F	14-pin Flat
H	Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

FUNCTION DIAGRAM



$Y = \overline{A \oplus B}$

ELECTRICAL CHARACTERISTICS

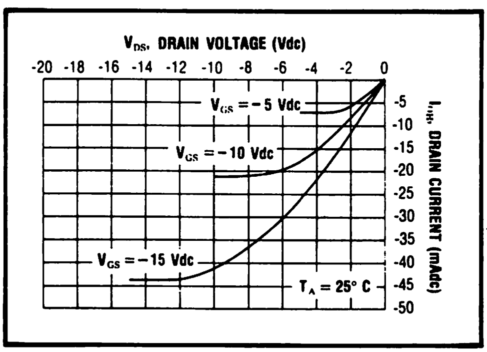
STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2]		+25°C			T_{HIGH} [2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN} = V_{SS}$ or V_{DD}	–	0.05	–	0.0005	0.05	–	1.5	μAdc
		10	All valid input	–	0.10	–	0.001	0.10	–	3.0	
		15	combinations	–	0.20	–	0.002	0.20	–	6.0	

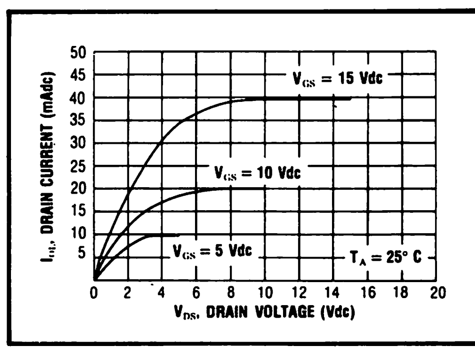
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}	5	–	150	300	ns
		10	–	65	130	
		15	–	50	100	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	



Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

CMOS AND GATES

4081B - Quad 2-Input AND
4082B - Dual 4-Input AND
4073B - Triple 3-Input AND

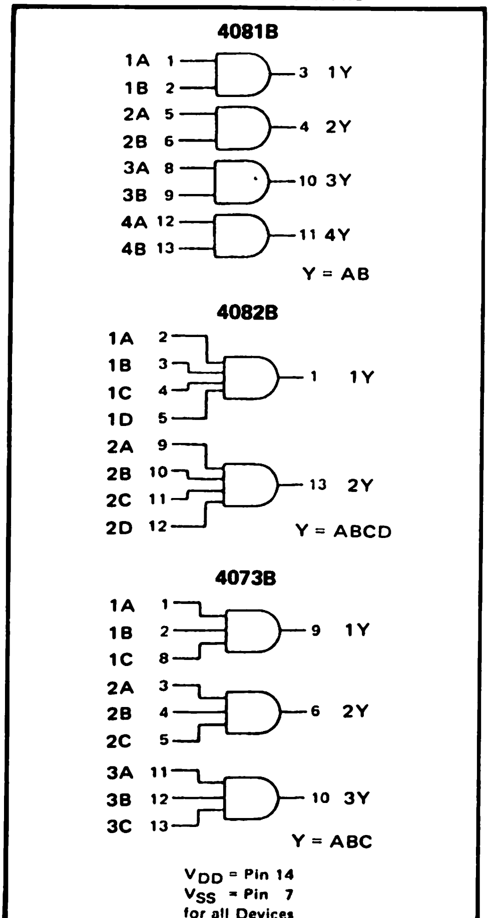
FEATURES

- **Buffered Outputs**
- **Diode Protection on all Inputs**
- **Fully "B"-Series Compatible**

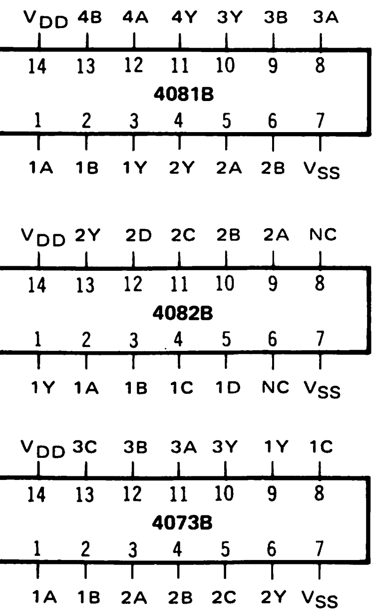
TRUTH TABLE

Inputs	Output
1 1 · · · 1	1
All other combinations	0

FUNCTION DIAGRAMS



CONNECTION DIAGRAMS
(all packages)



RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

ELECTRICAL CHARACTERISTICS

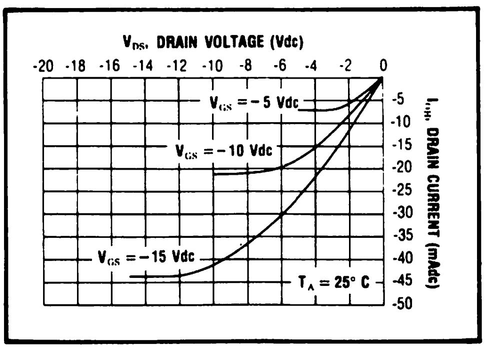
STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2]		+25°C			T_{HIGH} [2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN} = V_{SS}$ or V_{DD}	-	0.05	-	0.0005	0.05	-	1.5	μAdc
		10	All valid input	-	0.10	-	0.001	0.10	-	3.0	
		15	combinations	-	0.20	-	0.002	0.20	-	6.0	

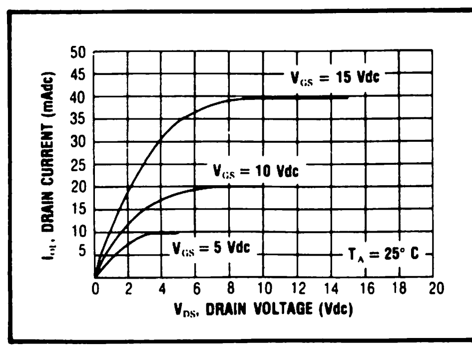
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}	5	-	120	240	ns
		10	-	60	120	
		15	-	45	90	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	-	100	200	ns
		10	-	50	100	
		15	-	40	80	

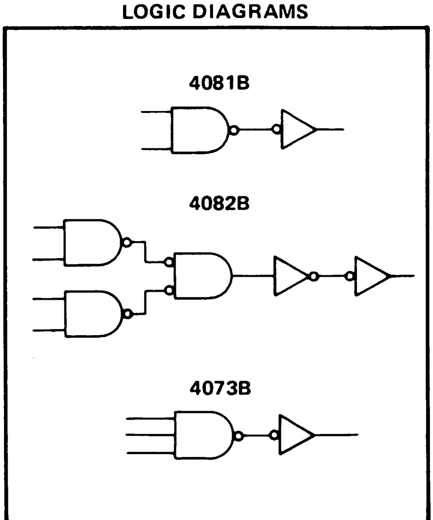


Typical P-Channel
Source Current Characteristics

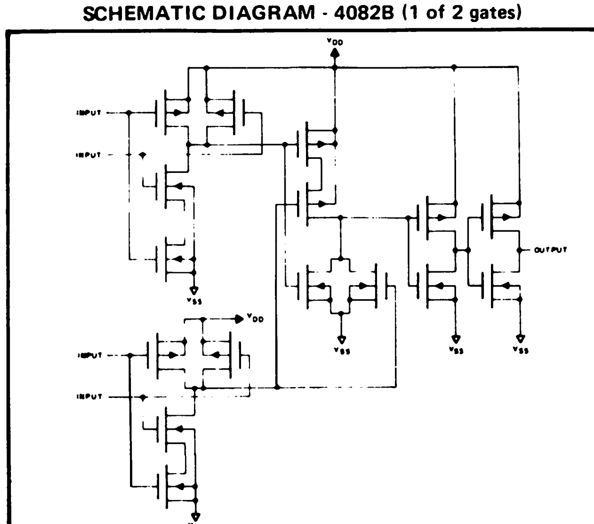


Typical N-Channel
Sink Current Characteristics

LOGIC DIAGRAMS



SCHEMATIC DIAGRAM - 4082B (1 of 2 gates)

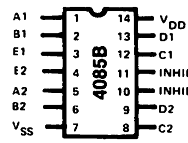


CMOS DUAL 2-WIDE, 2-INPUT AND-OR-INVERTER GATE

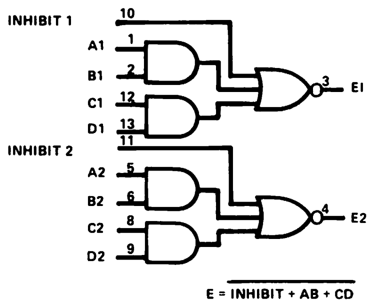
FEATURES

- Medium-speed operation $-t_{PHL}$ = 90 ns; t_{PLH} = 125 na (typ.) at 10 V
- Individual inhibit controls
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 18 V
- Maximum input current of 1 μA at 15 V over full temperature range; 100 nA at 15 V and 25° C
- Noise margin (over full package-temperature range):
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

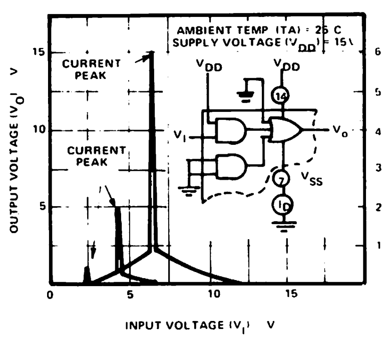
CONNECTION DIAGRAM



TOP VIEW



FUNCTIONAL DIAGRAM



DESCRIPTION

The 4085 contains a pair of AND-OR-INVERT gates, each consisting of two 2-input AND gates driving a 3-input NOR gate. Individual inhibit controls are provided for both A-O-I gates.

The 4085B types are supplied in 14-lead dual-in-line ceramic packages (D and C suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packs (F suffix), and in chip form (H suffix).

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS Min.	Max.	UNITS
Supply Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[2] Min.	T_{LOW}[2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH}[2] Min.	T_{HIGH}[2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN} = V_{SS}$ or V_{DD}	–	0.05	–	0.0005	0.05	–	1.5	μAdc
		10	All valid input	–	0.10	–	0.001	0.10	–	3.0	
		15	combinations	–	0.20	–	0.002	0.20	–	6.0	

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

ABSOLUTE MAXIMUM RATINGS

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to
V_{SS} Terminal) . . . . –0.5 to +20V

INPUT VOLTAGE RANGE,
ALL INPUTS . . . . –0.5 to V_{DD} +0.5V

DC INPUT CURRENT,
ANY ONE INPUT . . . . ±10 mA

POWER DISSIPATION PER PACKAGE (P_D):
For T_A = –40 to +60° C
(PACKAGE TYPE E) . . . . 500 mW
For T_A = +60 to +85e
For T_A = +60 to +85° C
(PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/° C to 200 mW
For T_A = –55 to +100° C
(PACKAGE TYPES D, F, C) . . . . . 500 mW
For T_A = +100 to +125° C
(PACKAGE TYPES D, F, C) . Derate Linearly at 12 mW/° C to 200 mW

DEVICE DISSIPATION
PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW

OPERATING TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, C, H . –55 to +125° C
PACKAGE TYPE E . . . . –40 to +85° C

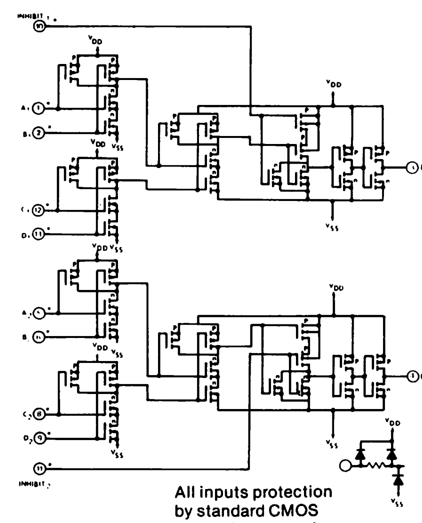
STORAGE TEMPERATURE
RANGE (T_{stg}) –65 to +150° C

LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ±1/32 inch (1.59 ±0.79mm)
from case for 10 s max. . . . . +265° C

DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50pF, R_L = 200 KΩ)

CHARACTERISTICS		CONDITIONS V_{DD} V	LIMITS Typ.	LIMITS Max.	UNITS
Propagation Delay Time (Data): High-to-Low Level	t_{PHL}	5	225	450	ns
		10	90	180	
		15	65	130	
Low-to-High Level	t_{PLH}	5	310	620	ns
		10	125	250	
		15	90	180	
Propagation Delay Time (Inhibit): High-to-Low Level	t_{PHL}	5	150	300	ns
		10	60	120	
		15	40	80	
Low-to-High Level	t_{PLH}	5	250	500	ns
		10	100	200	
		15	70	140	
Transition Time	t_{THL}, t_{TLH}	5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance	C_{IN}	Any Input	5	7.5	pF



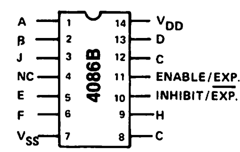
All inputs protection
by standard CMOS
protection network.

CMOS EXPANDABLE 4-WIDE, 2-INPUT AND-OR INVERT GATE

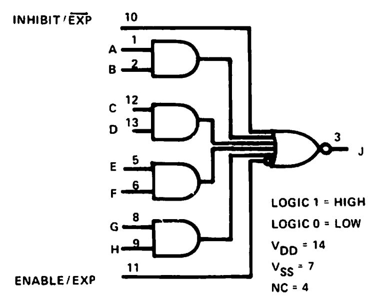
FEATURES

- Medium-speed operation — t_{PHL} = 90 ns; t_{PLH} = 140 ns (typ.) at 10 V
- INHIBIT and ENABLE inputs
- Buffered outputs
- 100% tested for quiescent current at 15 V
- Maximum input leakage current of 1μA over full package-temperature range; 100 nA at 15 V and 25° C
- Noise margin (over full package temperature range):
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

CONNECTION DIAGRAM



TOPVIEW



$J = \overline{INH + \overline{ENABLE} + AB + CD + EF + GH}$

FUNCTIONAL DIAGRAM

DESCRIPTION

The 4086B contains one 4-wide 2-input AND-OR-INVERT gate with an INHIBIT/$\overline{EXP}$ input and an ENABLE/EXP input. For a 4-wide A-O-I-function INHIBIT/EXP is tied to V_{SS} and ENABLE/EXP to V_{DD}. See Fig. 2 and its associated explanation for applications where a capability greater than 4-wide is required.

The 4086B is supplied in 14-lead dual-in-line ceramic packages (D and C suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packs (F suffix), and in chip form (H suffix).

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS Min.	LIMITS Max.	UNITS
Supply Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

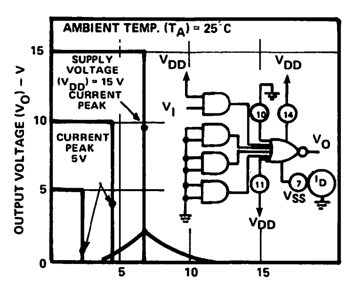


FIGURE I
TYPICAL VOLTAGE AND CURRENT TRANSFER CHARACTERISTICS

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2] Min.	T_{LOW} [2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH} [2] Min.	T_{HIGH} [2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN} = V_{SS}$ or V_{DD}	–	0.05	–	0.0005	0.05	–	1.5	μAdc
		10	All valid input	–	0.10	–	0.001	0.10	–	3.0	
		15	combinations	–	0.20	–	0.002	0.20	–	6.0	

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

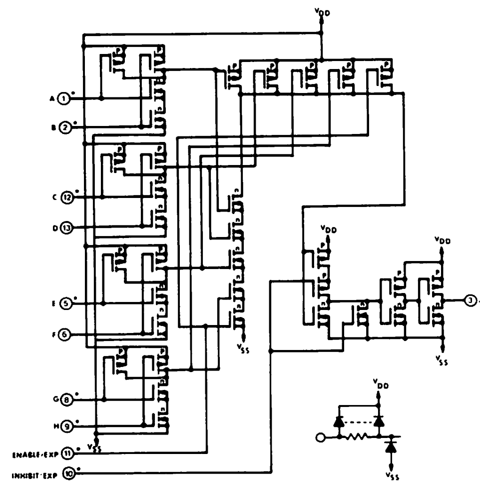
ABSOLUTE MAXIMUM RATINGS

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to
V_{SS} Terminal) . . . . −0.5 to + 18 V
INPUT VOLTAGE RANGE,
ALL INPUTS . . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT,
ANY ONE INPUT . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60° C
(PACKAGE TYPE E) . . . . 500 mW
For T_A = +60 to +85° C
(PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/° C to 200 mW
For T_A = −55 to +100° C
(PACKAGE TYPES D, C, F) . . . . 500 mW
For T_A = +100 to +125° C
(PACKAGE TYPES D, C, F) . . . . . Derate Linearly at 12 mW/° C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types). . . . 100 mW
OPERATING TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, C, H −55 to +125° C
PACKAGE TYPE E −40 to +85° C
STORAGE TEMPERATURE
RANGE (T_{stg}) . . . . −65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ±1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265° C

DYNAMIC ELECTRICAL CHARACTERISTICS

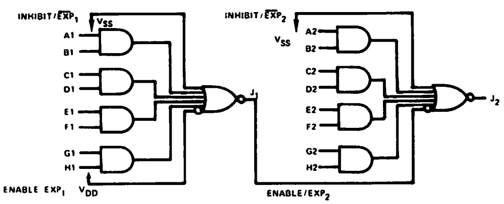
(T_A = 25°C; Input t_r, t_f = 20ns, C_L = 50pF, R_L = 200KΩ)

CHARACTERISTIC	CONDITIONS V_{DD} (V)	LIMITS TYP.	LIMITS MAX.	UNITS
Propagation Delay Time (Data) High to Low Level, t_{PHL}	5	225	450	ns
	10	90	180	
	15	60	120	
Low to High Level, t_{PLH}	5	350	700	ns
	10	140	280	
	15	100	200	
Propagation Delay Time (Inhibit) High to Low Level, $t_{PHL(INH)}$	5	150	300	ns
	10	60	120	
	15	40	80	
Low to High Level, $t_{PLH(INH)}$	5	250	500	ns
	10	100	200	
	15	70	140	
Transition Time, t_{THL}, t_{TLH}	5	100	200	ns
	10	50	100	
	15	40	80	
Input Capacitance C_{IN}	Any Input	5	7.5	pF



*ALL INPUTS PROTECTED BY STANDARD CMOS PROTECTION NETWORK

Fig. 3 shows two 4086's utilized to obtain an 8-wide 2-input A-O-I function. The output (J1) of one 4086 is fed directly to the ENABLE/EXP2 line of the second 4086. In a similar fashion, any NAND gate output can be fed directly into the ENABLE/EXP input to obtain a 5-wide A-O-I function. In addition, any AND gate output can be fed directly into the INHIBIT/$\overline{EXP}$ input with the same result.



$J2 = \overline{A1\,B1 + C1\,D1 + E1\,F1 + G1\,H1} \cdot \overline{A2\,B2 + C2\,D2 + E2\,F2 + F2\,H2}$

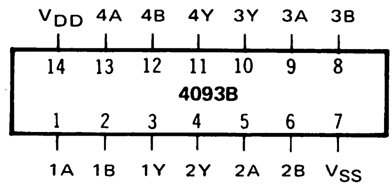
TWO 4086B'S CONNECTED
AS AN 8 WIDE 2 INPUT A-O-I GATE

CMOS QUAD SCHMITT TRIGGER

FEATURES

- Schmitt Trigger Action on each Input with no External Components
- Quad 2-Input NAND Configuration
- Noise Immunity Greater than 50%
- No Limit on Input Rise and Fall Times

CONNECTION DIAGRAM
(all packages)



DESCRIPTION

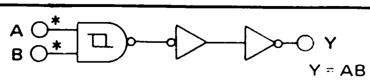
The 4093B consists of four Schmitt trigger circuits. Each circuit functions as a 2-input NAND gate with Schmitt trigger action on both inputs. The gate switches at different points for positive- and negative-going signals. The difference between the positive voltage (V_P) and the negative voltage (V_N) is defined as the hysteresis voltage (V_H). This device is useful in high-noise environments and in wave and pulse shapers and multivibrators.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

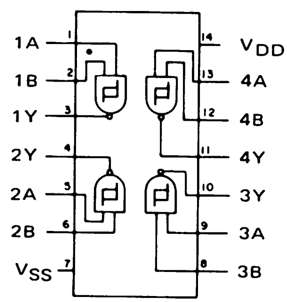
DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

LOGIC DIAGRAM



* All inputs protected by Standard Protection Network

BLOCK DIAGRAM



Y = AB

ELECTRICAL CHARACTERISTICS

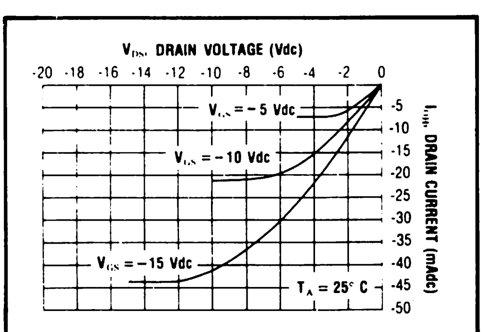
STATIC CHARACTERISTICS[1]

PARAMETER		VDD (Vdc)	CONDITIONS	T_{LOW}[2] Min.	T_{LOW}[2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH}[2] Min.	T_{HIGH}[2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN} = V_{SS}$ or V_{DD}	–	1.0	–	0.0005	1.0	–	30	μAdc
		10	All valid input	–	2.0	–	0.001	2.0	–	60	
		15	combinations	–	4.0	–	0.002	4.0	–	120	
POSITIVE TRIGGER THRESHOLD VOLTAGE	V_P (V_{IL})	5		3 typ		2.3	2.9	3.5	2.9 typ		Vdc
		10		5.9 typ		4.5	5.9	7.0	5.9 typ		
		15		8.9 typ		6.8	8.9	11	8.9 typ		
NEGATIVE TRIGGER THRESHOLD VOLTAGE	V_N (V_{IH})	5		2.6 typ		1.5	2.3	2.7	2.1 typ		Vdc
		10		4 typ		3.0	3.9	5.5	3.8 typ		
		15		5.5 typ		4.0	5.4	8.2	5.3 typ		
HYSTERESIS VOLTAGE	V_H	5		.4	2.0	.4	.75	2.0	.4	2.0	V_{dc}
		10		.7	3.0	.7	.95	3.0	.7	3.0	
		15		.85	4.0	.85	1.20	4.0	.85	4.0	

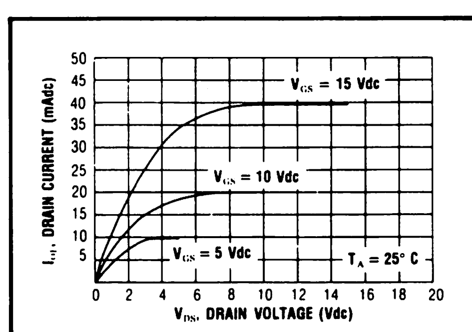
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25 C)

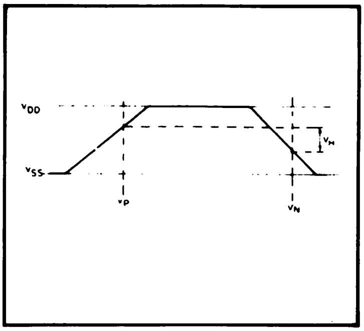
PARAMETER		VDD (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}	5	–	190	380	ns
		10	–	90	180	
		15	–	65	130	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	



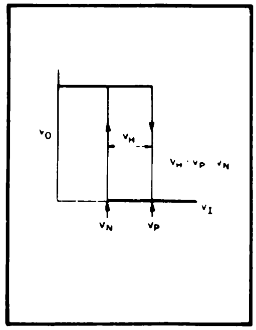
Typical P-Channel
Source Current Characteristics



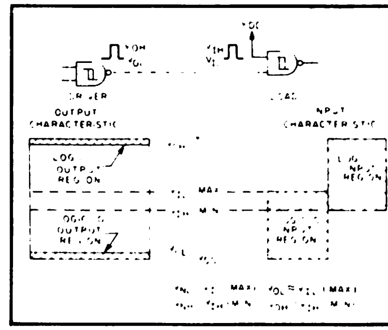
Typical N-Channel
Sink Current Characteristics



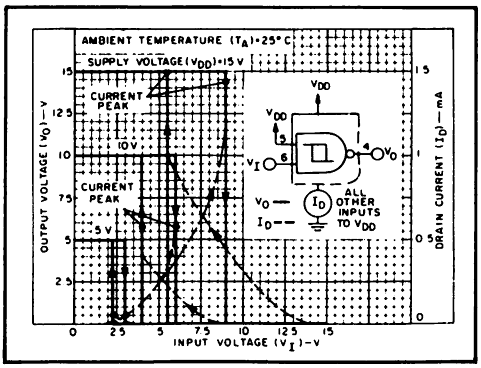
Definition of V_P, V_N and V_H.



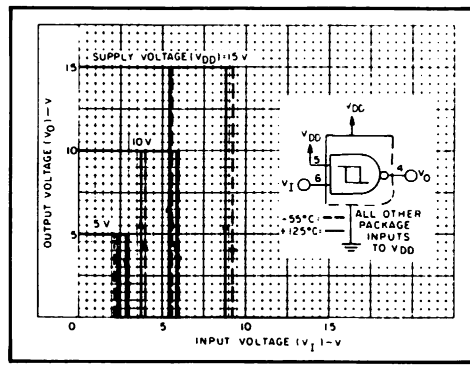
Transfer characteristic of 1 of 4 gates.



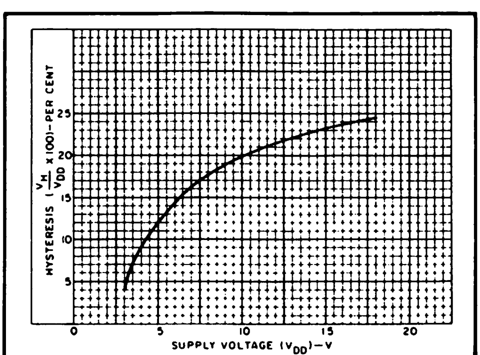
Input and output characteristics.

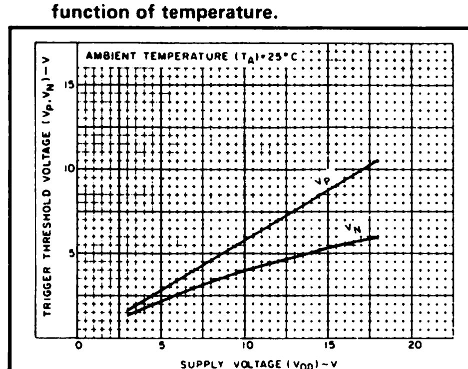


Typical current and voltage transfer characteristics.



Typical voltage transfer characteristics as a function of temperature.

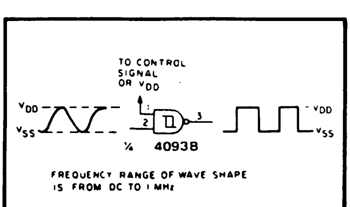




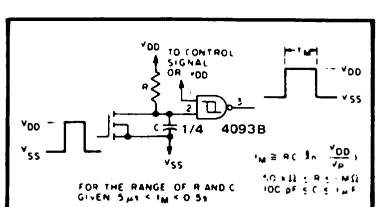
Typical trigger threshold voltage vs. V_{DD}.

Typical per cent hysteresis vs. supply voltage.

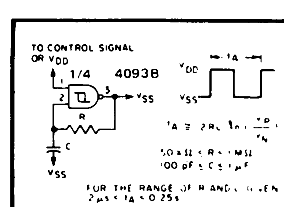
APPLICATIONS INFORMATION



Wave shaper.



Monostable multivibrator.



Astable multivibrator.

CMOS 8-STAGE SHIFT-AND-STORE BUS REGISTER

FEATURES:

- **3-state parallel outputs for connection to common bus**
- **Separate serial outputs synchronous to both positive and negative clock edges for cascading**
- **Medium speed operation—5 MHz at 10 V**
- **Quiescent current specified to 15 V**
- **Maximum input leakage of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**
- **5-V, 10-V, and 15-V parametric ratings**

DESCRIPTION:

The 4094B is an 8-stage serial shift register having a storage latch associated with each stage for strobing data from the serial input to parallel buffered 3-state outputs. The parallel outputs may be connected directly to common bus lines. Data is shifted on positive clock transitions. The data in each shift register stage is transferred to the storage register when the STROBE input is high. Data in the storage register appears at the outputs whenever the OUTPUT-ENABLE signal is high.

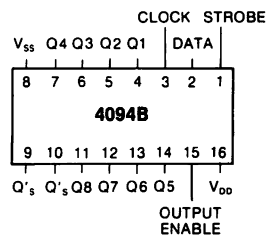
Two serial outputs are available for cascading a number of 4094B devices.

Data is available at the Q_S serial output terminal on positive clock edges to allow for high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information, available at the Q'_S terminal on the next negative clock edge, provides a means for cascading 4094B devices when the clock rise time is slow.

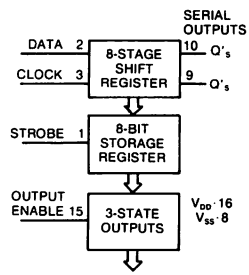
APPLICATIONS

- **Serial-to-parallel data conversion**
- **Remote control holding register**
- **Dual-rank shift, hold, and bus applications**

CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM



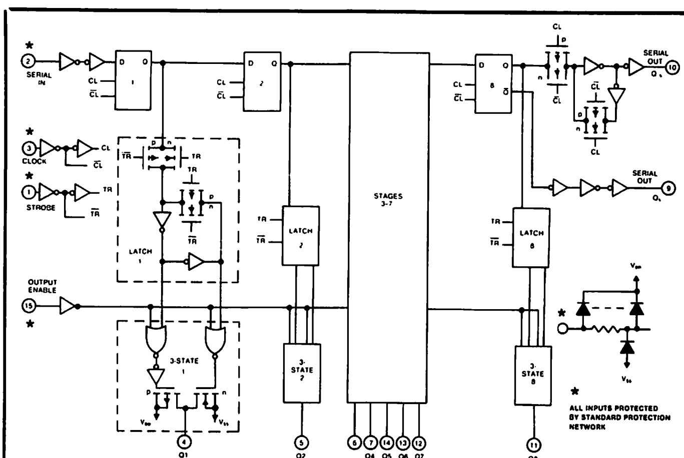
PARALLEL OUTPUTS Q1 - Q8

(TERMINALS 4, 5, 6, 7, 14, 13, 12, 11, RESPECTIVELY)

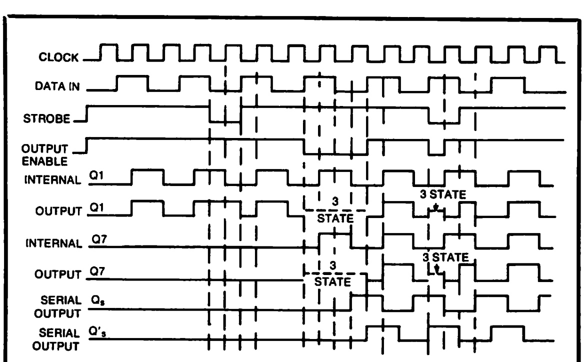
RECOMMENDED OPERATING CONDITIONS *at T_A = 25°C, Except as Noted.*
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	18	V
Data Setup Time, t_S	5 10 15	125 55 35	— — —	ns
Clock Pulse Width, t_W	5 10 15	200 100 83	— — —	ns
Clock Input Frequency, f_{CL}	5 10 15	dc	1.25 2.5 3	MH$_z$
Clock Rise & Fall Time, t_rCL, t_fCL*	5, 10, 15	—	15	μs
Strobe Pulse Width, t_W	5 10 15	200 80 70	— — —	ns

*If more than one unit is cascaded t_fCL (for Q_S only) should be made less than or equal to the sum of the fixed propagation delay at 50 pF and the transition time of the output driving stage for the estimated capacitive load.



Logic Diagram



TRUTH TABLE

CL▲	Output Enable	Strobe	Data	Parallel Outputs		Serial Outputs	
				Q1	QN	QS*	Q'S
	0	X	X	OC	OC	Q7	NC
	0	X	X	OC	OC	NC	Q7
	1	0	X	NC	NC	Q7	NC
	1	1	0	0	Q_{N-1}	Q7	NC
	1	1	1	1	Q_{N-1}	Q7	NC
	1	1	1	NC	NC	NC	Q7

▲ = Level Change   Logic 1 ≡ High   NC = No Change
X = Don't Care   Logic 0 ≡ Low   OC = Open Circuit

*At the positive clock edge information in the 7th shift register stage is transferred to the 8th register stage and the Q_s output.

STATIC ELECTRICAL CHARACTERISTICS [1]

PARAMETER	V_{DD}	T_{LOW}[2] Min.	T_{LOW}[2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH}[2] Min.	T_{HIGH}[2] Max.	Units
QUIESCENT DEVICE CURRENT (I_{DD})	5	—	5	—	0.02	5	—	150	μA
	10	—	10	—	0.02	10	—	300	
	15	—	20	—	0.02	20	—	600	
3-STATE OUTPUT LEAKAGE CURRENT (I_{ZL})	15	—	±0.1	—	$\pm 10^{-4}$	±0.1	—	±1	μA

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications"
[2] T_{LOW} = −55°C for C, D, F, H devices.
= −40°C for E Devices.
T_{HIGH} = +125°C for E, D, F, H devices.
= +85°C for E devices.

DYNAMIC ELECTRICAL CHARACTERISTICS
At $T_A = 25°C$; Input t_r, t_f = 20 ns, C_L = 50 pF

CHARACTERISTIC	V_{DD} (V)	LIMITS ALL PACKAGES MIN.	TYP.	MAX.	UNITS
Propagation Delay Time. t_{PHL}, t_{PLH} Clock to Serial Output (Q's)	5	—	300	600	ns
	10	—	125	250	
	15	—	95	190	
Clock to Serial Output (Q's)	5	—	230	460	ns
	10	—	110	220	
	15	—	75	150	
Clock to Parallel Output	5	—	420	840	ns
	10	—	195	390	
	15	—	135	270	
Strobe to Parallel Output	5	—	290	580	ns
	10	—	145	290	
	15	—	100	200	
Output Enable to Parallel Output: t_{PHL}	5	—	140	280	ns
	10	—	75	150	
	15	—	55	110	
t_{PLH}	5	—	225	450	ns
	10	—	95	190	
	15	—	70	140	
Minimum Strobe Pulse Width, t_W	5	—	100	200	ns
	10	—	40	80	
	15	—	35	70	
Minimum Clock Pulse Width, t_W	5	—	100	200	ns
	10	—	50	100	
	15	—	40	83	
Minimum Data Setup Time, t_S	5	—	60	125	ns
	10	—	30	55	
	15	—	20	35	
Transition Time; t_{THL}, t_{TLH}	5	—	100	200	ns
	10	—	50	100	
	15	—	40	80	
Clock Rise and Fall Time; t_r, t_f	5, 10, 15	—	—	15	μs
Max. Clock Input Frequency, f_{CL}	5	1.25	2.5	—	MHz
	10	2.5	5	—	
	15	3	6	—	
Average Input Capacitance, C_I (Any Input)	—	—	5	—	pF

8-BIT ADDRESSABLE LATCH

FEATURES
- Serial data input
- Active parallel output
- Storage register capability
- Master clear
- Can function as demultiplexer

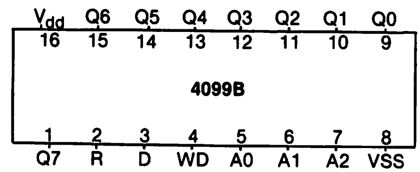
APPLICATIONS
- Multi-line decoders
- A/D converters

DESCRIPTION
The 4099B 8-bit addressable latch is a serial-input, parallel-output storage register that can perform a variety of functions.

Data are inputted to a particular bit in the latch when that bit is addressed (by means of inputs A0, A1, A2) and when WRITE DISABLE is at a low level. When WRITE DISABLE is high, data entry is inhibited; however, all 8 outputs can be continuously read independent of WRITE DISABLE and address inputs.

A master RESET input is available, which resets all bits to a logic "0" level when RESET and WRITE DISABLE are at a high level. When RESET is at a high level, and WRITE DISABLE is at a low level, the latch acts as a 1-of-8 demultiplexer; the bit that is addressed has an active output which follows the data input, while all unaddressed bits are held to a logic "0" level.

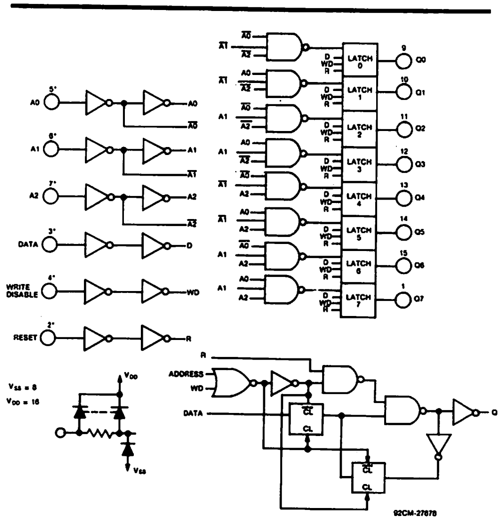
CONNECTION DIAGRAM



TRUTH TABLE

WD	R	Addressed Latch	Unaddressed Latch
0	0	D	Holds previous data
0	1	D	0
1	0	Holds previous data	
1	1	0	0

LOGIC DIAGRAM



*ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

TIMING DIAGRAMS

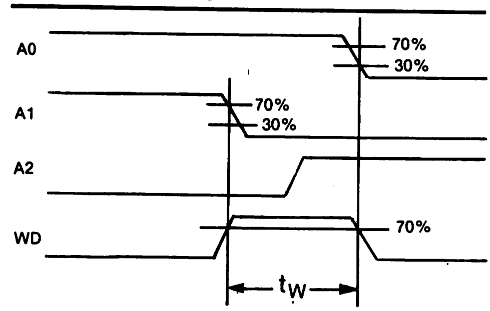


Fig.1 — Definition of WRITE DISABLE ON time.

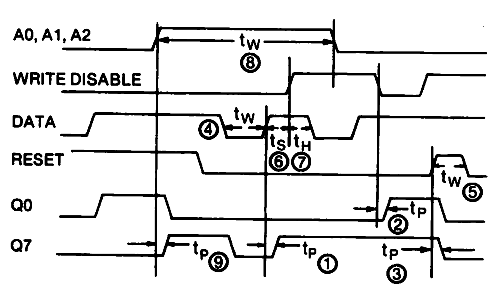


Fig. 2 — Master timing diagram.

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS[1, 2]

PARAMETER	V_{DD}	I_{LOW}[2] Min.	I_{LOW}[2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH} Min.	T_{HIGH} Max.	Units
QUIESCENT DEVICE CURRENT I_{DD}	5	—	5	—	0.02	5	—	150	μA
	10	—	10	—	0.02	10	—	300	
	15	—	20	—	0.02	20	—	600	

DYNAMIC CHARACTERISTICS

T_A = 25° C, C_L = 50 pF, Input t_r, t_f = 20 ns, R_L = 200 K

CHARACTERISTIC	SEE FIG 2*	V_{DD} (V)	LIMITS ALL PACKAGE TYPES TYP.	LIMITS ALL PACKAGE TYPES MAX.	UNITS
Propagation Delay: t_{PLH}, t_{PHL} Data to Output	1	5	200	400	
		10	75	150	
		15	50	100	
WRITE DISABLE to Output. t_{PLH}, t_{PHL}	2	5	200	400	
		10	80	160	ns
		15	60	120	
Reset to Output, t_{PHL}	3	5	175	350	
		10	80	160	
		15	65	130	
Address to Output, t_{PLH}, t_{PHL}	9	5	225	450	
		10	100	200	
		15	75	150	
Transition Time, T_{THL}, (Any Output) t_{TLH}		5	100	200	
		10	50	100	ns
		15	40	80	
Minimum Pulse Width, t_W Data	4	5	100	200	
		10	50	100	ns
		15	40	80	
Address	8	5	200	400	
		10	100	200	ns
		15	65	125	
Reset	5	5	75	150	
		10	40	75	ns
		15	25	50	
Minimum Setup Time, t_S Data to WRITE DISABLE	6	5	50	100	
		10	25	50	ns
		15	20	35	
Minimum Hold Time, t_H Data to WRITE DISABLE	7	5	75	150	
		10	40	75	ns
		15	25	50	
Average Input Capacitance C_1	Any Input		5	—	pF

*Circled numbers refer to times indicated on master timing diagram.

Note: In addition to the above characteristics, a WRITE DISABLE ON time (the time that WRITE DISABLE is at a high level) must be observed during an address change for the total time that the external address lines A0, A1, and A2 are settling to a stable level, to prevent a wrong cell from being addressed (see Fig. 1).

SOLID STATE SCIENTIFIC

SCL4160B
SCL4161B
SCL4162B
SCL4163B

CMOS SYNCHRONOUS 4-BIT COUNTERS

FEATURES

- BCD Decade (4160B, 4162B) or 4-Bit Binary (4161B, 4163B) Counting
- Internal Look-Ahead for Fast Counting
- Carry Output for Cascading
- Synchronously Programmable
- Sychronous Counting
- Load Control Input
- Clear Input - Asynchronous (4160B, 4161B) or Synchronous (4162B, 4163B)
- Static Operation - DC to 5MHz @ 10Vdc

DESCRIPTION

The 4160B - 4163B are Synchronous Programmable Counters constructed with complementary MOS P-Channel and N-Channel enhancement-mode devices in a single monolithic structure. These counters are functionally equivalent to the 74160 - 74163 TTL counters.

Two are synchronous programmable decade counters with asynchronous and synchronous Clear inputs respectively (4160, 4162). The other two are 4-bit binary counters with asynchronous and synchronous Clear respectively (4161, 4163).

SYNCHRONOUS MODE SELECTION 4160B/4161B

L	PE	TE	Mode
L	X	X	Preset
H	L	X	No Change
H	X	L	No Change
H	H	H	Count

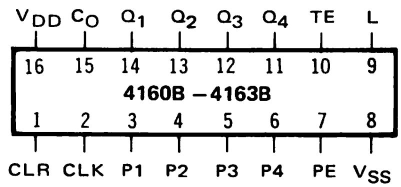
H = High level L = Low level X = Don't care

SYNCHRONOUS MODE SELECTION 4162B/4163B

CLR	L	PE	TE	Mode
H	L	X	X	Preset
H	H	L	X	No Change
H	H	X	L	No Change
H	H	H	H	Count
L	X	X	X	Reset

H = High level L = Low level X = Don't care

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

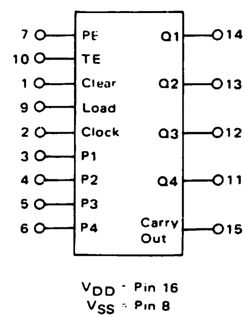
C	16-pin Cerdip
D	16-pin Ceramic
E	16-pin Epoxy
F	16-pin Flat
H	Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

BLOCK DIAGRAM



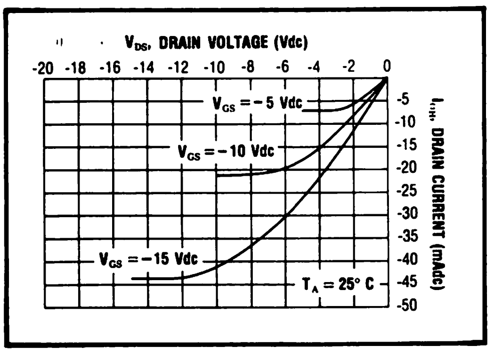
SELECTOR GUIDE

CLEAR	MODULUS	
	DECADE	BINARY
Asynchronous	4160B	4161B
Synchronous	4162B	4163B

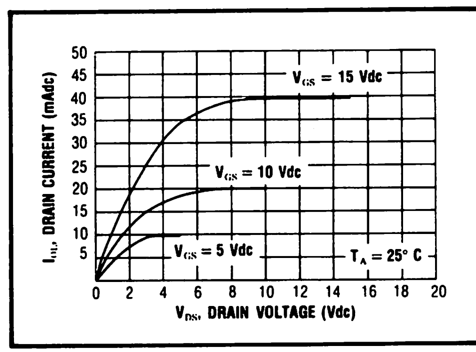
FUNCTIONAL DESCRIPTION

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the Load input disables the counter and causes the outputs to agree with the setup data after the next Clock pulse regardless of the levels of the Enable inputs. Low-to-high transitions at the Load input should be avoided when the Clock is low if the Enable inputs are high at or before the transition. The Clear function for the 4160, 4161 is asynchronous and a low level at the Clear input sets all four of the flip-flop outputs low regardless of the levels of the Clock, Load or Enable inputs. The Clear function for the 4162 and 4163 is synchronous and a low level at the Clear inputs sets all four of the flip-flop outputs low after the next Clock pulse regardless of the levels of the Enable inputs. This synchronous Clear allows the count length to be modified easily; decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the Clear input to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two Count Enable inputs and a Carry output. Both Count Enable inputs (PE, TE) must be high to count, and Enable input TE is fed forward to enable the carry output. The Carry output thus enabled will produce a positive output pulse with a duration approximately equal to the positive portion of the Q1 output. This positive overflow Carry pulse can be used to enable successive cascaded stages. High-to-low-level transitions at the Enable PE or TE inputs should occur only when the Clock input is high.

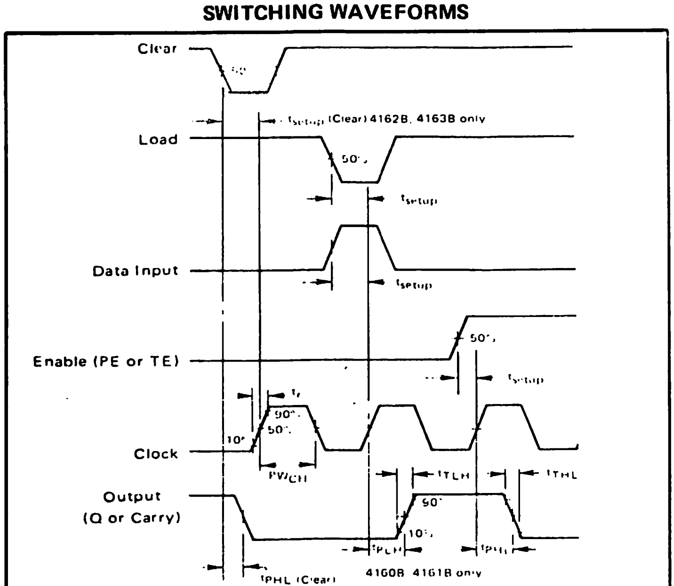


Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

SWITCHING WAVEFORMS



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2] Min.	T_{LOW} [2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH} [2] Min.	T_{HIGH} [2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN} = V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	μAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		15	combinations	–	20	–	0.2	20	–	600	

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

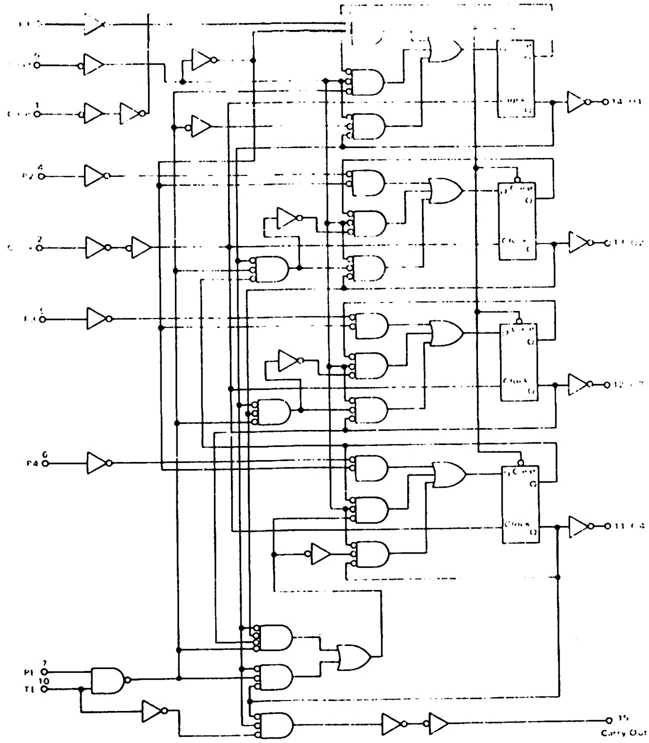
PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}					
Clock to Q		5	–	200	400	ns
		10	–	80	160	
		15	–	60	120	
Clock to Carry Out		5	–	240	480	ns
		10	–	95	190	
		15	–	75	150	
TE to Carry Out		5	–	180	360	ns
		10	–	70	140	
		15	–	50	100	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
MINIMUM CLOCK PULSE WIDTH	PW_{CL}	5	–	85	170	ns
		10	–	35	70	
		15	–	25	50	
MAXIMUM CLOCK FREQUENCY	f_{CL}	5	2.0	3.0	–	MHz
		10	5.5	8.5	–	
		15	8.0	12.0	–	
MAXIMUM CLOCK RISE AND FALL TIME [1]	t_{rCL}, t_{fCL}	5	50	∞	–	ms
		10	50	∞	–	
		15	50	∞	–	
MINIMUM SETUP TIME	t_{setup}					
Data to Clock		5	–	120	240	ns
		10	–	45	90	
		15	–	30	65	
Load to Clock		5	–	120	240	ns
		10	–	45	90	
		15	–	30	65	
PE or TE to Clock		5	–	170	340	ns
		10	–	70	140	
		15	–	50	100	
CLEAR OPERATION						
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}					
Clear to Q (4160, 4161 only)		5	–	150	300	ns
		10	–	50	100	
		15	–	30	60	
MINIMUM SETUP TIME	t_{setup}					
Clear to Clock (4162, 4163 only)		5	–	120	240	ns
		10	–	50	100	
		15	–	30	60	

[1] When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.

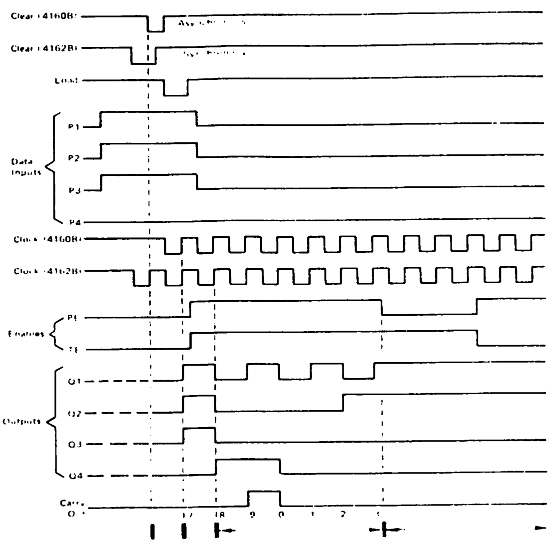
4160B, 4162B LOGIC DIAGRAM
(Clear is synchronous for 4162B)

Sequence illustrated in waveforms:

1. Clear outputs to zero.
2. Preset to BCD seven.
3. Count to eight, nine, zero, one, two and three.
4. Inhibit



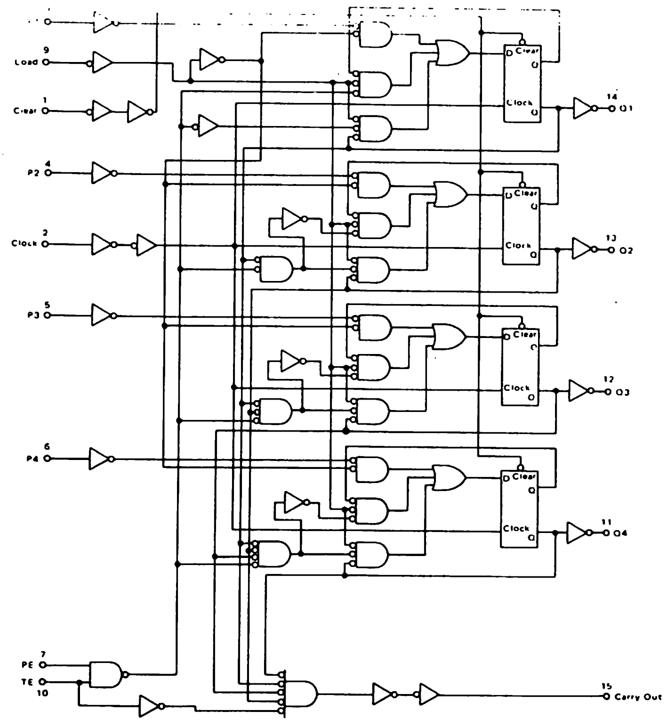
4160B, 4162B TIMING DIAGRAM



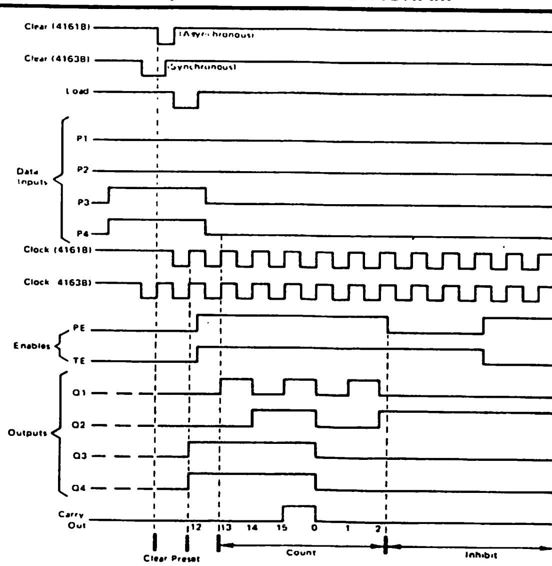
4161B, 4163B LOGIC DIAGRAM
(Clear is Synchronous for 4163B)

Sequence illustrated in waveforms:

1. Clear outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one and two.
4. Inhibit.



4161B, 4163B TIMING DIAGRAM



CMOS HEX TYPE D FLIP-FLOP

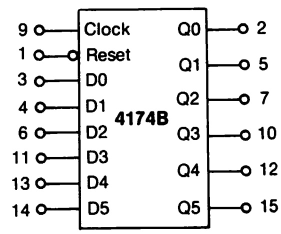
FEATURES:

- **Static Operation**
- **All Inputs and Outputs Buffered**
- **Diode Protection on All Inputs**
- **Supply Voltage Range = 3.0 Vdc to 18 Vdc**
- **Output Compatible with Two HTL Loads, Two Low-Power TTL Loads or One Low-Power Schottky TTL Load**
- **Functional Equivalent to TTL 74174**

DESCRIPTION:

The 4174B hex type D flip-flop is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Data on the D inputs which meets the setup time requirements is transferred to the Q ouptuts on the positive edge of the clock pulse. All six flip-flops share common clock and reset inputs. The reset is active low, and independent of the clock.

CONNECTION DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range—C, D, F, H E	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} < (V_{in}$ or $V_{out}) < V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

TRUTH TABLE
(Positive Logic)

INPUTS			OUTPUT	
Clock	Data	$\overline{\text{Reset}}$	Q	
↑	0	1	0	
↑	1	1	1	
↓	X	1	Q	No Change
X	X	0	0	

X = Don't Care

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	All Types Min	All Types Typ	All Types Max	Unit
Output Rise and Fall Time	t_r, t_f	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time—Clock to Q	t_{PLH}, t_{PHL}	5.0 10 15	— — —	150 70 50	300 140 100	ns
Propagation Delay Time—Reset to Q	t_{PHL}	5.0 10 15	— — —	250 100 75	500 200 150	ns
Minimum Clock Pulse Width	PW_C	5.0 10 15	— — —	75 45 35	150 90 70	ns
Minimum Reset Pulse Width	PW_R	5.0 10 15	— — —	100 50 40	200 100 80	ns
Maximum Clock Pulse Frequency	PRF	5.0 10 15	2.0 5.0 6.5	7.0 12.0 15.5	— — —	MHz
Maximum Clock Pulse Rise and Fall Time	t_r, t_f	5.0 10 15	15 15 15	— — —	— — —	µs
Data Setup Time	t_{setup}	5.0 10 15	— — —	20 10 0	40 20 15	ns
Data Hold Time	t_{hold}	5.0 10 15	— — —	40 20 15	80 40 30	ns
Reset Removal Time**	t_{rem}	5.0 10 15	— — —	125 50 40	250 100 80	ns

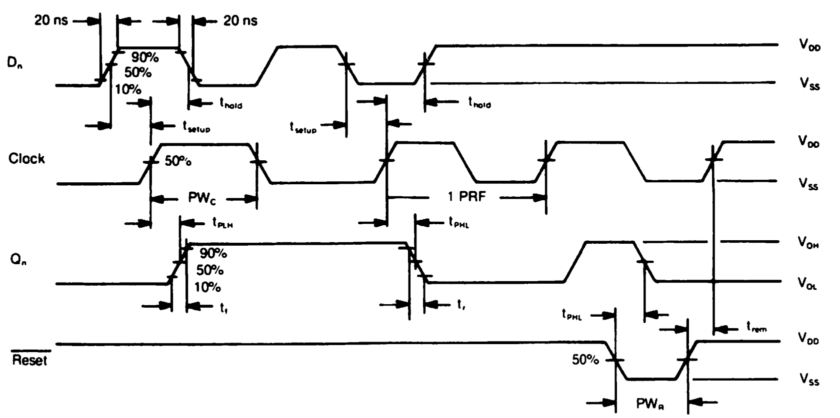
*The formulas given are for the typical characteristics only.
**The reset signal must be high prior to a positive-going transition of the clock.

STATIC CHARACTERISTICS [1]

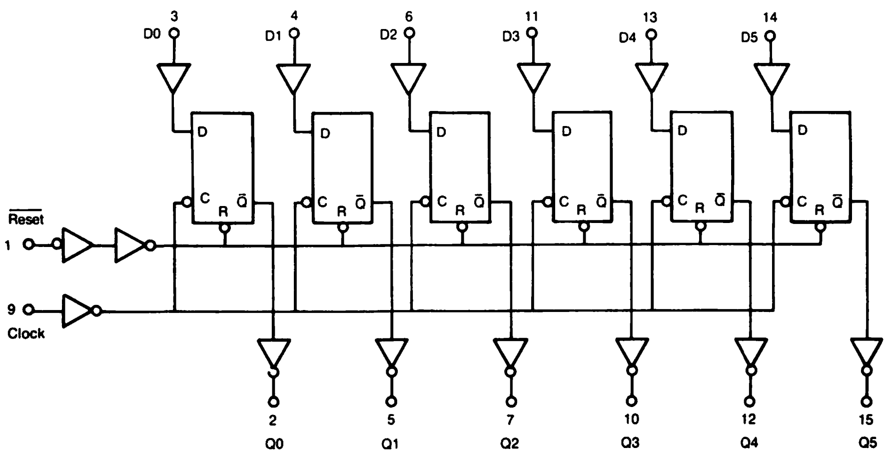
PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2] Min.	T_{LOW} [2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH} [2] Min.	T_{HIGH} [2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5 10 15	V_{IN} = V_{SS} or V_{DD} All valid input combinations	– – –	5 10 20	– – –	0.005 0.010 0.015	5 10 20	– – –	150 300 600	µAdc

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

TIMING DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



CMOS PRESETTABLE UP-DOWN COUNTERS
(Dual Clock with Reset)

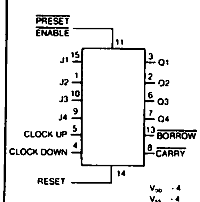
FEATURES:

- **Individual clock lines for counting up or counting down**
- **Synchronous high-speed carry and borrow propagation delays for cascading**
- **Asynchronous reset and preset capability**
- **Medium-speed operation—f_{CL} = 8 MHz (typ.) @ 10 V**

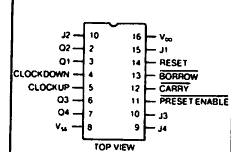
APPLICATIONS:

- **Up/down difference counting**
- **Multistage ripple counting**
- **Synchronous frequency dividers**
- **A/D and D/A conversion**
- **Programmable binary or BCD counting**

4192B, 4193B
FUNCTIONAL DIAGRAM



4192B, 4193B
TERMINAL ASSIGNMENT



DESCRIPTION:

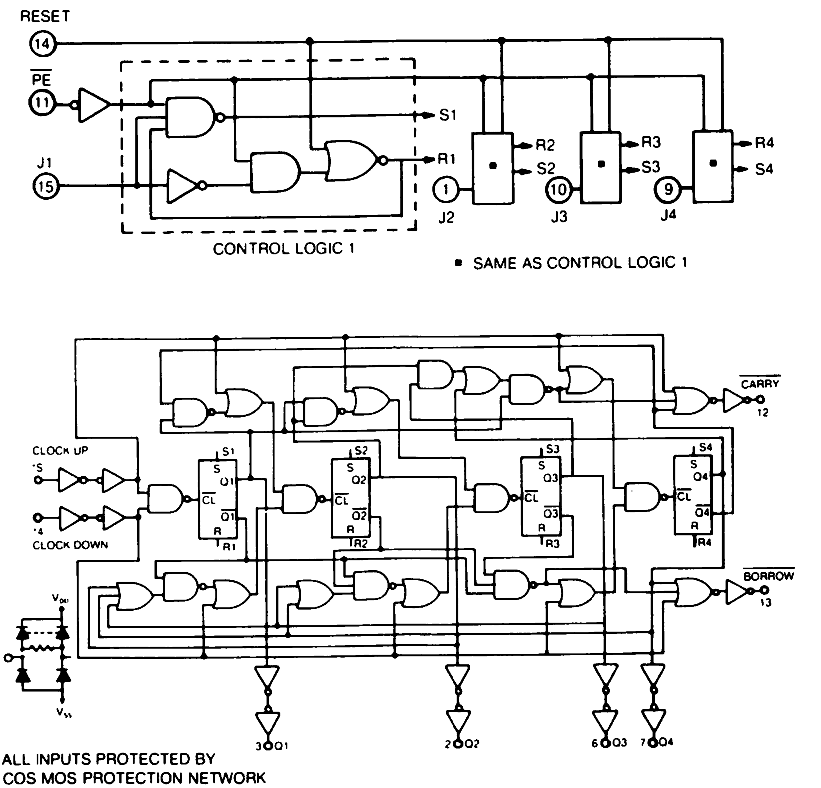
The SSS- 4192B Presettable BCD Up/Down Counter and the 4193B Presettable Binary Up/Down Counter each consist of 4 synchronously clocked, gated "D" type flip-flops connected as a counter. The inputs consist of 4 individual jam lines, a PRESET ENABLE control, individual CLOCK UP and CLOCK DOWN signals and a master RESET. Four buffered Q signal outputs as well as CARRY and BORROW outputs for multiple-stage counting schemes are provided.

The counter is cleared so that all outputs are in a low state by a high on the RESET line. A RESET is accomplished asynchronously with the clock. Each output is individually programmable asynchronously with the clock to the level on the corresponding jam input when the PRESET ENABLE control is low.

The counter counts up one count on the positive clock edge of the CLOCK UP signal provided the CLOCK DOWN line is high. The counter counts down one count on the positive clock edge of the CLOCK DOWN signal provided the CLOCK UP line is high.

The CARRY and BORROW signals are high when the counter is counting up or down. The CARRY signal goes low one-half clock cycle after the counter reaches its maximum count in the count-up mode. The BORROW signal goes low one-half clock cycle after the counter reaches its minimum count in the count-down mode. Cascading of multiple packages is easily accomplished without the need for additional external circuitry by tying the BORROW and CARRY outputs to the CLOCK DOWN and CLOCK UP inputs, respectively, of the succeeding counter package.

The 4192B and 4193B types are supplied in 16-lead hermetic dual-in-line ceramic packages (C and D suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (F suffix), and in chip form (H suffix).

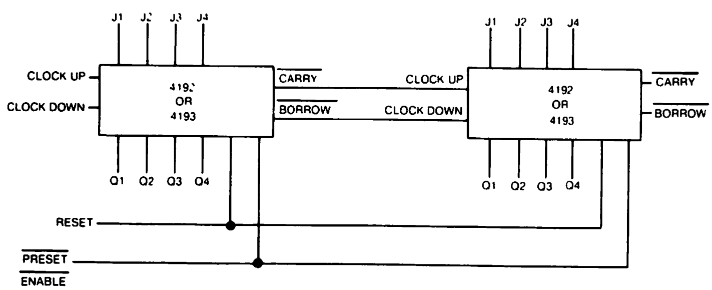


4192B logic diagram (BCD).

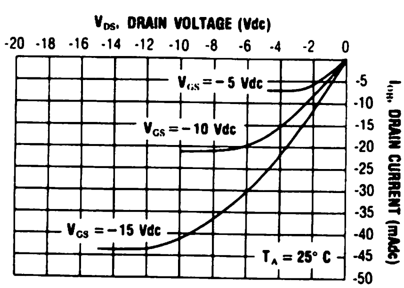
STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2]		+25°C			T_{HIGH} [2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN} = V_{SS}$ or V_{DD}	–	5	–	0.04	5	–	150	μAdc
		10	All valid input	–	10	–	0.04	10	–	300	
		15	combinations	–	20	–	0.04	20	–	600	

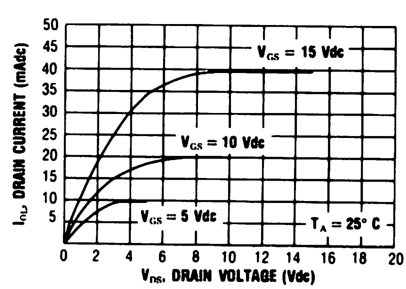
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.



Cascaded counter packages.



Typical P-Channel
Source Current Characteristics

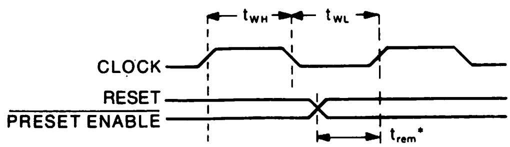


Typical N-Channel
Sink Current Characteristics

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		−55 to +125	°C
E Device		−40 to +85	°C



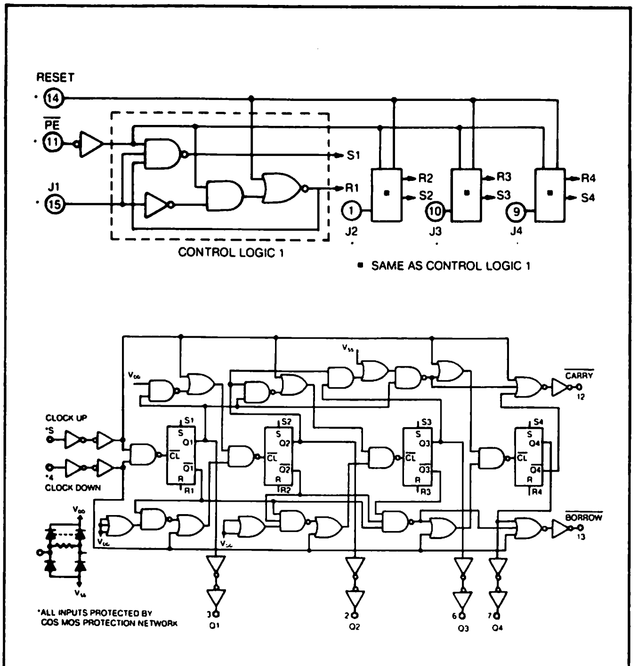
* RESET OR PRESET ENABLE REMOVAL TIME

Timing diagram defining t_{rem}

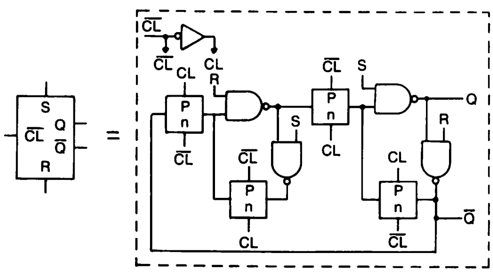
DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C
Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	V_{DD} (V)	LIMITS Min.	Typ.	Max.	UNITS
Propagation Delay Time t_{PHL}, t_{PLH}: CLOCK UP or CLOCK DOWN to Q, RESET to Q	5	—	250	500	ns
	10	—	120	240	
	15	—	90	180	
$\overline{\text{PE}}$ to Q	5	—	200	400	ns
	10	—	100	200	
	15	—	70	140	
CLOCK UP to $\overline{\text{CARRY}}$, CLOCK DOWN to $\overline{\text{BORROW}}$	5	—	160	320	ns
	10	—	80	160	
	15	—	60	120	
$\overline{\text{RESET}}$ or $\overline{\text{PE}}$ to $\overline{\text{BORROW}}$ or $\overline{\text{CARRY}}$	5	—	300	600	ns
	10	—	150	300	
	15	—	110	220	
Transition Time, t_{THL}, t_{TLH}	5	—	100	200	ns
	10	—	50	100	
	15	—	40	80	
Min. Removal Time, t_{rem}* RESET or PE	5	—	40	80	ns
	10	—	20	40	
	15	—	15	30	
Min. Pulse Width, t_W RESET	5	—	240	480	ns
	10	—	150	300	
	15	—	130	260	
$\overline{\text{PE}}$	5	—	120	240	ns
	10	—	85	170	
	15	—	70	140	
CLOCK	5	—	90	180	ns
	10	—	45	90	
	15	—	30	60	
Max. Clock Input Frequency, f_{CL}	5	2	4	—	MHz
	10	4	8	—	
	15	5.5	11	—	
Clock Rise & Fall time, t_r, t_f	5	—	—	15	µs
	10	—	—	15	
	15	—	—	5	
Input Capacitance, C_{IN}: RESET	—	—	10	15	pF
All Other Inputs	—	—	5	7.5	pF

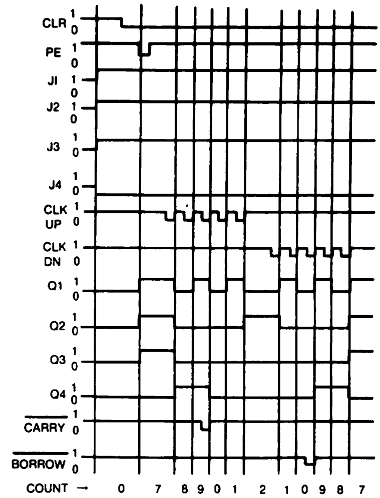
*The time required for RESET or PRESET ENABLE control to be removed before clocking (see timing diagram).



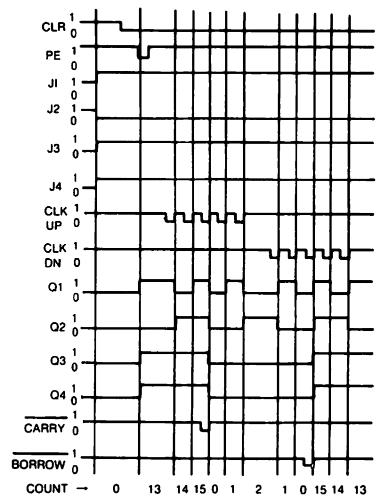
4193B logic diagram (binary).



Internal logic of Flip-flop.



4192B timing diagram.



4193B timing diagram.

TRUTH TABLE

CLOCK UP	CLOCK DOWN	$\overline{\text{PRESET ENABLE}}$	RESET	ACTION
_/‾	1	1	0	COUNT UP
‾_	1	1	0	NO COUNT
1	_/‾	1	0	COUNT DOWN
1	‾_	1	0	NO COUNT
X	X	0	0	PRESET
X	X	X	1	RESET

1 = HIGH LEVEL 0 = LOW LEVEL X = DON'T CARE

CMOS EXPANDABLE GATES

FEATURES

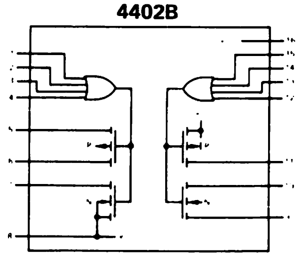
- Dual 4-Input Gates with Uncommitted Output Transistors
- Simplifies Construction of Combinational Logic Functions
- CMOS-to-TTL Interface Capability
- All Inputs Diode-Protected

DESCRIPTION

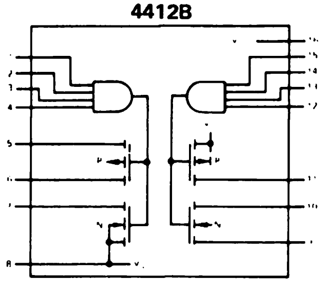
These devices are buffered Dual 4-input NOR Gates (4402B) and NAND Gates (4412B), with uncommitted output transistors. Gate expansion, complex combinational gating, and interface circuits can be constructed from these devices.

LOGIC DIAGRAMS

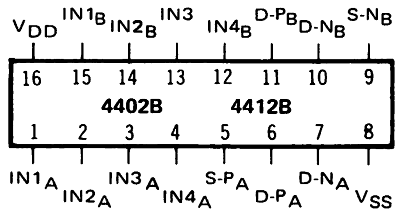
4402B



4412B



CONNECTION DIAGRAM
(all packages)



D = Drain
S = Source

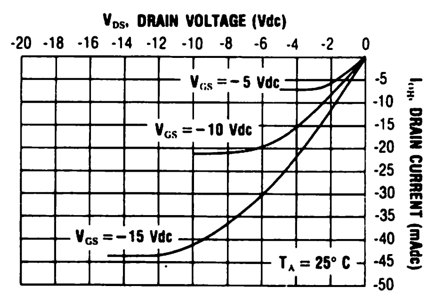
Add suffix for package:

C	16-pin Cerdip
D	16-pin Ceramic
E	16-pin Epoxy
F	16-pin Flat
H	Chip

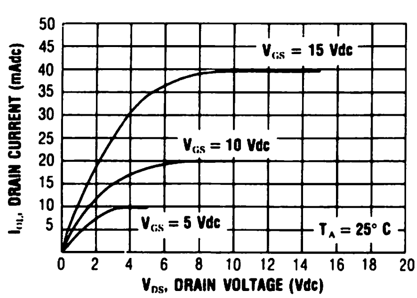
RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C



Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2] Min.	T_{LOW} [2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH} [2] Min.	T_{HIGH} [2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN} = V_{SS}$ or V_{DD}	–	0.05	–	0.0005	0.05	–	1.5	μAdc
		10	All valid input	–	0.10	–	0.001	0.10	–	3.0	
		15	combinations	–	0.20	–	0.002	0.20	–	6.0	

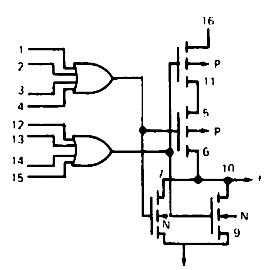
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

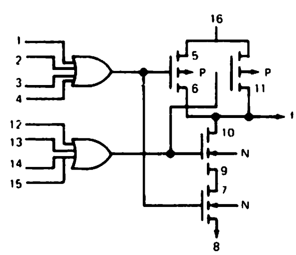
PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME Connected as Dual 4-Input Gates	t_{PLH}, t_{PHL}	5	–	125	250	ns
		10	–	60	120	
		15	–	45	90	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	

APPLICATIONS INFORMATION

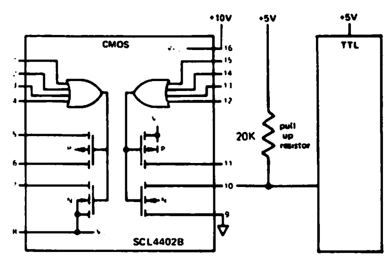
4402B



8-Input NOR Configuration
$f = \overline{1+2+3+4+12+13+14+15}$

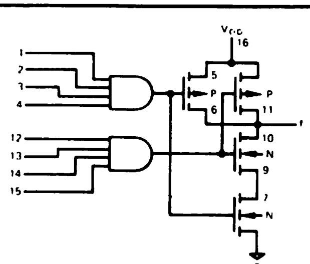


Dual 4-Input OR/NAND Gate
$f = \overline{(1+2+3+4)\cdot(12+13+14+15)}$

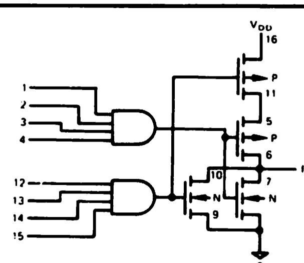


Interfacing CMOS to TTL

4412B



8-Input NAND
f 1 2 3 4 12 13 14 15



Dual 4-Input AND/NOR Gate
f (1 2 3 4) + (12 13 14 15)

For additional information, see Application Note AN-102.

CMOS 8-STAGE BINARY COUNTER

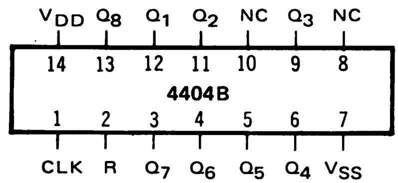
FEATURES

- 8-Stage Synchronous Counter
- Buffered Outputs from all 8 Stages
- Direct Reset
- Fully Static Operation – DC to 8MHz @ 10Vdc

DESCRIPTION

The 4404B consists of eight synchronous, single-phase clocked counting stages, with the Q output of each stage accessible. The counter is reset to all "zeroes" by a high level on the Reset line. Each stage of the counter utilizes a master-slave flip-flop configuration. The state of the counter is advanced one step in binary order on the negative-going transition of the input clock pulse.

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

C	14-pin Cerdip
D	14-pin Ceramic
E	14-pin Epoxy
F	14-pin Flat
H	Chip

TRUTH TABLE

CLOCK	RESET	OUTPUT STATE
↑	0	No Change
↓	0	Advance to next state
X	1	All Outputs are low

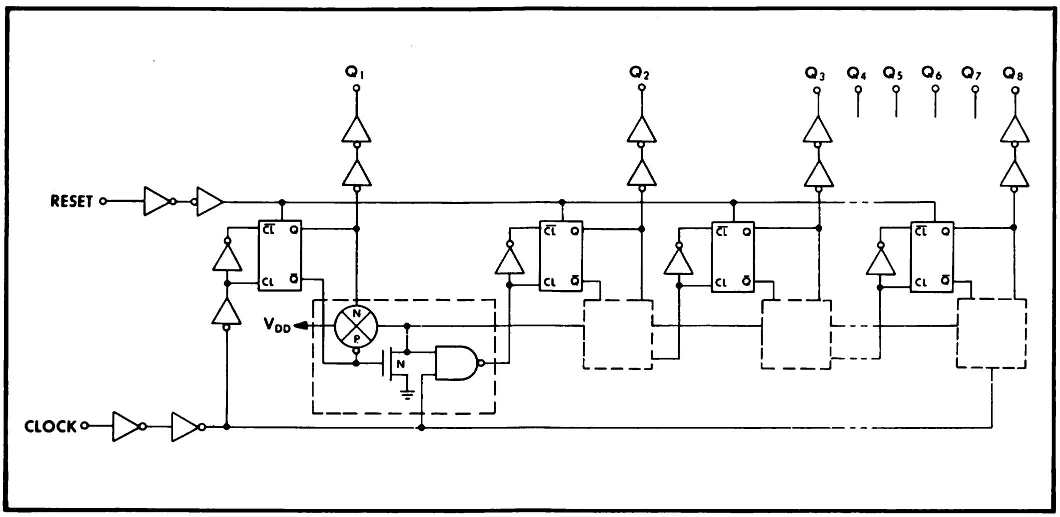
X = Don't Care

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

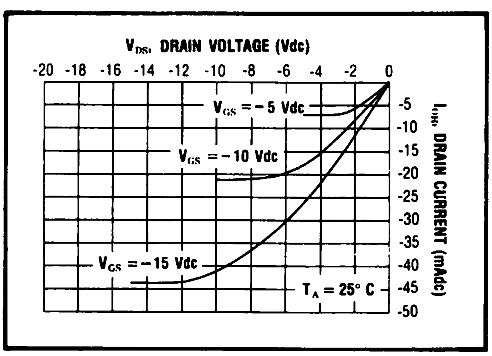
STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2] Min.	T_{LOW} [2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH} [2] Min.	T_{HIGH} [2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5 10 15	$V_{IN} = V_{SS}$ or V_{DD} All valid input combinations	– – –	5 10 20	– – –	0.05 0.1 0.2	5 10 20	– – –	150 300 600	μAdc

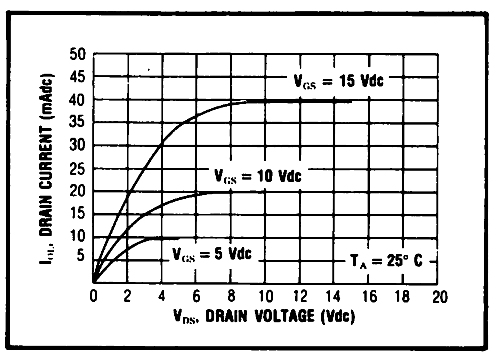
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = –55°C for C, D, F, H device.
= –40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}	5 10 15	– – –	250 125 100	500 250 200	ns
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5 10 15	– – –	100 50 40	200 100 80	ns
MINIMUM CLOCK PULSE WIDTH	PW_{CL}	5 10 15	– – –	125 65 50	250 130 100	ns
MAXIMUM CLOCK FREQUENCY	f_{CL}	5 10 15	2.0 4.0 5	4.0 8.0 10	– – –	MHz
MAXIMUM CLOCK RISE AND FALL TIME	t_{rCL}, t_{fCL}	5 10 15	15 5 3	– – –	– – –	μs
RESET OPERATION						
PROPAGATION DELAY TIME	t_{PHL}	5 10 15	– – –	175 75 60	350 150 120	ns
MINIMUM RESET PULSE WIDTH	PW_R	5 10 15	– – –	100 50 40	200 100 80	ns
RESET REMOVAL TIME	t_{rem}	5 10 15	– – –	200 90 65	400 180 130	ns



Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

CMOS QUAD ANALOG SWITCH

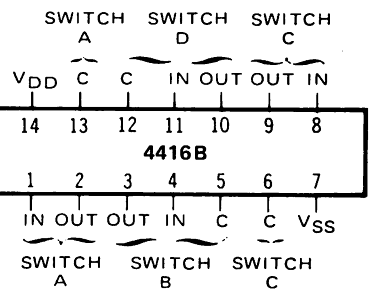
FEATURES

- DPDT Switch Operation Without External Logic
- Wide Range of Digital and Analog Signal Levels — Digital or Analog Signal to 18 Volts peak
- Low ON Resistance — 200 Ω typ. over $15V_{p-p}$ Signal Input Range, $V_{DD} - V_{SS} = 15V$
- Matched Switch Characteristics - 10 Ω typ. Difference Between R_{ON} Values at a Fixed Bias Point over 15 V_{p-p} Signal Input Range, $V_{DD} - V_{SS} = 15V$
- High "ON/OFF" Output Voltage Ratio — 65 dB typ. @ f_{is} = 10 kHz, R_L = 10 kΩ
- High Degree of Linearity — 0.4% Distortion typ. @ f_{is} = 1 kHz, V_{is} = 5 V_{p-p}, $V_{DD} - V_{SS}$ = 10V, R_L = 10 kΩ
- Extremely low OFF Switch Leakage Resulting in Very Low Offset Current and High Effective OFF Switch Resistance — 10 pA typ. @ $V_{DD} - V_{SS}$ = 10V, T_A = 25° C
- Extremely High Control Input Impedance (Control Circuit Isolated from Signal Circuit) — 10^{12}Ω typ.
- Low Crosstalk Between Switches — -50dB typ. @ f_{is} = 0.9 MHz, R_L = 1kΩ
- Matched Control-Input to Signal-Output Capacitances - Reduces Output Signal Transients
- Transmits Frequencies up to 40MHz

DESCRIPTION

The 4416B is a single-chip monolithic silicon integrated circuit containing eight N-channel and eight P-channel enhancement-mode MOS transistors connected to from four independent bilateral signal switches. Each switch consists of both P- and N-channel devices with common source and drain connections. A single control signal is required per switch. Both P and N devices in a given switch are biased ON or OFF by the control signal.

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

C	14-pin Cerdip	F	14-pin Flat
D	14-pin Ceramic	H	Chip
E	14-pin Epoxy		

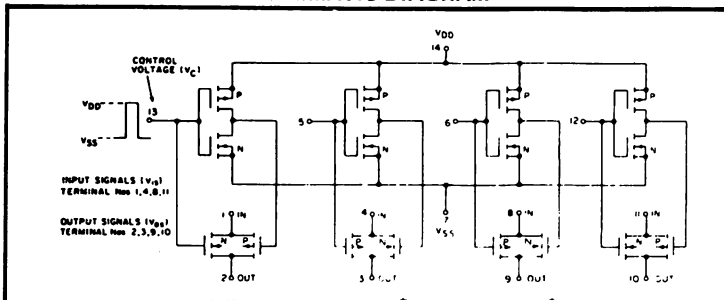
RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

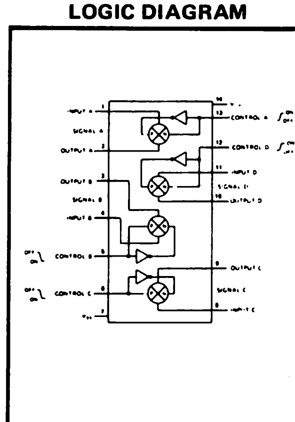
The CMOS switch permits peak input-signal voltage swings equal to the full supply voltage, a considerable advantage over single-channel types. When the control input is high the switch will be ON. When the control input is low the switch will be OFF.

SCHEMATIC DIAGRAM



NOTE:
All switch P-channel substrates are internally connected to terminal No. 14.
All switch N-channel substrates are internally connected to terminal No. 7.
***Note the difference from the 4016B**

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS[1]

PARAMETER		CONDITIONS	V_{IS}	V_{SS} (Vdc)	V_{DD} (Vdc)	T_{LOW}[2] Min.	T_{LOW}[2] Max.	25°C Min.	25°C Typ.	25°C Max.	T_{HIGH}[2] Min.	T_{HIGH}[2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	$V_{IN} = V_{SS}$ or V_{DD} All valid input combinations		0	5	–	0.05	–	0.0005	0.05	–	1.5	µAdc
				0	10	–	0.1	–	0.001	0.1	–	3.0	
				0	15	–	0.2	–	0.002	0.2	–	6.0	
MINIMUM INPUT HIGH VOLTAGE (Control Input)	V_{IH}	$V_{IS} = V_{SS}$ $V_{OS} = V_{DD}$ $I_{OS} = 10\mu A$		0	5	–	2.9	–	1.5	2.7	–	2.4	Vdc
				0	10	–	2.9	–	1.5	2.7	–	2.4	
				0	15	–	2.9	–	1.5	2.7	–	2.4	
MAXIMUM INPUT LOW VOLTAGE (Control Input)	V_{IL}	$V_{IS} = V_{SS}$ $V_{OS} = V_{DD}$ $I_{OS} = 10\mu A$		0	5	0.9	–	0.7	1.5	–	0.4	–	Vdc
				0	10	0.9	–	0.7	1.5	–	0.4	–	
				0	15	0.9	–	0.7	1.5	–	0.4	–	
SWITCH INPUT/OUTPUT LEAKAGE (Switch off)	I_{OFF}	$V_C = V_{SS}$[4]	±7.5	-7.5	+7.5	–	±250	–	±0.1	±250	–	±2500	nAdc
			±5	-5	+5	–	±125	–	±0.01	±125	–	±1250	
ON-RESISTANCE	R_{ON}	$V_C = V_{DD}$[4] $R_L = 10k\Omega$	+7.5	-7.5	+7.5	–	200	–	100	220	–	450	Ω
			-7.5			–	200	–	100	220	–	450	
			±0.25			–	180	–	80	200	–	420	
			+5	-5	+5	–	260	–	160	300	–	500	Ω
			-5			–	260	–	160	300	–	500	
			±0.25			–	260	–	150	290	–	500	
			+15	0	+15	–	230	–	130	250	–	500	Ω
			+0.25			–	100	–	40	120	–	260	
			+9.3			–	250	–	150	270	–	580	
			+10	0	+10	–	220	–	120	240	–	500	Ω
			+0.25			–	100	–	60	130	–	280	
			+5.6			–	400	–	220	420	–	900	
ON-RESISTANCE MATCH (Same package)	ΔR_{ON}	$V_C = V_{DD}$[4] $R_L = 10k\Omega$	±7.5	-7.5	+7.5	–	–	–	10	–	–	–	Ω
			±5	-5	+5	–	–	–	15	–	–	–	

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

[4] Reverse polarity of V_C (control input) for switches B and C.

DYNAMIC CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

PARAMETER		CONDITIONS	R_L	V_{SS} (Vdc)	V_{DD} (Vdc)	Min.	Typ.	Max.	Units
SIGNAL INPUTS (V_{IS}) AND OUTPUTS (V_{OS})									
PROPAGATION DELAY TIME Signal input to signal output	t_{PLH}, t_{PHL}	$V_C = V_{DD}$[1] V_{IS} = square wave $R_L = 10k\Omega$		0	5	–	20	40	ns
				0	10	–	10	20	
				0	15	–	7.5	15	
BANDWIDTH (-3dB) (Sine Wave)	BW	$V_C = V_{DD}$[1] $V_{IS} = 5V_{p\text{-}p}$ centered @0.0Vdc	1kΩ	-5	+5	–	54	–	MHz
			10kΩ			–	40	–	
			100kΩ			–	38	–	
			1MΩ			–	37	–	

ELECTRICAL CHARACTERISTICS (Continued)

DYNAMIC CHARACTERISTICS (C_L = 50 pF, T_A = 25°C) (Continued)

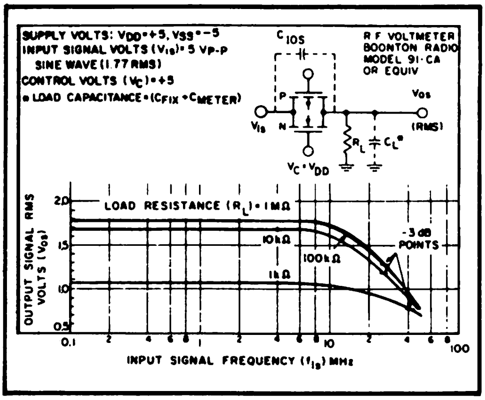
PARAMETER		CONDITIONS	R_L	V_{SS} (Vdc)	V_{DD} (Vdc)	Min.	Typ.	Max.	Units
SIGNAL INPUTS (V_{IS}) AND OUTPUTS (V_{OS}) (Continued)									
INSERTION LOSS (= 20 log$_{10}$ $\frac{V_{OS}}{V_{IS}}$)		V_C = V_{DD}[1] V_{IS} = 5$V_{p\text{-}p}$ centered @0.0Vdc	1kΩ	-5	+5	–	2.3	–	dB
			10kΩ			–	0.2	–	
			100kΩ			–	0.1	–	
			1MΩ			–	0.05	–	
SIGNAL DISTORTION (Sine Wave)		V_C = V_{DD}[1] V_{IS} = 5$V_{p\text{-}p}$ centered @0.0Vdc f_{IS} = 1.0kHz R_L = 10kΩ		-5	+5	–	0.4	–	%
FEEDTHROUGH (-50dB)		V_C = V_{SS}[1] V_{IS} = 5$V_{p\text{-}p}$ centered @0.0Vdc	1kΩ	–5	+5	–	1250	–	kHz
			10kΩ			–	140	–	
			100kΩ			–	18	–	
			1MΩ			–	2	–	
CROSSTALK (-50dB) (Between two switches)		V_C (A) = V_{DD}[1] V_C (B) = V_{SS}[1] V_{IS}(A) = 5$V_{p\text{-}p}$ centered @0.0Vdc R_L = 1.0k		-5	+5	–	0.9	–	MHz
CAPACITANCE Input	C_{IS}	V_C = V_{SS}[1]		-5	+5	–	4	–	pF
Output	C_{OS}					–	4	–	pF
Feedthrough	C_{IOS}					–	0.2	–	pF
CONTROL INPUT (V_C)									
PROPAGATION DELAY TIME Turn on	t_{PLH}, t_{PHL}	$V_{SS} \leq V_{IS} \leq V_{DD}$ R_L = 10kΩ		0	5	–	40	80	ns
				0	10	–	20	40	
				0	15	–	15	30	
MAXIMUM INPUT FREQUENCY	f_C	$V_{SS} \leq V_{IS} \leq V_{DD}$ R_L = 1.0kΩ		0	5	–	5	–	MHz
				0	10	–	10	–	
				0	15	–	12	–	
CROSSTALK (To signal port)		V_C = Square wave R_L = 10kΩ R_{IN} = 1.0kΩ		0	5	–	30	–	mV
				0	10	–	50	–	
				0	15	–	100	–	

NOTE: [1] Reverse polarity of Vc (control input) for switches B and C.

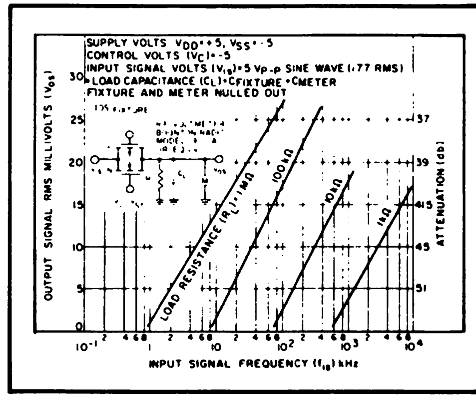
TYPICAL ON-RESISTANCE CHARACTERISTICS

CHARACTERISTIC*	SUPPLY CONDITIONS		LOAD CONDITIONS					
			R_L = 1kΩ		R_L = 10kΩ		R_L = 100kΩ	
	V_{DD} (V)	V_{SS} (V)	VALUE (Ω)	V_{is} (V)	VALUE (Ω)	V_{is} (V)	VALUE (Ω)	V_{is} (V)
R_{ON}	+15	0	200	+15	200	+15	180	+15
			200	0	200	0	200	0
R_{ON}(max.)	+15	0	300	+11	300	+9.3	320	+9.2
R_{ON}	+10	0	290	+10	250	+10	240	+10
			290	0	250	0	300	0
R_{ON}(max.)	+10	0	500	+7.4	560	+5.6	610	+5.5
R_{ON}	+ 5	0	560	+ 5	470	+ 5	450	+ 5
			600	0	580	0	800	0
R_{ON}(max.)	+ 5	0	1.7k	+4.2	7k	+2.9	33k	+2.7
R_{ON}	+7.5	–7.5	200	+7.5	200	+7.5	180	+7.5
			200	–7.5	200	–7.5	180	–7.5
R_{ON}(max.)	+7.5	–7.5	290	±0.25	280	±25	400	±0.25
R_{ON}	+ 5	– 5	280	+ 5	250	+ 5	240	+ 5
			310	– 5	250	– 5	240	– 5
R_{ON}(max.)	+ 5	– 5	600	±0.25	580	±0.25	760	±0.25
R_{ON}	+2.5	–2.5	590	+2.5	450	+2.5	490	+2.5
			720	–2.5	520	–2.5	520	–2.5
R_{ON}(max.)	+2.5	–2.5	232k	±0.25	300k	±0.25	870k	±0.25

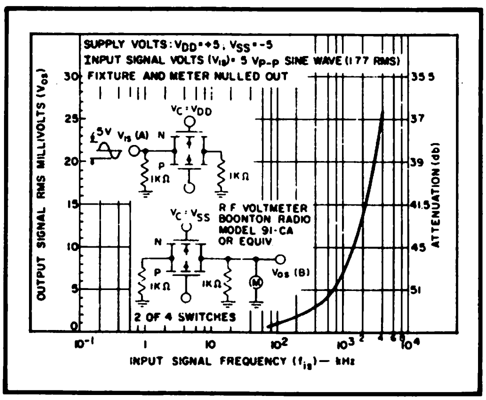
* Variation from a perfect switch; R_{ON} = 0Ω.



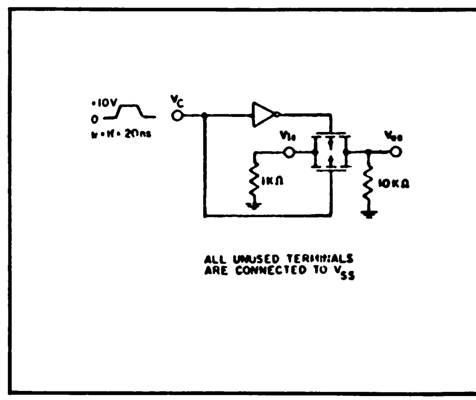
Typ. switch frequency response - switch "ON"



Typ. feedthru vs. freq. — switch "OFF"



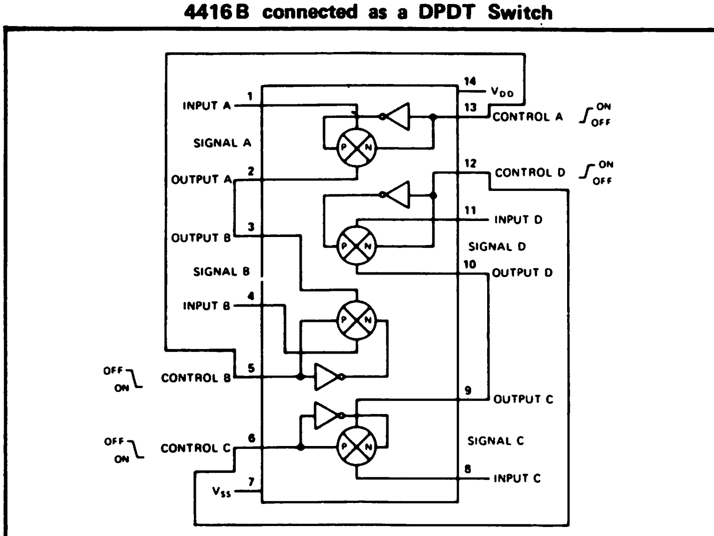
Typ. crosstalk between switch circuits in the same package



Test circuit, Crosstalk-control input to signal output.

APPLICATIONS INFORMATION

4416B connected as a DPDT Switch



CMOS DECADE COUNTER/7-SEGMENT DECODER/DRIVERS

FEATURES

- **Monolithic Construction of Bipolar Transistors on Outputs Allow Direct Display Drive**
- **Decade Counter and 7-Segment Decoder in One Package**
- **Direct Reset**
- **Display Enable Function (4426AB)**
- **Ripple Blanking and Lamp Test Functions (4433AB)**
- **Trigger from either Edge of Clock Input**
- **Carry Output for Cascading Stages**
- **Fully Static Operation - DC to 5MHz @ 10Vdc**

DESCRIPTION

These two devices each consist of a 5-stage Johnson decade counter and an output decoder which converts the Johnson code to a 7-segment decoded output for driving each stage in a numerical display. A "high" Reset signal clears the decade counter to its zero count. The counters have interchangeable Clock and Clock Enable lines for incrementing on either a positive-going or negative-going transition, respectively. Antilock gating is provided on the Johnson counter, thus assuring proper counting sequence. The Carry-Out (C_{OUT}) signal completes one cycle every ten clock input cycles and is used to directly clock the succeeding decade in a multi-decade counting chain.

4426AB

When the Display Enable is "low" the seven decoded outputs are forced off regardless of the state of the counter. Activation of the display only when required results in significant power savings. This system also facilitates implementation of display-character multiplexing.

The Carry Out and ungated "C-segment" signals are not gated by the Display Enable and therefore are available continuously. This feature is a requirement in implementation of certain divider functions such as divide-by-60 and divide-by-12.

4433AB

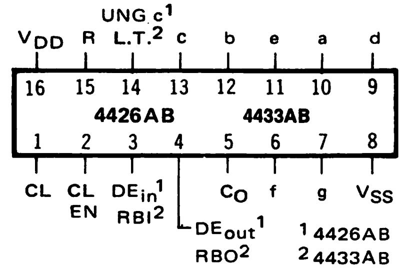
The 4433AB has provisions for automatic blanking of the nonsignificant zeros in a multi-digit decimal number which results in an easily readable display consistent with normal writing practice. For example, the number 0050.0700 in an eight-digit display would be displayed as 50.07. Zero suppression on the integer side is obtained by connecting the RBI terminal of the 4433AB associated with the most significant digit in the display to a "low-level" voltage and connecting the RBO terminal of that stage to the RBI terminal of the 4433AB in the next-lower significant position in the display. This procedure is continued for each succeeding 4433AB on the integer side of the display. On the fraction side of the display the RBI of the 4433AB associated with the least significant digit is connected to a "low level" voltage and the RBO of the 4433AB is connected to the RBI terminal of the 4433AB in the next more-significant-digit position. Again, this procedure is continued for all 4433AB on the fraction side of the display.

In a purely fractional number the zero immediately preceding the decimal point can be displayed by connecting the RBI of that stage to a "high-level" voltage (instead of to the RBO of the next more-significant stage). For Example: optional zero - 0.7346.

Likewise, the zero in a number such as 736.0 can be displayed by connecting the RBI of the 4433AB associated with it to a "high-level" voltage.

A "high" Lamp Test signal turns on all outputs.

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

C	16-pin Cerdip	F	16-pin Flat
D	16-pin Ceramic	H	Chip
E	16-pin Epoxy		

RECOMMENDED OPERATING CONDITIONS

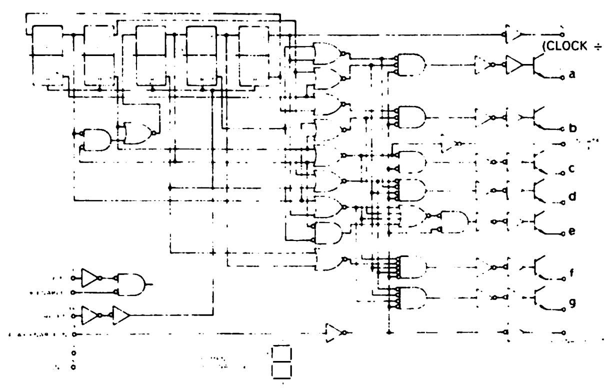
For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

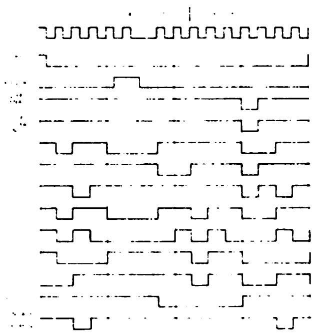
BIPOLAR OUTPUTS

These devices are functionally and pin-for-pin interchangeable with all CMOS device types 4026AB and 4433AB. All counting and decoding in 4426AB and 4433AB devices is implemented with CMOS transistor circuitry. In order to furnish higher output drive for applications such as driving LED's, bipolar Darlington transistors have been furnished at each display drive output.

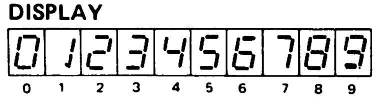
LOGIC DIAGRAM



TIMING DIAGRAM



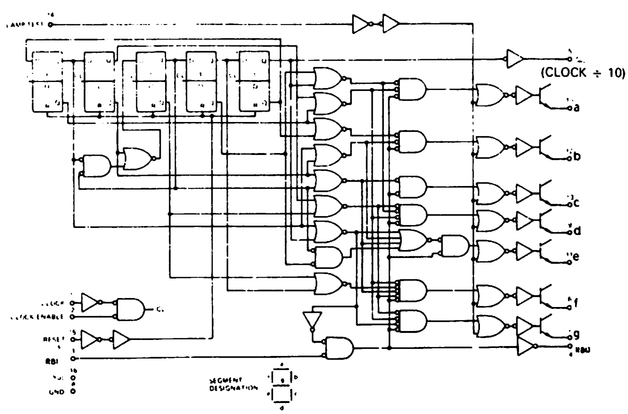
DISPLAY



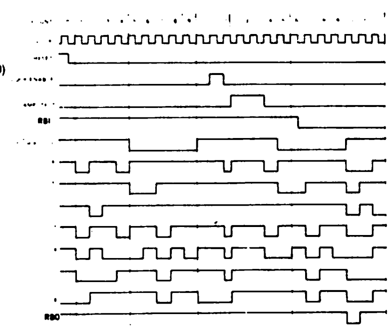
Collector of each output transistor internally tied to V_{DD}.

4426AB Decade Counter/7-Segment Decoder/Driver with Display Enable.

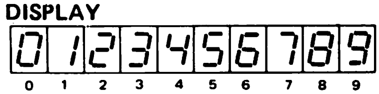
LOGIC DIAGRAM



TIMING DIAGRAM



DISPLAY



Collector of each output transistor internally tied to V_{DD}.

4433B Decade Counter/7-Segment Decoder/Driver with Ripple Blanking.

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS [1,3]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[2] Min.	T_{LOW}[2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH}[2] Min.	T_{HIGH}[2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN} = V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	µAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		15	combinations	–	15	–	0.2	20	–	600	
HIGH LEVEL OUTPUT VOLTAGE Decoded Outputs	V_{OH}	5	$V_{IN} = V_{SS}$ or V_{DD}	4.25	–	4.25	–	–	4.25	–	Vdc
		10		9.25	–	9.25	–	–	9.25	–	
		15	$\lvert I_O \rvert < 1\mu A$	14.25	–	14.25	–	–	14.25	–	
MINIMUM INPUT HIGH VOLTAGE	V_{IH}	5	$V_O = 0.5V$ or 4.25V	–	3.75	–	2.75	3.75	–	3.75	Vdc
		10	$V_O = 1.0V$ or 9.0V	–	7.5	–	5.5	7.5	–	7.5	
		15	$V_O = 1.5V$ or 13.5V $\lvert I_O \rvert < 1\mu A$	–	11.25	–	8.25	11.25	–	11.25	
MAXIMUM INPUT LOW VOLTAGE	V_{IL}	5	$V_O = 0.5V$ or 4.25V	1.25	–	1.25	2.25	–	1.25	–	Vdc
		10	$V_O = 1.0V$ or 9.0V	2.5	–	2.5	4.5	–	7.5	–	
		15	$V_O = 1.5V$ or 13.5V $\lvert I_O \rvert < 1\mu A$	3.75	–	3.75	6.75	–	3.75	–	
OUTPUT HIGH (SOURCE) CURRENT Decoded Outputs[3]	I_E	5	$V_{OH} = 3.5V$	–	–	-15	-25	–	–	–	mAdc
		10	$V_{OH} = 8.5V$	–	–	–	-60	–	–	–	
		15	$V_{OH} = 13.5V$	–	–	–	-100	–	–	–	
Carry Output	I_{OH}	5	$V_{OH} = 4.6V$	-0.10	–	-0.10	-0.4	–	-0.07	–	mAdc
		10	$V_{OH} = 9.5V$	-0.30	–	-0.30	-1.0	–	-0.20	–	
		15	$V_{OH} = 13.5V$ $V_{IN} = V_{SS}$ or V_{DD}	-0.90	–	-0.90	-4.0	–	-0.65	–	
Remaining Outputs		5	$V_{OH} = 4.6V$	-0.08	–	-0.08	-0.2	–	-0.06	–	mAdc
		10	$V_{OH} = 9.5V$	-0.20	–	-0.20	-0.5	–	-0.14	–	
		15	$V_{OH} = 13.5V$ $V_{IN} = V_{SS}$ or V_{DD}	-0.60	–	-0.60	-1.5	–	-0.42	–	
OUTPUT LOW (SINK) CURRENT Carry Output	I_{OL}	5	$V_{OL} = 0.4V$	-0.10	–	-0.10	0.4	–	-0.07	–	mAdc
		10	$V_{OL} = 0.5V$	-0.30	–	-0.30	1.0	–	-0.20	–	
		15	$V_{OL} = 1.5V$ $V_{IN} = V_{SS}$ or V_{DD}	-0.90	–	-0.90	4.0	–	-0.65	–	
Remaining Outputs		5	$V_{OL} = 0.4V$	0.13	–	-0.08	0.25	–	-0.06	–	mAdc
		10	$V_{OL} = 0.5V$	0.31	–	-0.20	0.6	–	-0.14	–	
		15	$V_{OL} = 1.5V$ $V_{IN} = V_{SS}$ or V_{DD}	1.43	–	-0.60	2.5	–	-0.42	–	

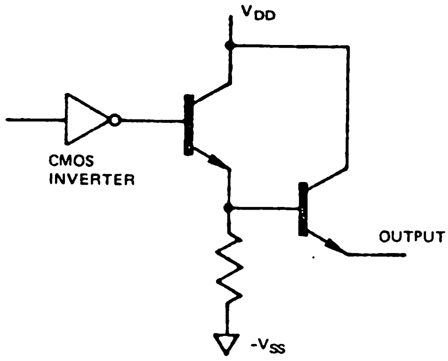
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.
[3] Observe Package Power Dissipation rating.

ELECTRICAL CHARACTERISTICS (Continued)

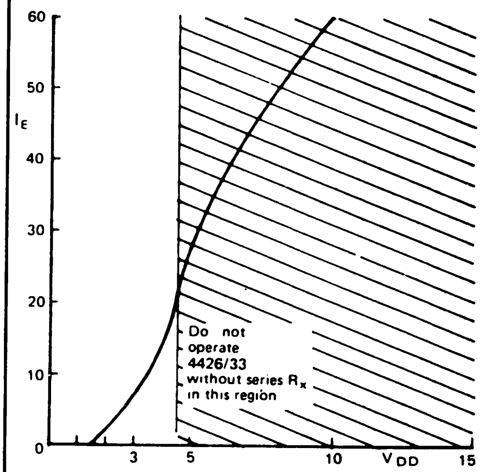
DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME Clock to Decoded Outputs	t_{PLH}, t_{PHL}	5 10 15	– – –	850 250 200	1700 500 400	ns
Clock to Carry Out	t_{PLH}, t_{PHL}	5 10 15	– – –	500 125 100	1000 250 200	ns
OUTPUT TRANSITION TIME Decoded Outputs	t_{TLH}, t_{THL}	5 10 15	– – –	450 200 150	900 400 300	ns
Carry Output	t_{TLH}, t_{THL}	5 10 15	– – –	250 125 100	500 250 200	ns
MINIMUM CLOCK OR ENABLE PULSE WIDTH	PW_{CL}, PW_{CE}	5 10 15	– – –	200 100 80	400 200 160	ns
MAXIMUM CLOCK FREQUENCY	f_{CL}	5 10 15	1.25 2.5 3.0	2.5 5.0 6.0	– – –	MHz
MAXIMUM CLOCK OR ENABLE RISE AND FALL TIME	t_{rCL}, t_{fCL}	5 10 15	15 15 3	– – –	– – –	μs
MINIMUM CLOCK OR ENABLE SETUP TIME	t_{setup}	5 10 15	– – –	250 100 80	500 200 160	ns
RESET OPERATION						
PROPAGATION DELAY TIME Reset to Decoded Outputs	t_{PLH}, t_{PHL}	5 10 15	– – –	700 250 200	1400 500 400	ns
Reset to Carry Output	t_{PLH}, t_{PHL}	5 10 15	– – –	500 125 100	1000 250 200	ns
MINIMUM RESET PULSE WIDTH	PW_R	5 10 15	– – –	200 100 80	400 200 160	ns
RESET REMOVAL TIME	t_{rem}	5 10 15	– – –	375 150 125	750 300 250	ns

OUTPUT NETWORK

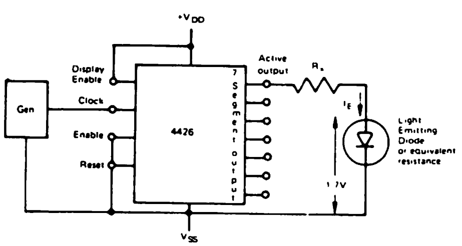


The darlington NPN transistor network shown is typical of each of seven segment drive outputs per integrated circuit.

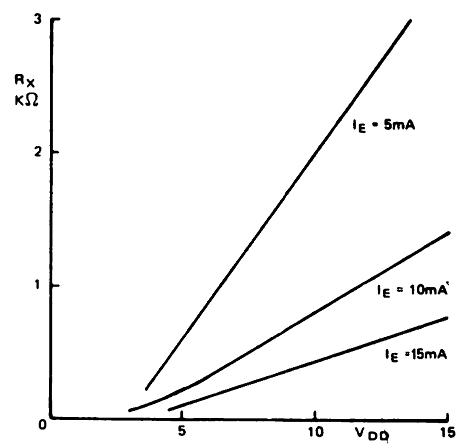


Typical Output Current per Segment vs. Supply Voltage.

DISPLAY INTERFACE



Typical Display Connection



R_x required to limit LED Current

CMOS BINARY-TO-OCTAL DECODER

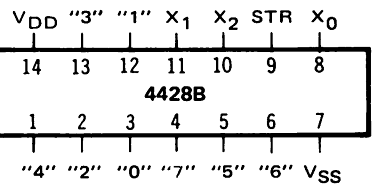
FEATURES

- Binary-to-Octal Decoding
- Buffered Outputs Go High on Selection
- Strobe Input for Simple Expansion

DESCRIPTION

The 4428B is a one-of-eight CMOS Strobed Decoder. The three inputs labeled X_0, X_1, and X_2, constitute a three-bit word which defines a number from 0 to 7, and activates one of eight outputs of the decoder. The Strobe line inhibits the outputs from responding to the inputs. If the Strobe line is a logic "1", one of eight outputs is a logic "1". This is an important feature of the Strobe since many 4428B's may be cascading to produce a 1 or N X 8 strobed decoder. This array is particularly useful in expanding memory systems.

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

C 14-pin Cerdip
D 14-pin Ceramic
E 14-pin Epoxy
F 14-pin Flat
H Chip

TRUTH TABLE – Strobe at Logical 1

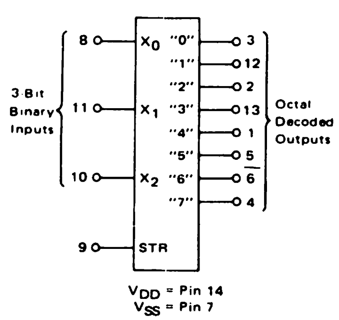
	Address Input			Output							
	X_2	X_1	X_0	"0"	"1"	"2"	"3"	"4"	"5"	"6"	"7"
PIN	10	11	8	3	12	2	13	1	5	6	4
	0	0	0	1	0	0	0	0	0	0	0
	0	0	1	0	1	0	0	0	0	0	0
	0	1	0	0	0	1	0	0	0	0	0
	0	1	1	0	0	0	1	0	0	0	0
	1	0	0	0	0	0	0	1	0	0	0
	1	0	1	0	0	0	0	0	1	0	0
	1	1	0	0	0	0	0	0	0	1	0
	1	1	1	0	0	0	0	0	0	0	1

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

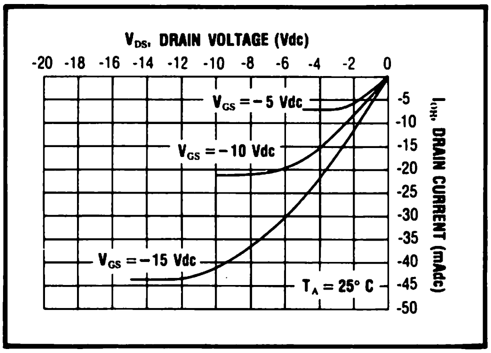
STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2] Min.	T_{LOW} [2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH} [2] Min.	T_{HIGH} [2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5 10 15	$V_{IN} = V_{SS}$ or V_{DD} All valid input combinations	– – –	5 10 20	– – –	0.05 0.1 0.2	5 10 20	– – –	150 300 600	μAdc

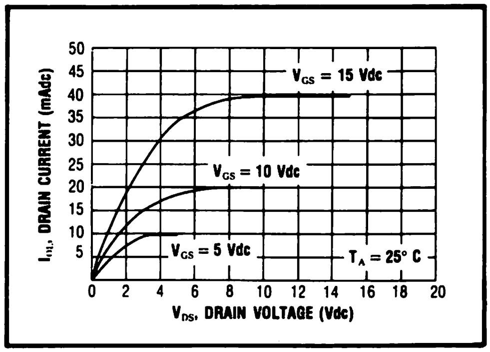
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETERS		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}	5 10 15	– – –	225 100 70	450 200 140	ns
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5 10 15	– – –	100 50 40	200 100 80	ns

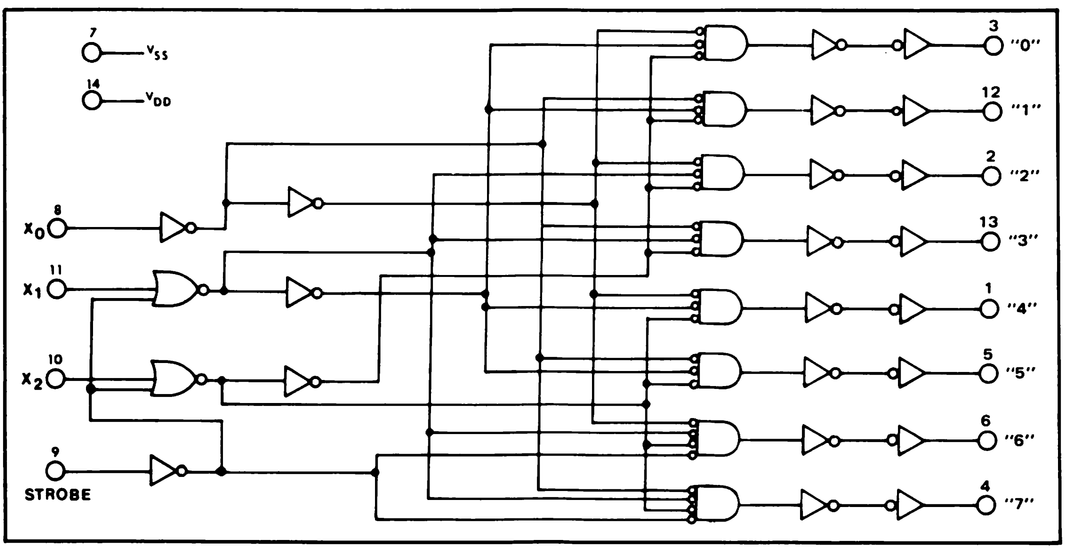


Typical P-Channel
Source Current Characteristics



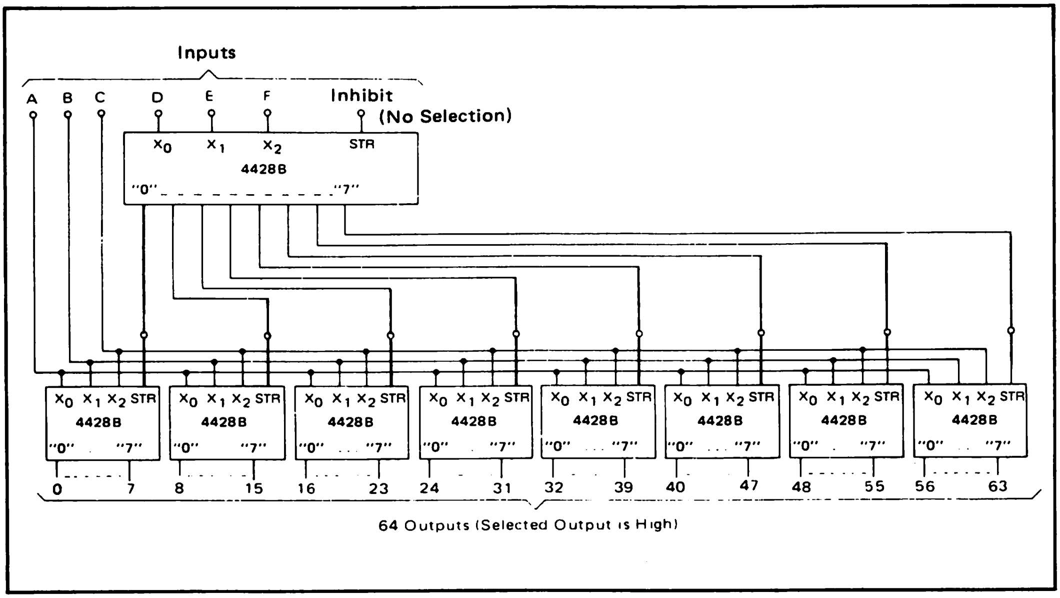
Typical N-Channel
Sink Current Characteristics

LOGIC DIAGRAM



APPLICATIONS INFORMATION

SIX-BIT BINARY 1-OF-64 DECODER



CMOS QUAD BUFFER-DRIVER

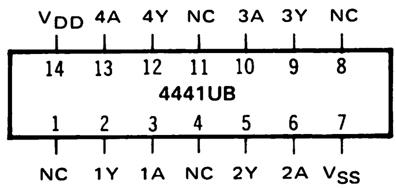
FEATURES

- Symmetrical High-Current Outputs
- High-Speed Operation with Large Capacitive Loads
- Low Output Impedance
- Diode Protection on all Inputs

DESCRIPTION

The 4441UB is a monolithic N-channel and P-channel enhancement-mode integrated circuit consisting of four large buffers for very high current capability. This device is useful as a line driver, low-power resistor-network driver for A/D and D/A conversion, display and clock drivers.

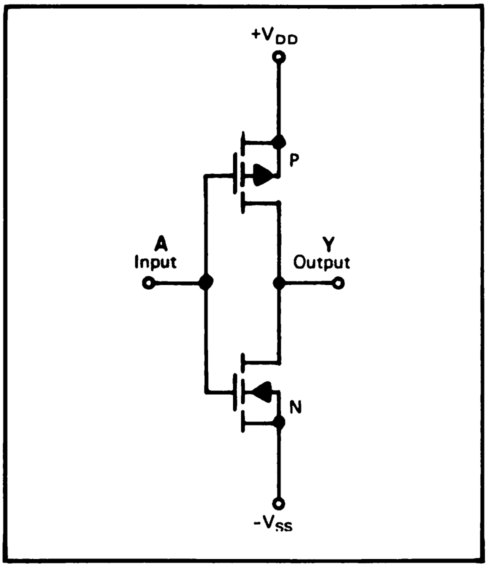
CONNECTION DIAGRAM
(all packages)



Add suffix for package:

C	14-pin Cerdip	F	14-pin Flat
D	14-pin Ceramic	H	Chip
E	14-pin Epoxy		

SCHEMATIC DIAGRAM
(one of four buffers)

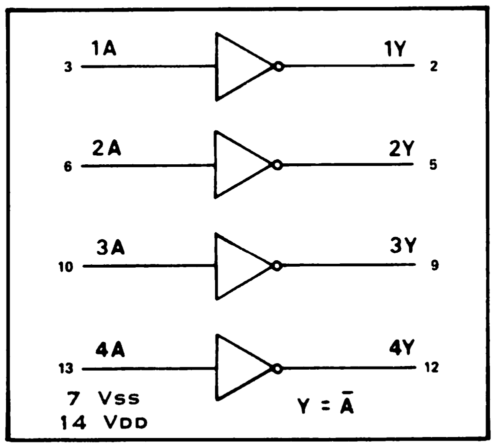


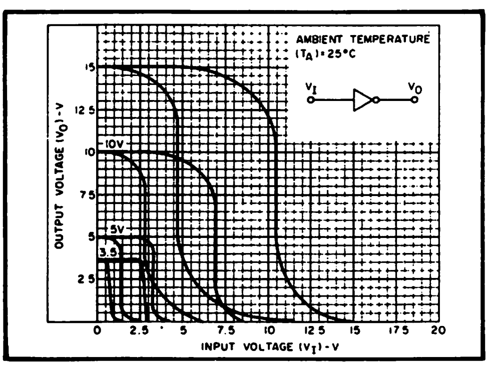
RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

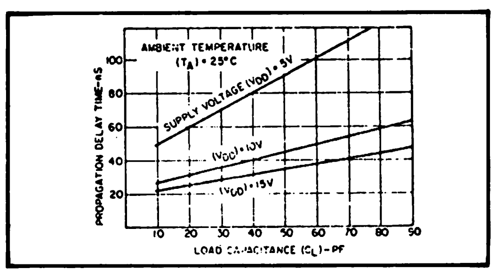
DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	^{o}C
E Device		-40 to +85	^{o}C

LOGIC DIAGRAM





Minimum and maximum transfer characteristics.



Typical propagation delay time vs. C_L

ELECTRICAL CHARACTERISTICS

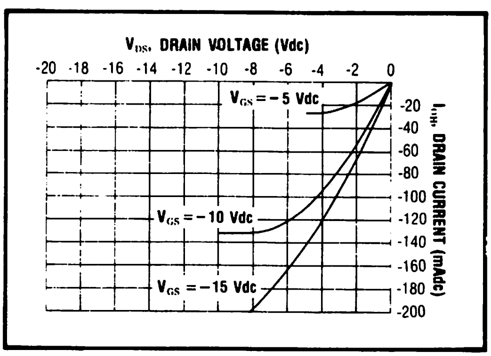
STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2] Min.	T_{LOW} [2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH} [2] Min.	T_{HIGH} [2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN} = V_{SS}$ or V_{DD}	–	1.0	–	0.005	1.0	–	30	µAdc
		10	All valid input	–	2.0	–	0.01	2.0	–	60	
		15	combinations	–	4.0	–	0.02	4.0	–	120	
OUTPUT HIGH (SOURCE) CURRENT	I_{OH}	5	V_{OH} = 4.6V	-2.5	–	-2.0	-4.5	–	-1.4	–	mAdc
		10	V_{OH} = 9.5V	-7.3	–	-5.8	-14.0	–	-4.0	–	
		15	V_{OH} = 13.5V	-23.1	–	-18.5	-45	–	-13.0	–	
			$V_{IN} = V_{SS}$								
OUTPUT LOW (SINK) CURRENT	I_{OL}	5	V_{OL} = 0.4V	2.4	–	2.4	4.5	–	1.7	–	mAdc
		10	V_{OL} = 0.5V	7.0	–	7.0	14.0	–	4.9	–	
		15	V_{OL} = 1.5V	22.2	–	27	45	–	19	–	
			$V_{IN} = V_{DD}$								

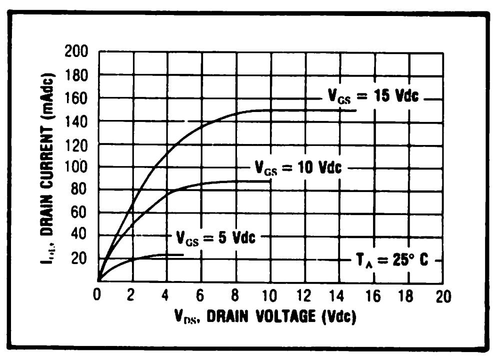
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}	5	–	90	180	ns
		10	–	45	90	
		15	–	35	70	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	90	180	ns
		10	–	45	90	
		15	–	35	70	



Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

SOLID STATE SCIENTIFIC

SCL4445B

CMOS 21-STAGE DIVIDER

FEATURES

- **Low Duty Cycle Push-Pull Outputs**
- **Inverter on Chip for Crystal Oscillator Circuit**
- **Buffered Output Available for Trimming Oscillator**
- **21 Fully Static Stages**
- **10MHz Counting Rate @ 10Vdc**

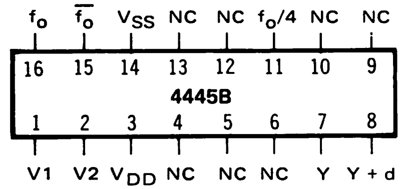
DESCRIPTION

The 4445B monolithic aluminum gate CMOS integrated circuit consists of an oscillator inverter, 21 toggle flip-flops, and two flip-flops used to produce a 3.125% duty cycle output wave-form. Push-pull operation is provided by the inverter output buffers. A divide-by-4 frequency output is provided as an oscillator monitor or subsidiary high frequency output.

The 4445B is especially suited for low-power timekeeping applications such as desk or wall clocks, automobile clocks, and digital timing references. Its output is suitable for driving miniature synchronous motors, stepping motors, or external bipolar transistors in push-push fashion.

The 4445B is pin compatible with device type CD4045A. The extra function $f_o/4$ is provided on pin 11.

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

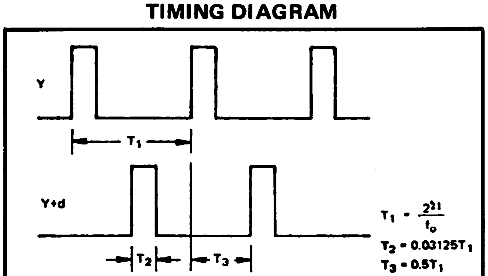
C	16-pin Cerdip
D	16-pin Ceramic
E	16-pin Epoxy
F	16-pin Flat
H	Chip

RECOMMENDED OPERATING CONDITIONS

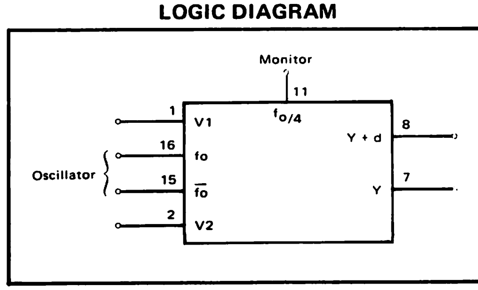
For maximum reliability:

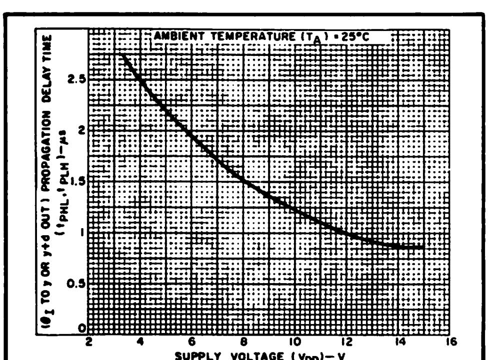
DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

TIMING DIAGRAM

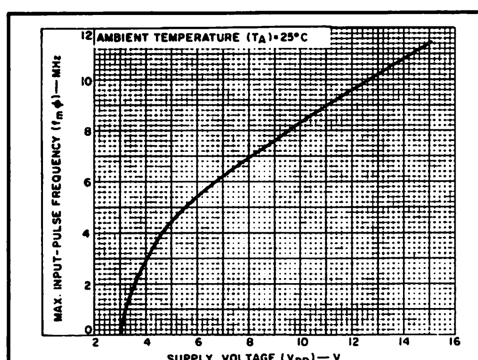


LOGIC DIAGRAM





Typical propagation delay (f_o to y or y + d out) vs. V_{DD}. (C_L = 50pF).



Typical f_o vs. V_{DD} (C_L = 50pF).

ELECTRICAL CHARACTERISTICS

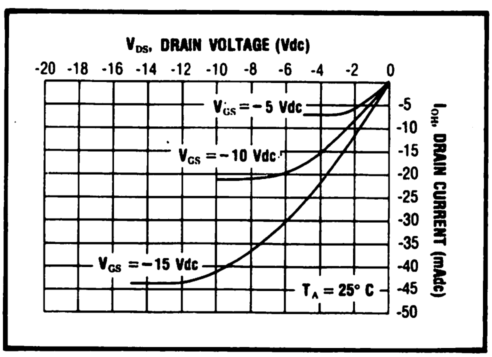
STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2]		+25°C			T_{HIGH} [2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN} = V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	μAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		15	combinations	–	20	–	0.2	20	–	600	

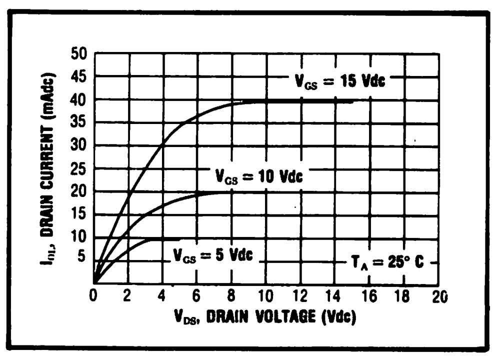
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
MAXIMUM CLOCK FREQUENCY	f_{CL}	5	3	6	–	MHz
		10	5	10	–	
		15	6	12	–	
MAXIMUM CLOCK RISE AND FALL TIME	t_{rCL}, t_{fCL}	5	15	–	–	μs
		10	15	–	–	
		15	5	–	–	

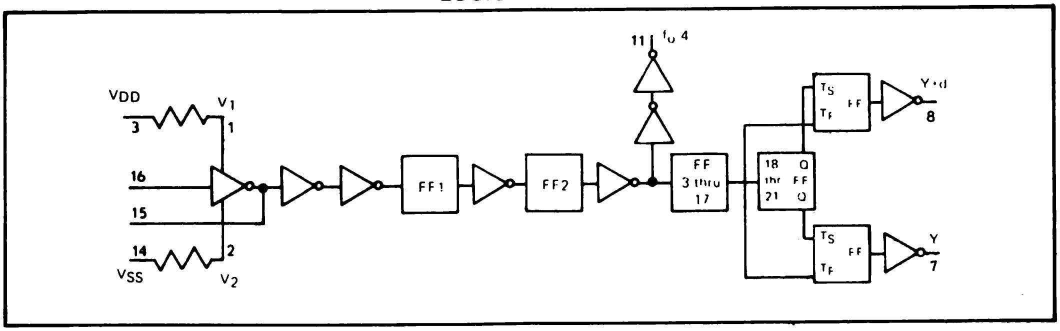


Typical P-Channel
Source Current Characteristics

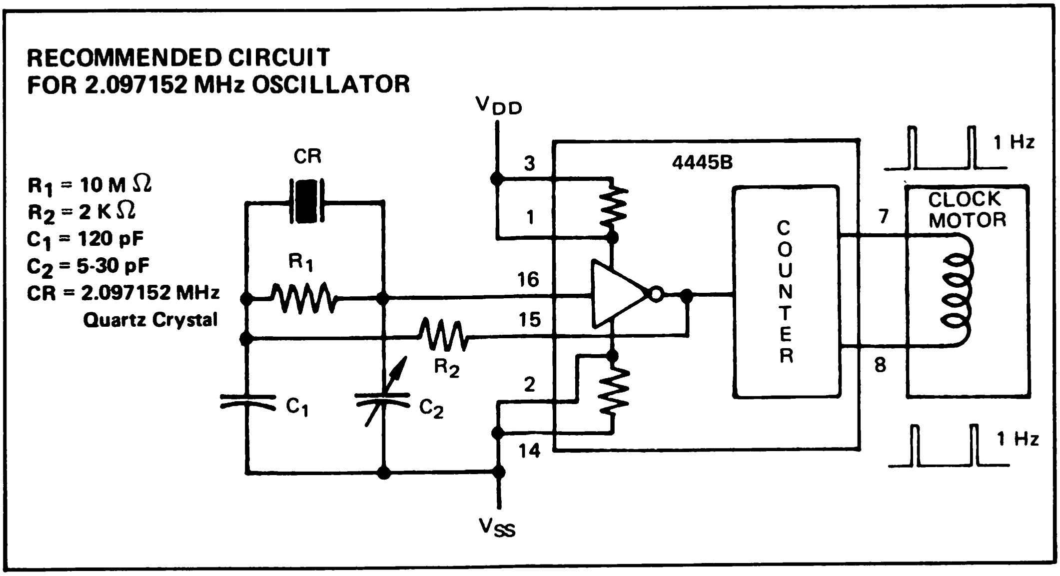


Typical N-Channel
Sink Current Characteristics

LOGIC DIAGRAM



APPLICATIONS INFORMATION



Typical clock motor driver

CMOS HEX INVERTER

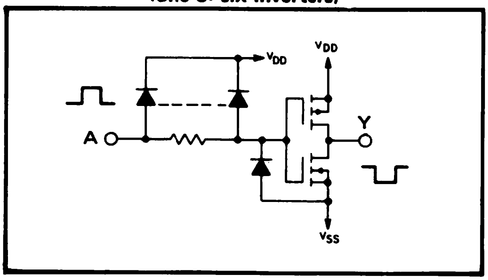
FEATURES

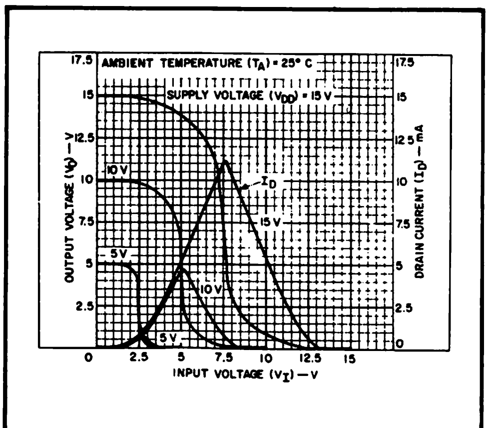
- All Inputs Fully Diode-Protected
- Pin Compatible with 4009B, 4049B
- Fully "B"-Series Compatible

DESCRIPTION

The 4449UB consists of six CMOS inverter circuits. It is pin-compatible with the 4009UB, 4049UB, and equivalent device types. In systems which do not require the high output current and level-shifting capabilities of the buffers, the less expensive 4449 can be substituted directly with no change in board layout. The device is particularly useful for quasi-linear circuits, such as oscillators and multivibrators.

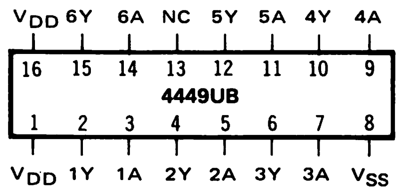
SCHEMATIC DIAGRAM
(one of six inverters)





Typical current and voltage transfer characteristics.

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

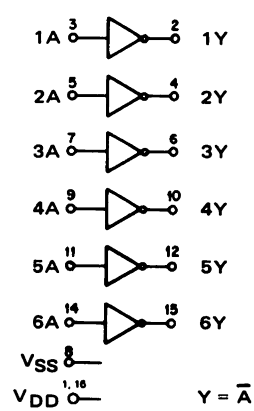
C	16-pin Cerdip
D	16-pin Ceramic
E	16-pin Epoxy
F	16-pin Flat
H	Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

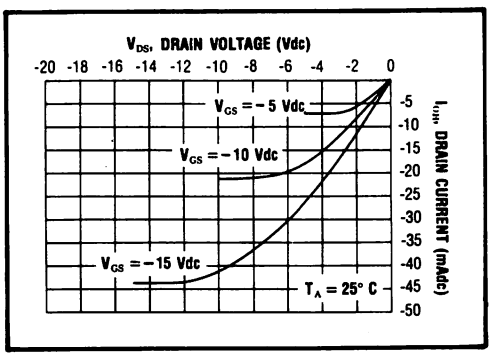
STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2] Min.	T_{LOW} [2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH} [2] Min.	T_{HIGH} [2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5 10 15	V_{IN} = V_{SS} or V_{DD} All valid input combinations	– – –	0.05 0.10 0.20	– – –	0.0005 0.001 0.002	0.05 0.10 0.20	– – –	1.5 3.0 6.0	µAdc

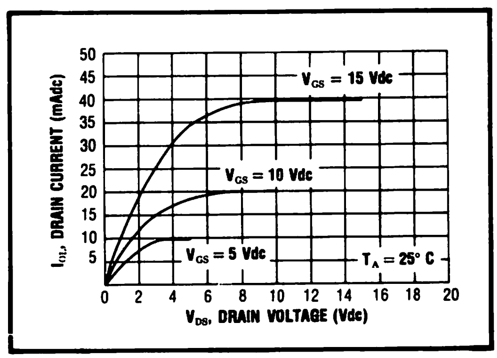
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}	5 10 15	– – –	60 30 25	120 60 50	ns
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5 10 15	– – –	100 50 40	200 100 80	ns

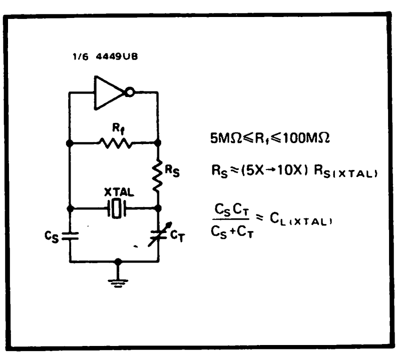


Typical P-Channel
Source Current Characteristics

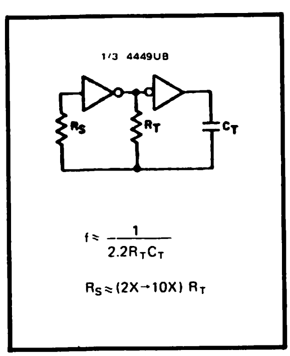


Typical N-Channel
Sink Current Characteristics

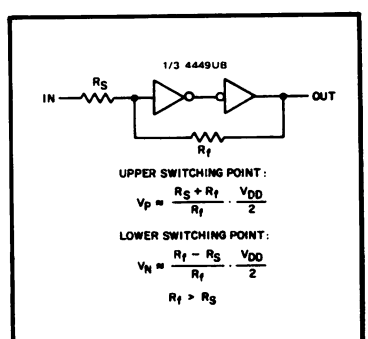
APPLICATIONS INFORMATION



Typical crystal oscillator circuit



Typical RC oscillator circuit



Input pulse shaping circuit (Schmitt trigger)

CMOS STROBED HEX INVERTER/BUFFER

FEATURES

- 3-State Outputs with Separate Disable Control
- Common Input Inhibit Line
- TTL Output Drive Guaranteed Over Temperature Range
- Output Impedance < 200 Ω @ 5Vdc Guaranteed Over Temperature Range

DESCRIPTION

The 4502B is a Strobed Hex Inverter/Buffer with a common Data Input Inhibit Control and a common Output Disable Control. The 3-state output allows common bus configurations.

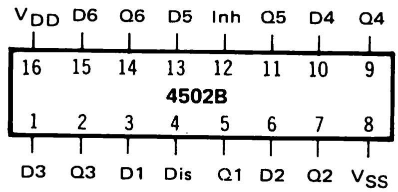
TRUTH TABLE

D_n	Inhibit	Disable	Q_n
0	0	0	1
1	0	0	0
X	1	0	0
X	X	1	High Impedance

X = Don't Care

CONNECTION DIAGRAM

(all packages)



Add suffix for package:

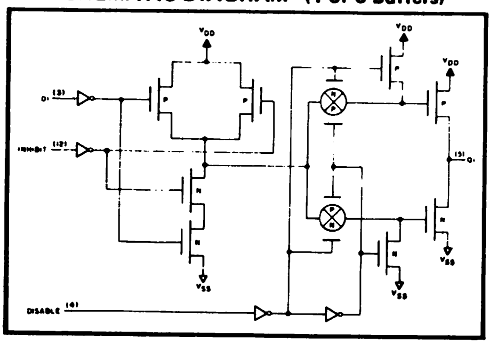
C	16-pin Cerdip	F	16-pin Flat
D	16-pin Ceramic	H	Chip
E	16-pin Epoxy		

RECOMMENDED OPERATING CONDITIONS

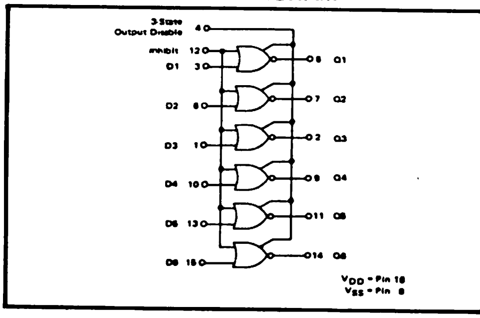
For maximum reliability:

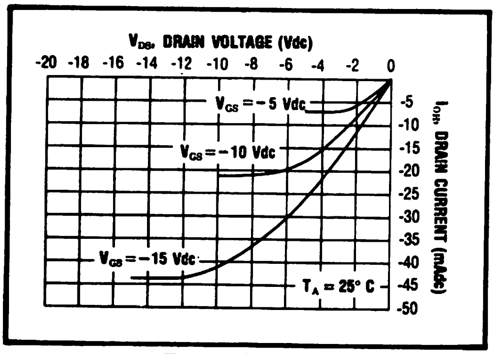
DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

SCHEMATIC DIAGRAM (1 of 6 buffers)

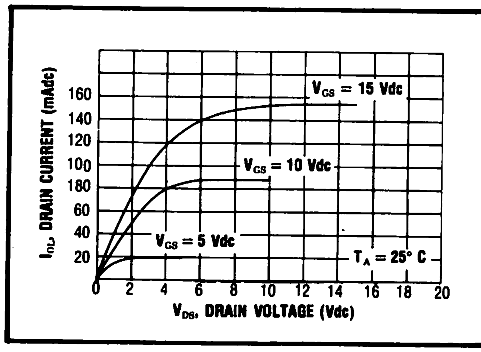


LOGIC DIAGRAM





Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2] Min.	T_{LOW} [2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH} [2] Min.	T_{HIGH} [2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5 10 15	$V_{IN} = V_{SS}$ or V_{DD} All valid input combinations	– – –	1.0 2.0 4.0	– – –	0.005 0.01 0.02	1.0 2.0 4.0	– – –	30 60 120	μAdc
OUTPUT LOW (SINK) CURRENT	I_{OL}	5 10 15	V_{OL} = 0.4V V_{OL} = 0.5V V_{OL} = 1.5V $V_{IN} = V_{SS}$ or V_{DD}	3.5 7.8 29	– – –	2.8 6.3 24.0	5.7 12.5 49	– – –	2.0 4.4 16	– – –	mAdc
3-STATE OUTPUT LEAKAGE CURRENT	I_{ZL}	15		–	±0.1	–	$\pm10^{-4}$	±0.1	–	±1.0	μAdc

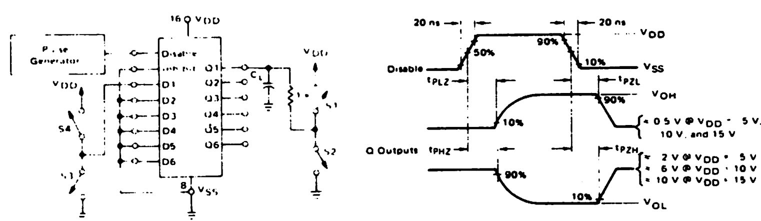
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME From Data Inputs	t_{PLH}	5 10 15	– – –	125 60 45	250 120 90	ns
	t_{PHL}	5 10 15	– – –	100 50 40	200 100 80	ns
From Disable	t_{PHZ}, t_{PLZ} t_{PZH}, t_{PZL}	5 10 15	– – –	65 30 25	130 60 50	ns
OUTPUT TRANSITION TIME	t_{TLH}	5 10 15	– – –	100 50 40	200 100 80	ns
	t_{THL}	5 10 15	– – –	60 30 20	120 60 40	ns

Switch Positions for 3 State Test

TEST	S1	S2	S3	S4
t_{PHZ}	Open	Closed	Closed	Open
t_{PLZ}	Closed	Open	Open	Closed
t_{PZL}	Closed	Open	Open	Closed
t_{PZH}	Open	Closed	Closed	Open



3-State AC Test Circuit and Waveforms (t_{PHZ}, t_{PZH}, t_{PLZ}, t_{PZL})

PRELIMINARY

HEX NON-INVERTING LEVEL SHIFTER

FEATURES

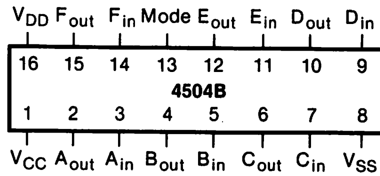
- **Up and down level-shifting capability**
- **Input Threshold Can Be Shifted for TTL Compatibility**
- **3 to 18 Vdc Operation for V_{DD} and V_{CC}**
- **Diode Protected Inputs to V_{SS}**

DESCRIPTION

The 4504B is a non-inverting hex level shifter that is designed to shift a TTL signal to CMOS logic levels for any CMOS supply voltage between 5 and 15 volts. The control input allows interface from CMOS to CMOS at one logic level to another logic level.

The V_{DD} level selects the output voltage levels and the V_{CC} level sets the input signal levels.

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

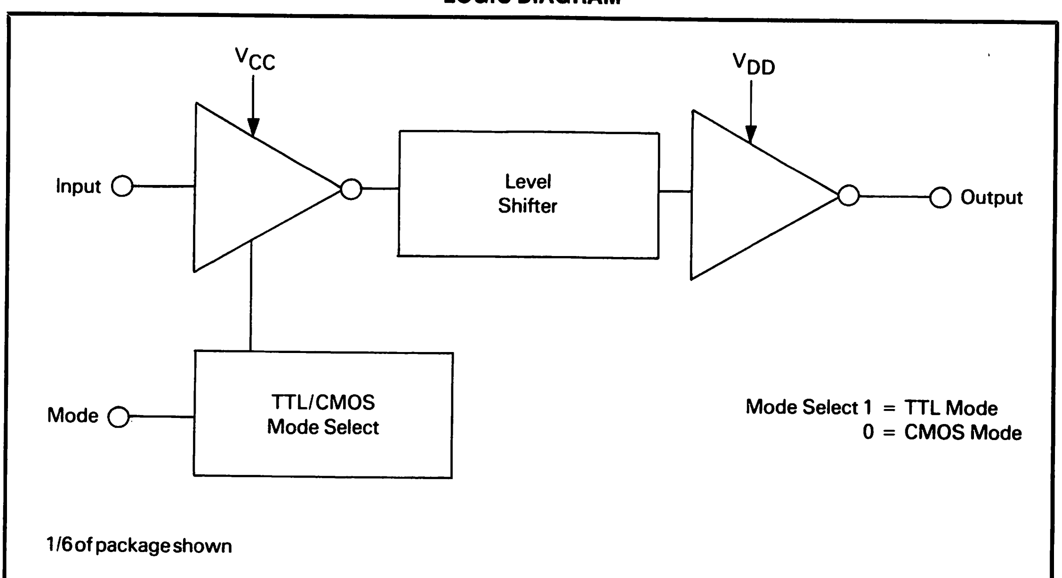
C 16-pin Cerdip
D 16-pin Ceramic
E 16-pin Epoxy
F 16-pin Flat
H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD}-V_{SS}$	3 to 15 V_{dc}
Operating Temperature	T_A	
C, D, F, H Device		−55 to +125 °C
E Device		−40 to +85 °C

LOGIC DIAGRAM



STATIC CHARACTERISTICS

PARAMETER		CONDITIONS	V_{SS} (Vdc)	V_{DD} (Vdc)	T_{LOW}[2] Min.	T_{LOW}[2] Max.	25°C Min.	25°C Typ.	25°C Max.	T_{HIGH}[2] Min.	T_{HIGH}[2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	$V_{IN} = V_{SS}$ or V_{DD} All valid input combinations	0 0 0	5 10 15	– – –	0.05 0.1 0.2	– – –	0.0005 0.001 0.002	0.05 0.1 0.2	– – –	1.5 3.0 6.0	μAdc

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications"
[2] T_{LOW} = −55°C for C, D, F, H device.
= −40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

CHARACTERISTIC	SYMBOL	SHIFTING MODE	V_{CC} Vdc	V_{DD} Vdc	Limits Min.	Limits Typ.	Limits Max.	Units
PROPAGATION DELAY, HIGH TO LOW	t_{PHL}	TTL – CMOS $V_{DD} > V_{CC}$	5.0 5.0	10 15	– –	120 120	– –	ns
		CMOS – CMOS $V_{DD} > V_{CC}$	5.0 5.0 10	10 15 15	– – –	100 120 50	– – –	
		CMOS – CMOS $V_{CC} > V_{DD}$	10 15 15	5.0 5.0 10	– – –	160 160 160	– – –	
PROPAGATION DELAY, LOW TO HIGH	t_{PHL}	TTL – CMOS $V_{DD} > V_{CC}$	5.0 5.0	10 15	– –	200 160	– –	ns
		CMOS – CMOS $V_{DD} > V_{CC}$	5.0 5.0 10	10 15 15	– – –	100 120 50	– – –	
		CMOS – CMOS $V_{CC} > V_{DD}$	10 15 15	5.0 5.0 10	– – –	160 160 65	– – –	
OUTPUT RISE AND FALL TIME	t_{TLH}, t_{THL}	ALL	– – –	5.0 10 15	– – –	100 50 40	– – –	ns

SOLID STATE SCIENTIFIC

CMOS DUAL 4-BIT LATCH

FEATURES

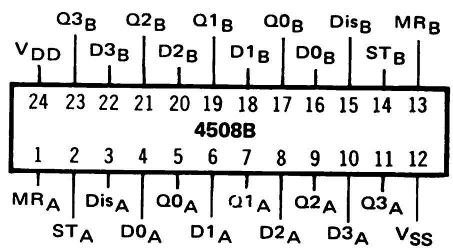
- Two Independent Four-Bit Latches
- 3-State Outputs
- Direct Reset
- All Inputs Buffered

DESCRIPTION

The 4508B consists of two identical independent 4-Bit Latches with separate Strobe (ST) and Master Reset (MR) controls. Separate Disable inputs force the outputs to a high-impedance state for bus line applications.

These devices find primary use in buffer storage, holding register, and display circuits, and other general digital logic applications.

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

D 24-pin Ceramic
E 24-pin Plastic
H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

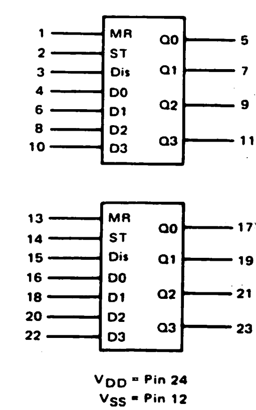
DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
D, H Device		-55 to +125	°C
E Device		-40 to +85	°C

TRUTH TABLE

MR	ST	Disable	D3	D2	D1	D0	Q3	Q2	Q1	Q0
0	1	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	1	0	0	0	1
0	1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0	0
0	1	0	1	0	0	0	1	0	0	0
0	0	0	X	X	X	X	Latched			
1	X	0	X	X	X	X	0	0	0	0
X	X	1	X	X	X	X	High Impedance			

X = Don't Care

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

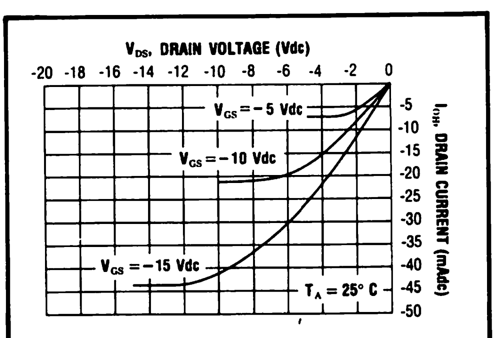
STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2] Min.	T_{LOW} [2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH} [2] Min.	T_{HIGH} [2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5 10 15	$V_{IN} = V_{SS}$ or V_{DD} All valid input combinations	– – –	5 10 20	– – –	0.05 0.1 0.2	5 10 20	– – –	150 300 600	μAdc
3-STATE OUTPUT LEAKAGE CURRENT	I_{ZL}	15		–	±0.1	–	$\pm 10^{-4}$	±0.1	–	±1.0	μAdc

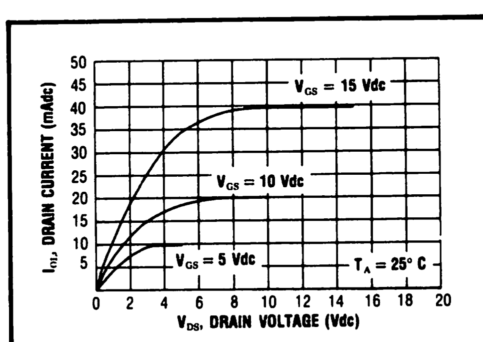
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for D, H device.
= -40°C for E device.
T_{HIGH} = +125°C for D, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME From Data Inputs	t_{PLH}, t_{PHL}	5 10 15	– – –	220 90 60	440 180 120	ns
From Disable Input	t_{PHZ}, t_{PLZ} t_{PZH}, t_{PZL}	5 10 15	– – –	85 45 30	170 90 60	ns
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5 10 15	– – –	100 50 40	200 100 80	ns
MINIMUM MASTER RESET PULSE WIDTH	PW_{MR}	5 10 15	– – –	100 50 35	200 100 70	ns
MINIMUM STROBE PULSE WIDTH	PW_{ST}	5 10 15	– – –	70 35 20	140 70 40	ns
MINIMUM SETUP TIME Data Inputs	t_{setup}	5 10 15	– – –	25 10 5	50 20 10	ns
MINIMUM HOLD TIME Data Inputs	t_{hold}	5 10 15	– – –	0 0 0	0 0 0	ns

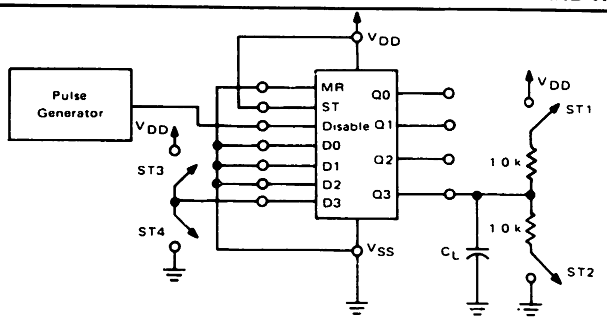


Typical P-Channel
Source Current Characteristics

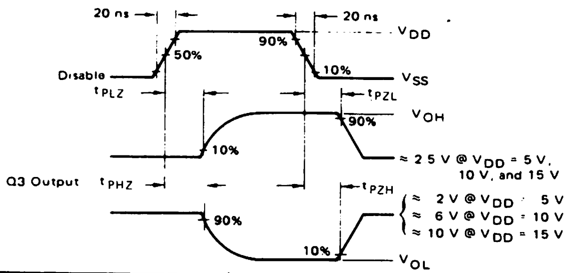


Typical N-Channel
Sink Current Characteristics

3-STATE AC TEST CIRCUIT AND WAVEFORMS

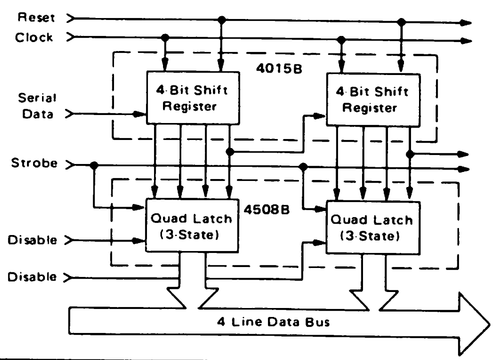


TEST	ST1	ST2	ST3	ST4
t_{PHZ}	OPEN	CLOSE	CLOSE	OPEN
t_{PLZ}	CLOSE	OPEN	OPEN	CLOSE
t_{PZL}	CLOSE	OPEN	OPEN	CLOSE
t_{PZH}	OPEN	CLOSE	CLOSE	OPEN

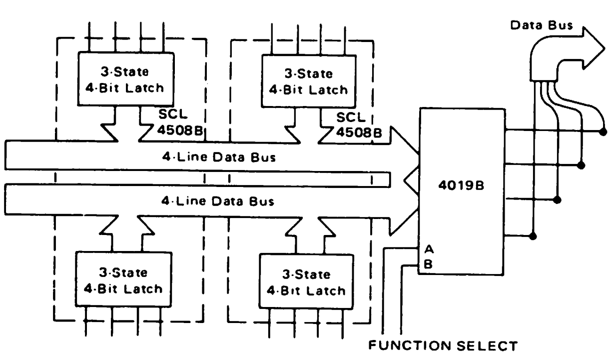


APPLICATIONS INFORMATION

BUS REGISTER



DUAL MULTIPLEXED BUS REGISTER WITH FUNCTION SELECT



FUNCTION SELECT

A	B	Function
0	0	Inhibit (all 0)
1	0	Select A Bus
0	1	Select B Bus
1	1	$A_i + B_i$

SOLID STATE SCIENTIFIC

CMOS BCD UP/DOWN COUNTER

FEATURES

- Internally Synchronous for High Speed
- Asynchronous Preset Enable
- Asynchronous Reset
- Logic Edge-Clocked Design
- 6MHz Counting Rate @ 10Vdc
- Carry Output for Cascading Stages

DESCRIPTION

The 4510B consists of a four-stage Up/Down Counter with provisions for "look-ahead" carry in both counting modes. The inputs consist of a single Clock, Carry-in (Clock Enable), Reset, Up/Down, Preset Enable, and four individual Jam signals. Four separate buffered Q signals and a Carry out signal are provided as outputs.

A high Preset Enable signal allows information on the Jam inputs to preset the counter to any state asynchronously with the Clock. A high on the Reset line resets all stages to the "zero" state. The counter is advanced one count at the positive transition of the Clock when the Carry-in and Preset Enable signals are low. Advancement is inhibited when the Carry-in or Preset Enable signals are high. The Carry-out signal is normally high and goes low when the counter reaches its maximum count in the Up mode or the minimum count in the Down mode, provided the Carry-in signal is low. The Carry-in signal in the low state can thus be considered a "Clock Enable." The Carry-in terminal must be connected to V_{SS} when not in use.

The counter counts Up when the Up/Down input is high, and Down when the Up/Down input is low. Multiple packages can be connected in either a parallel-clocking or a ripple-clocking arrangement. Parallel clocking provides synchronous control and hence faster response from all counting outputs. Ripple-clocking allows for longer clock input rise and fall times.

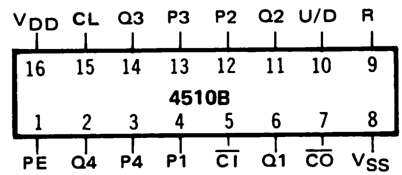
This counter finds primary use in up/down and differential counting and frequency synthesizer applications. It is also useful in A/D and D/A conversion and for magnitude and sign generation.

TRUTH TABLE

$\overline{\text{CARRY IN}}$	UP/DOWN	PRESET ENABLE	RESET	ACTION
1	X	0	0	No Count
0	1	0	0	Count Up
0	0	0	0	Count Down
X	X	1	0	Preset
X	X	X	1	Reset

X = Don't Care

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

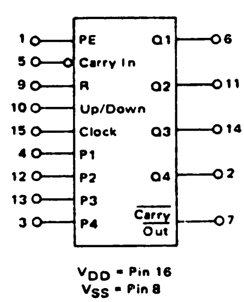
C	16-pin Cerdip
D	16-pin Ceramic
E	16-pin Epoxy
F	16-pin Flat
H	Chip

RECOMMENDED OPERATING CONDITIONS

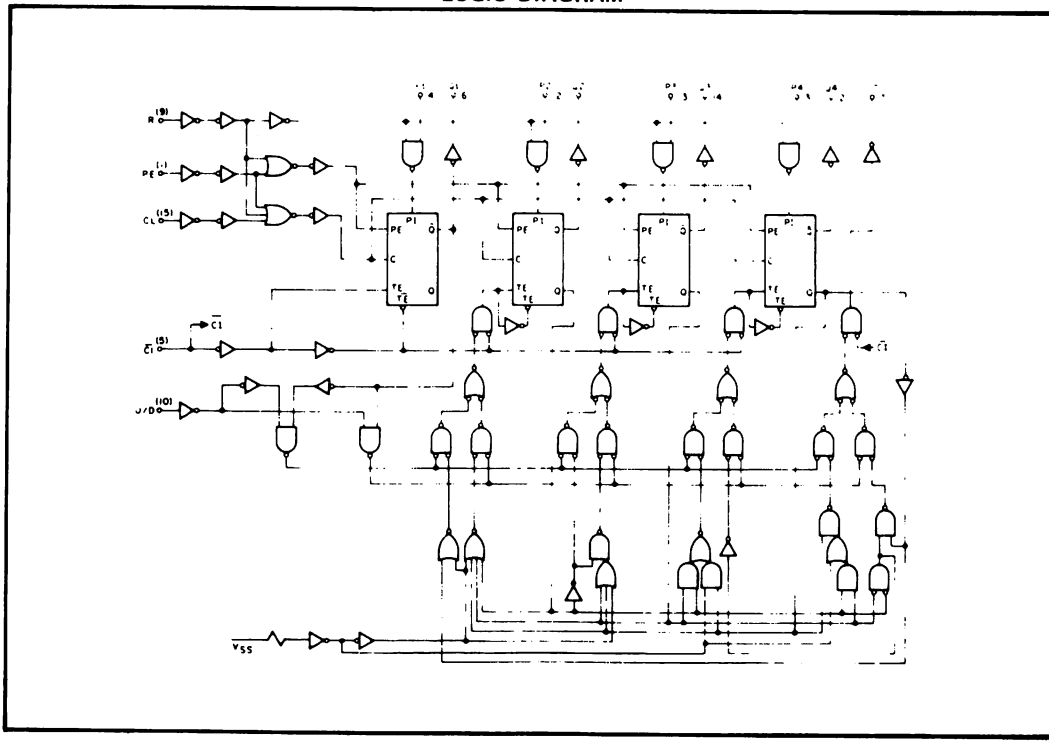
For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

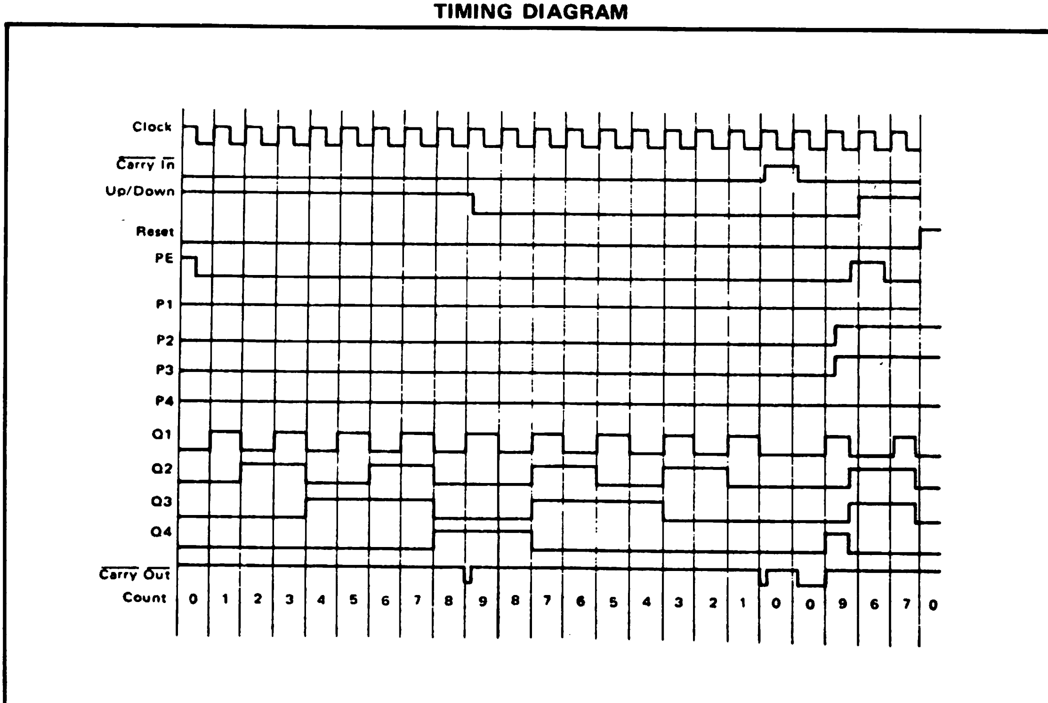
BLOCK DIAGRAM



LOGIC DIAGRAM



TIMING DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS[1]

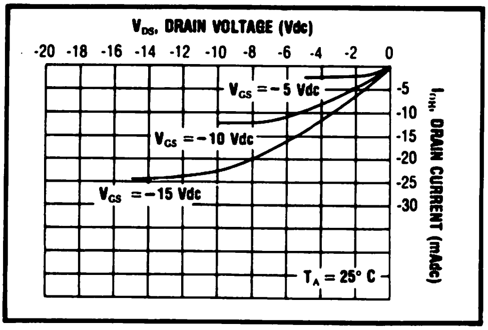
PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[2] Min.	T_{LOW}[2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH}[2] Min.	T_{HIGH}[2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5 10 15	$V_{IN}=V_{SS}$ or V_{DD} All valid input combinations	– – –	5 10 20	– – –	0.05 0.1 0.2	5 10 20	– – –	150 300 600	μAdc

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

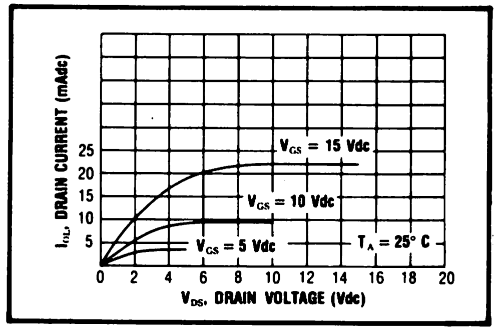
DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME Clock to Q	t_{PLH}, t_{PHL}	5 10 15	– – –	200 100 75	400 200 150	ns
Clock to $\overline{\text{Carry Out}}$		5 10 15	– – –	210 120 90	420 240 180	ns
$\overline{\text{Carry In}}$ to $\overline{\text{Carry Out}}$		5 10 15	– – –	125 60 50	250 120 100	ns
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5 10 15	– – –	100 50 40	200 100 80	ns
MINIMUM CLOCK PULSE WIDTH	PW_{CL}	5 10 15	– – –	170 85 70	340 170 140	ns
MAXIMUM CLOCK FREQUENCY	f_{CL}	5 10 15	2.0 4.0 5.5	4.0 8.0 11.0	– – –	MHz
MAXIMUM CLOCK RISE AND FALL TIME[1]	t_{rCL}, t_{fCL}	5 10 15	15 15 15	– – –	– – –	μs
MINIMUM SETUP TIME $\overline{\text{Carry In}}$	t_{setup}	5 10 15	– – –	130 65 50	260 130 100	ns
Up/Down		5 10 15	– – –	250 100 75	500 200 150	ns
PRESET OR RESET OPERATION						
PROPAGATION DELAY TIME Preset Enable or Reset to Q	t_{PLH}, t_{PHL}	5 10 15	– – –	210 105 90	420 210 180	ns
Preset Enable or Reset to $\overline{\text{Carry Out}}$		5 10 15	– – –	320 160 25	640 320 250	ns
MINIMUM PRESET ENABLE OR RESET PULSE WIDTH	PW_{PE}, PW_R	5 10 15	– – –	100 50 40	200 100 80	ns
PRESET ENABLE OR RESET REMOVAL TIME	t_{rem}	5 10 15	– – –	325 110 90	650 220 180	ns

[1] When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.



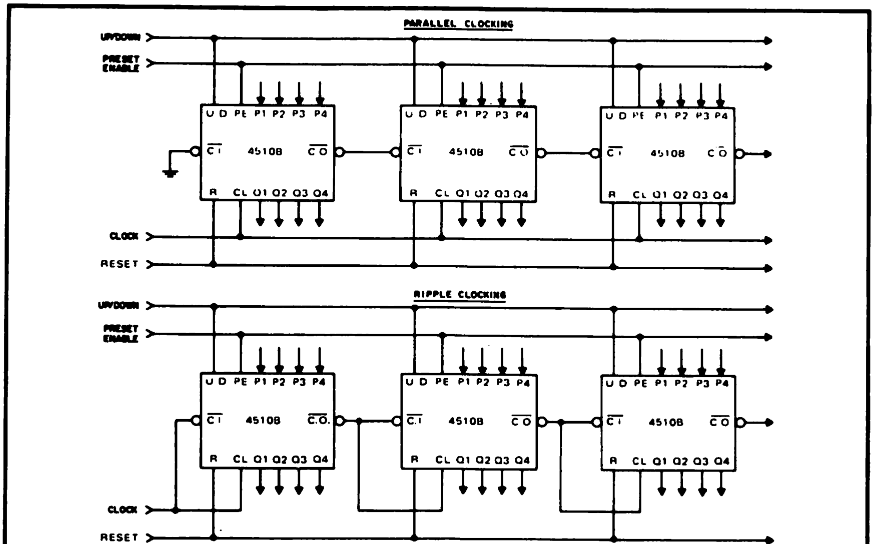
Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

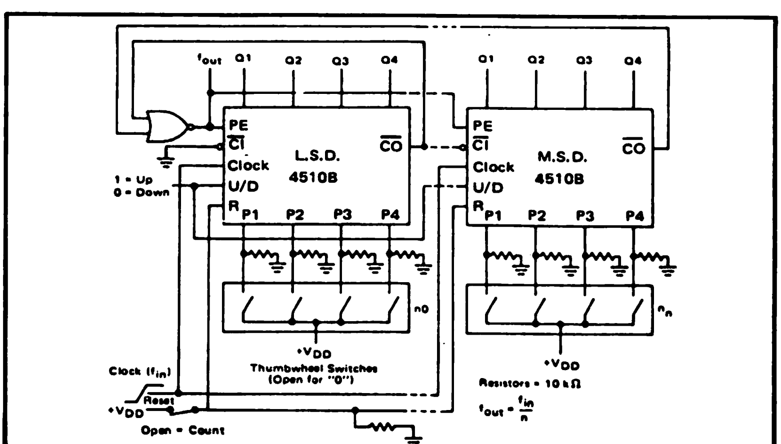
APPLICATIONS INFORMATION

CASCADING COUNTERS



The Up/Down control can be changed at any count. The only restriction on changing the Up/Down control is that the clock input to the first counting stage must be "high"

Cascading Counter Packages.



Programmable Cascaded Frequency Divider

SOLID STATE SCIENTIFIC

SCL4511B

CMOS BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER

FEATURES

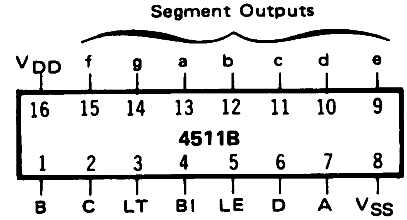
- High-Current Sourcing Bipolar Outputs (Up to 25 mA)
- Latched Storage of Input Code
- Blanking Input for Display Intensity Modulation
- Lamp Test Provision
- Readout Blanking for Illegal Input Combinations

DESCRIPTION

The 4511B provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and an output drive capability to source up to 25 mA of current. Lamp Test, Blanking, and Latch Enable inputs are used to test the display, turn off the display, and store a BCD code, respectively. It can be used with LED, incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

Applications include counter display drivers, seven-segment decimal display, and various clock, watch, and timer uses.

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

C	16-pin Cerdip
D	16-pin Ceramic
E	16-pin Epoxy
F	16-pin Flat
H	Chip

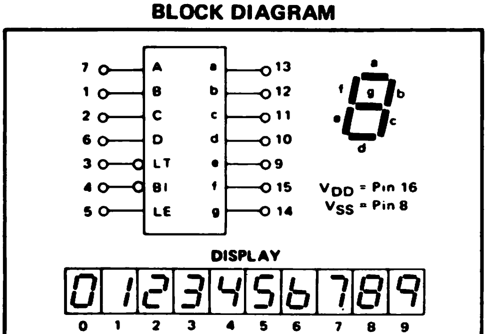
TRUTH TABLE

LE	BI	LT	D	C	B	A	a	b	c	d	e	f	g	DISPLAY
X	X	0	X	X	X	X	1	1	1	1	1	1	1	8
X	0	1	X	X	X	X	0	0	0	0	0	0	0	Blank
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	0	1	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	1	0	0	0	0	0	0	0	Blank
1	1	1	X	X	X	X	*							*

X = Don't care

* Depends upon the BCD code applied during the 0 to 1 transition of LE.

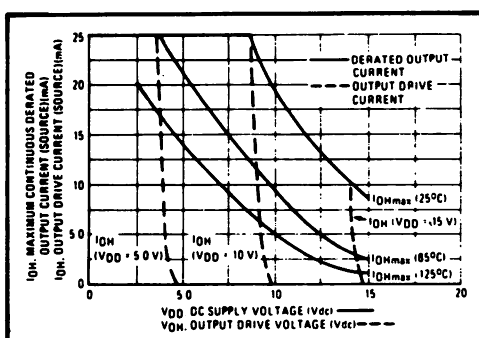
BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C



Typical P-Channel Source Current Characteristics

The maximum continuous (worst case) derated output drive current applies to a single output with all other outputs sourcing an equal amount of current. Operation above the derating curve at a given temperature is not recommended.

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS[1]

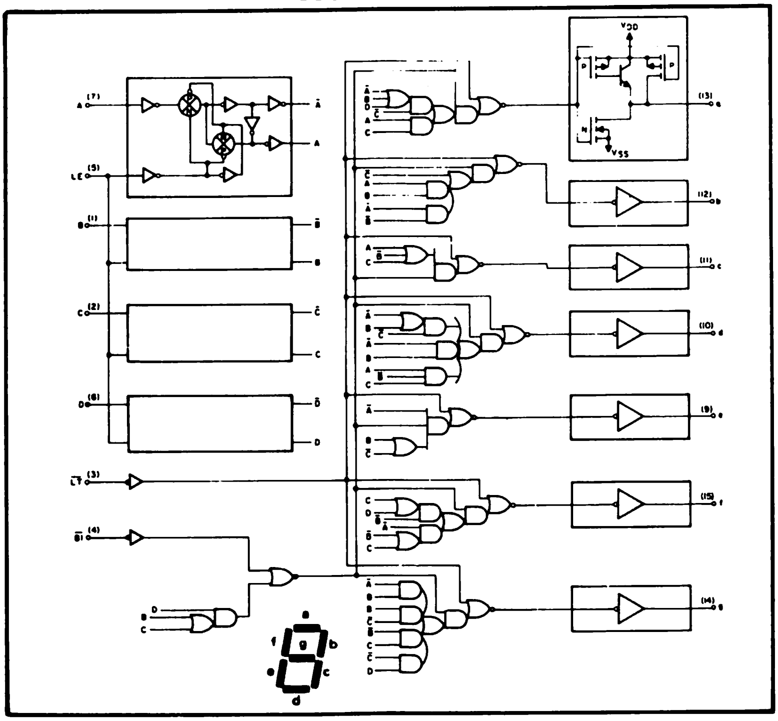
PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[2] Min.	T_{LOW}[2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH}[2] Min.	T_{HIGH}[2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN} = V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	μAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		15	combinations	–	20	–	0.2	20	–	600	
OUTPUT DRIVE VOLTAGE	V_{OUT}	5	I_{OH} = 0 mAdc	4.99	–	4.99	5.0	–	4.95	–	Vdc
			– 5	–	–	–	4.25	–	–	–	
			– 10	–	–	3.9	4.13	–	–	–	
			– 15	–	–	–	3.95	–	–	–	
			– 20	–	–	3.4	3.75	–	–	–	
			– 25	–	–	–	3.5	–	–	–	
		10	I_{OH} = 0mAdc	9.99	–	9.99	10	–	9.95	–	Vdc
			– 5	–	–	–	9.25	–	–	–	
			–10	–	–	9.0	9.15	–	–	–	
			–15	–	–	–	9.03	–	–	–	
			–20	–	–	8.6	8.90	–	–	–	
			– 25	–	–	–	8.75	–	–	–	
		15	I_{OH} = 0mAdc	14.99	–	14.99	15	–	14.96	–	Vdc
			– 5	–	–	–	14.25	–	–	–	
			–10	–	–	14.0	14.18	–	–	–	
			–15	–	–	–	14.08	–	–	–	
			–20	–	–	13.6	13.95	–	–	–	
			–25	–	–	–	13.80	–	–	–	
OUTPUT LOW (SINK) CURRENT	I_{OL}	5	V_{OL} = 0.4V	1.9	–	1.5	3.4	–	1.1	–	mAdc
		10	V_{OL} = 0.5V	5.0	–	4.0	6.5	–	2.8	–	
		15	V_{OL} = 1.5V	13.8	–	11.0	24	–	7.7	–	
			$V_{IN} = V_{SS}$ or V_{DD}								

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

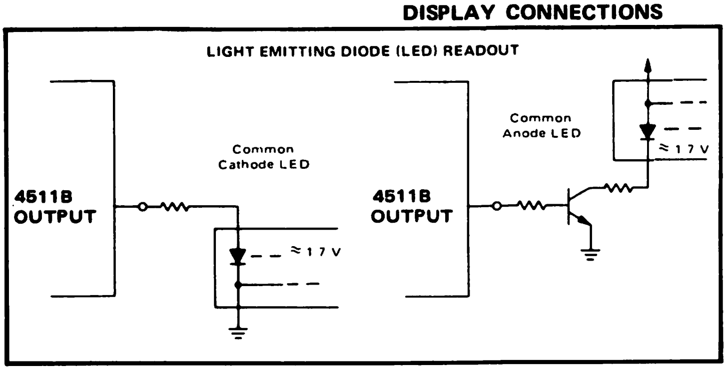
PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME From Data Inputs	t_{PLH}	5	–	520	1040	ns
		10	–	210	420	
		15	–	150	300	
	t_{PHL}	5	–	660	1320	ns
		10	–	260	520	
		15	–	180	360	
From Blanking Input	t_{PLH}	5	–	300	600	ns
		10	–	125	250	
		15	–	100	200	
	t_{PHL}	5	–	500	1000	ns
		10	–	200	400	
		15	–	160	320	
From Lamp Test Input	t_{PLH}	5	–	300	600	ns
		10	–	120	240	
		15	–	90	180	
	t_{PHL}	5	–	325	650	ns
		10	–	130	260	
		15	–	95	190	
OUTPUT TRANSITION TIME	t_{TLH}	5	–	170	250	ns
		10	–	120	200	
		15	–	100	180	
	t_{THL}	5	–	400	900	ns
		10	–	225	450	
		15	–	200	400	
MINIMUM DATA INPUT SETUP TIME	t_{setup}	5	–	90	180	ns
		10	–	40	80	
		15	–	20	40	
MINIMUM DATA INPUT HOLD TIME	t_{hold}	5	–	-90	0	ns
		10	–	-40	0	
		15	–	-20	0	
MINIMUM LATCH ENABLE PULSE WIDTH	PW_{LE}	5	–	260	520	ns
		10	–	110	220	
		15	–	65	130	

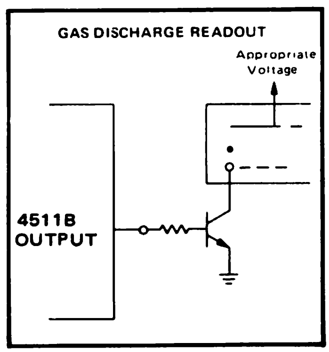
LOGIC DIAGRAM

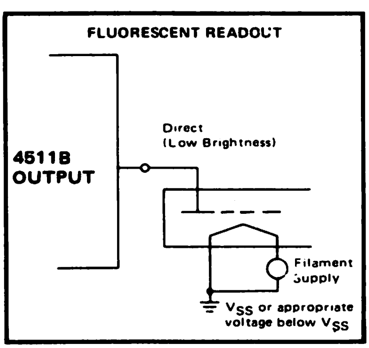


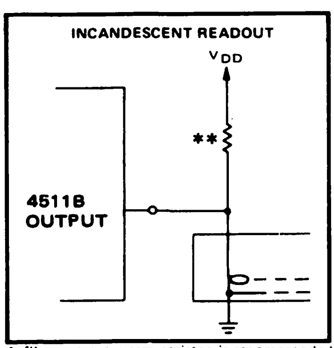
APPLICATIONS INFORMATION

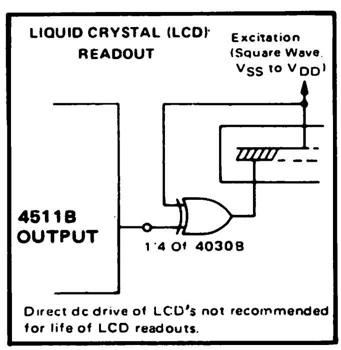
DISPLAY CONNECTIONS











**A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

CMOS 8-CHANNEL DATA SELECTOR

FEATURES

- 3-State Output with Disable Control
- Separate Inhibit Input
- Selects One of Eight Data Sources
- Performs Parallel-To-Serial Conversion

DESCRIPTION

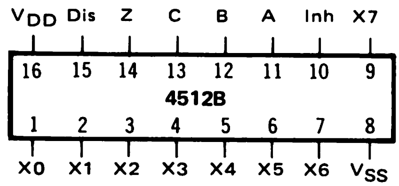
The 4512B is an 8-Channel Data Selector with Function Inhibit and Output Disable controls. One of eight binary inputs is selected by Select inputs A, B, and C, and is routed to the output Z. A high on the Disable input causes the Z output to assume a high-impedance state, regardless of other input conditions. This allows the output to interface directly with bus-oriented systems. When the Inhibit input is high, it forces the output low, providing the Disable input is low. By manipulation of the inputs, the 4512B can provide any logic functions of four variables (see Applications Information).

TRUTH TABLE

C	B	A	INHIBIT	DISABLE	Z
0	0	0	0	0	X0
0	0	1	0	0	X1
0	1	0	0	0	X2
0	1	1	0	0	X3
1	0	0	0	0	X4
1	0	1	0	0	X5
1	1	0	0	0	X6
1	1	1	0	0	X7
ϕ	ϕ	ϕ	1	0	0
ϕ	ϕ	ϕ	ϕ	1	High Impedance

ϕ = Don't Care

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

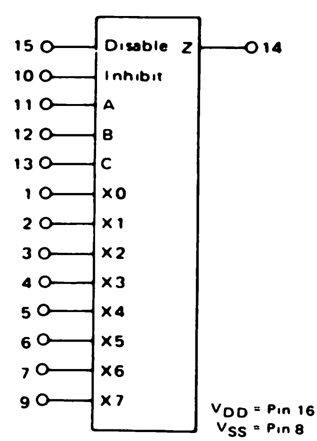
C	16-pin Cerdip
D	16-pin Ceramic
E	16-pin Epoxy
F	16-pin Flat
H	Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

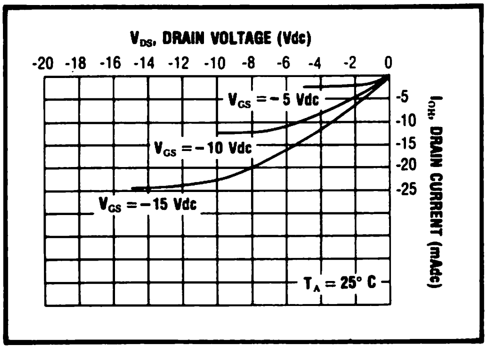
STATIC CHARACTERISTICS[1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[2]		+25°C			T_{HIGH}[2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5 10 15	$V_{IN} = V_{SS}$ or V_{DD} All valid input combinations	– – –	5 10 20	– – –	0.05 0.1 0.2	5 10 20	– – –	150 300 600	μAdc
3-STATE OUTPUT LEAKAGE CURRENT	I_{ZL}	15		–	±0.1	–	$\pm 10^{-4}$	±0.1	–	±1.0	μAdc

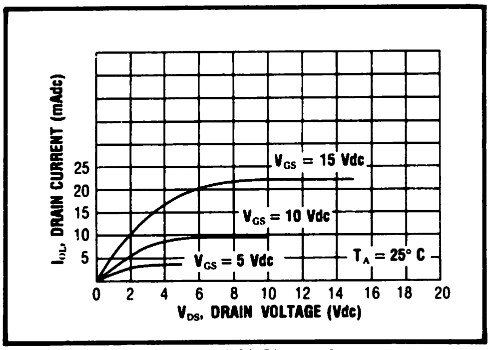
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME From Inhibit	t_{PLH}, t_{PHL}	5 10 15	– – –	120 55 40	240 110 80	ns
From Select Input	t_{PLH}, t_{PHL}	5 10 15	– – –	225 100 75	450 200 150	ns
From Data Input	t_{PLH}, t_{PHL}	5 10 15	– – –	200 80 60	400 160 120	ns
From Disable	t_{PHZ}, t_{PZH} t_{PLZ}, t_{PZL}	5 10 15	– – –	60 30 25	120 60 50	ns
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5 10 15	– – –	100 50 40	200 100 80	ns

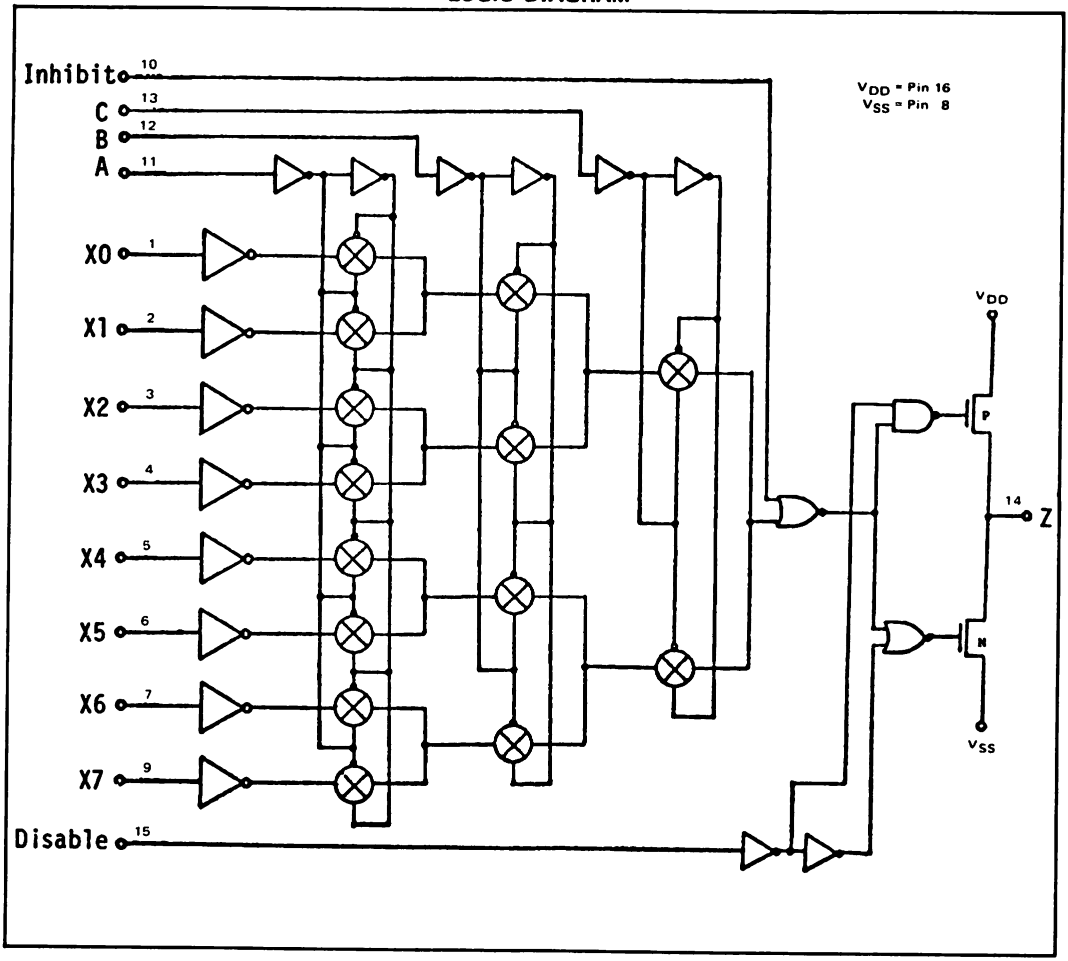


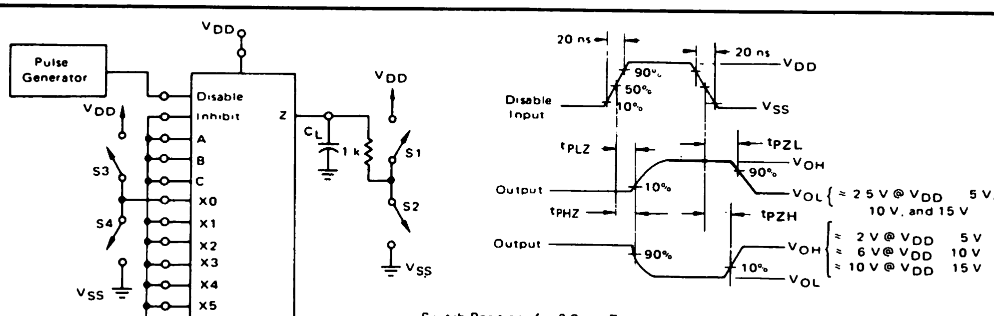
Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

LOGIC DIAGRAM





Switch Positions for 3-State Test

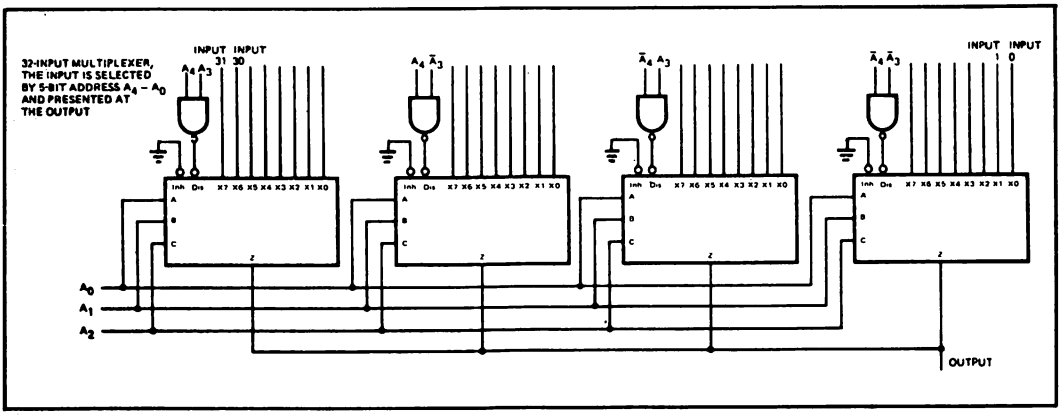
TEST	S1	S2	S3	S4
t_{PHZ}	Open	Closed	Closed	Open
t_{PLZ}	Closed	Open	Open	Closed
t_{PZL}	Closed	Open	Open	Closed
t_{PZH}	Open	Closed	Closed	Open

3-State AC Test Circuit and Waveform

APPLICATIONS INFORMATION

32-INPUT MULTIPLEXER

Output terminals of several 4512B devices can be connected to a single data bus. One 4512B is selected by the 3-state Disable control, and the remaining devices are disabled into a high-impedance state. A 32-input multiplexer utilizing four 4512B data selectors and a single 4011B is shown.



LOGIC FUNCTION GENERATORS

In addition to the standard application of multiplexers in data conversion techniques, these circuits can also be used in generating logic functions, which in many cases can reduce system package count.

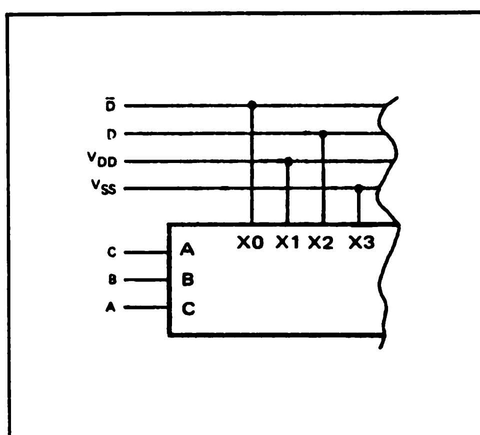
A multiplexer is a multiple-position single-pole switch. One set of inputs selects the position of the switch. The second set of inputs collects the input data, which is transferred through the circuit to one output. By using the binary select inputs and the data inputs, the 4512B can generate any of the 65,536 different functions of four variables.

Assume the four binary inputs are A, B, C, and D, and that Z is the desired function. Using the select inputs as the first three variables, any combination of A, B, and C will select a data input (assuming the output is enabled). For each combination of A, B, and C, the required output, as a function of the fourth variable D, can be HIGH or LOW or the same as D or the inverse of D. Therefore, the truth table may be examined and each data input of the 4512B is connected to V_{DD}, V_{SS}, D, or $\overline{D}$ as required. In such fashion, the function is generated.

In the example shown, the first two outputs are the inverse of D, so X0 is connected to $\overline{D}$. The next two are HIGH, so X1 is connected to V_{DD}, etc.

INPUT VARIABLES				REQUIRED FUNCTION
A	B	C	D	Z
L	L	L	L	H
L	L	L	H	L
L	L	H	L	H
L	L	H	H	H
L	H	L	L	L
L	H	L	H	H
L	H	H	L	L
L	H	H	H	L
H	L	L	L	L
.	.	.	.	.
.	.	.	.	.
		.	.	.

H = HIGH Level
L = LOW Level



CMOS 4-TO-16 LINE DECODERS WITH LATCH

FEATURES

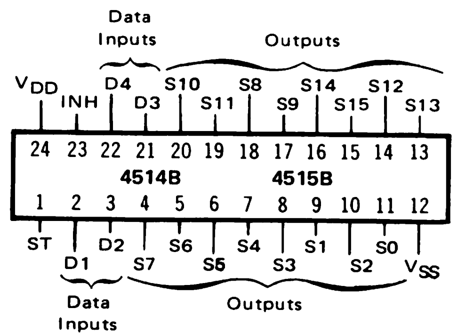
- Strobed Input Latch
- Inhibit Control
- Selected Output Active High (4514B) or Active Low (4515B)

DESCRIPTION

The 4514B and 4515B are two output options of a 4-to-16 Line Decoder with Latched Inputs. The 4514B presents a logic "1" at the selected output, and the 4515B presents a logic "0" at the selected output. The latches hold the last input data presented prior to the Strobe transition from "1" to "0". Inhibit allows all outputs to be placed at "0" (4514B), or "1" (4515B), regardless of the state of the Data or Strobe inputs.

Applications include code conversion, address decoding, memory selection control, demultiplexing, and readout decoding.

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

D 24-pin Ceramic
E 24-pin Epoxy
H Chip

TRUTH TABLE (Strobe = 1)

Inhibit	Data Inputs D	C	B	A	Selected Output 4514B = Logic "1" 4515B = Logic "0"
0	0	0	0	0	S0
0	0	0	0	1	S1
0	0	0	1	0	S2
0	0	0	1	1	S3
0	0	1	0	0	S4
0	0	1	0	1	S5
0	0	1	1	0	S6
0	0	1	1	1	S7
0	1	0	0	0	S8
0	1	0	0	1	S9
0	1	0	1	0	S10
0	1	0	1	1	S11
0	1	1	0	0	S12
0	1	1	0	1	S13
0	1	1	1	0	S14
0	1	1	1	1	S15
1	X	X	X	X	All Outputs = "0", 4514B All Outputs = "1", 4515B

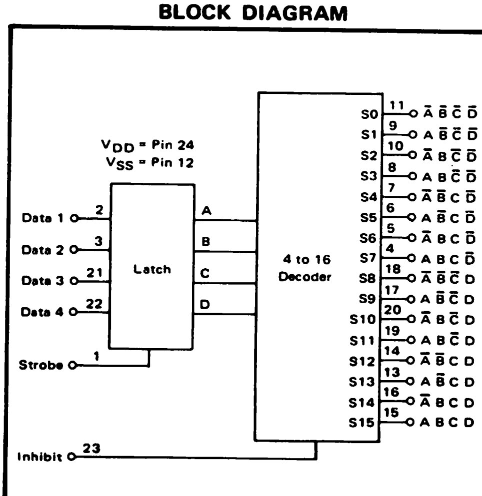
X = Don't Care

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
D, H Device		-55 to +125	°C
E Device		-40 to +85	°C

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

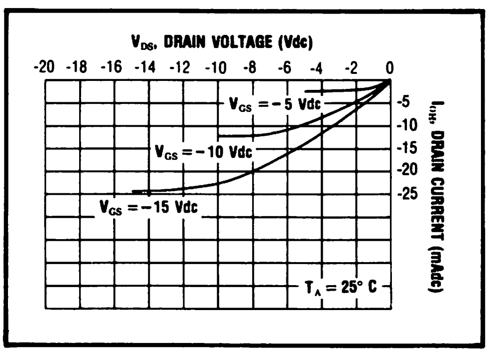
STATIC CHARACTERISTICS[1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[2] Min.	T_{LOW}[2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH}[2] Min.	T_{HIGH}[2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN} = V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	μAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		15	combinations	–	20	–	0.2	20	–	600	

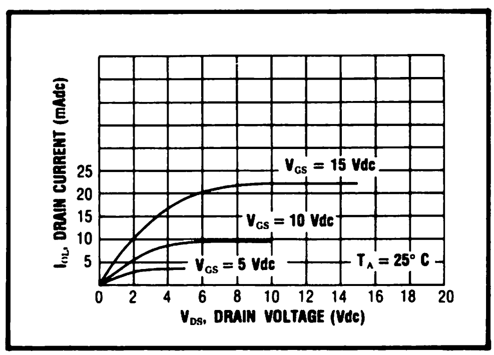
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = −55°C for C, D, F, H device.
= −40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME From Data Inputs	t_{PLH}, t_{PHL}	5	–	485	970	ns
		10	–	185	370	
		15	–	135	270	
From Inhibit Input		5	–	250	500	ns
		10	–	110	220	
		15	–	85	170	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
MINIMUM DATA INPUT SETUP TIME	t_{setup}	5	–	75	150	ns
		10	–	35	70	
		15	–	20	40	
MINIMUM STROBE PULSE WIDTH	PW_{ST}	5	–	125	250	ns
		10	–	50	100	
		15	–	40	75	

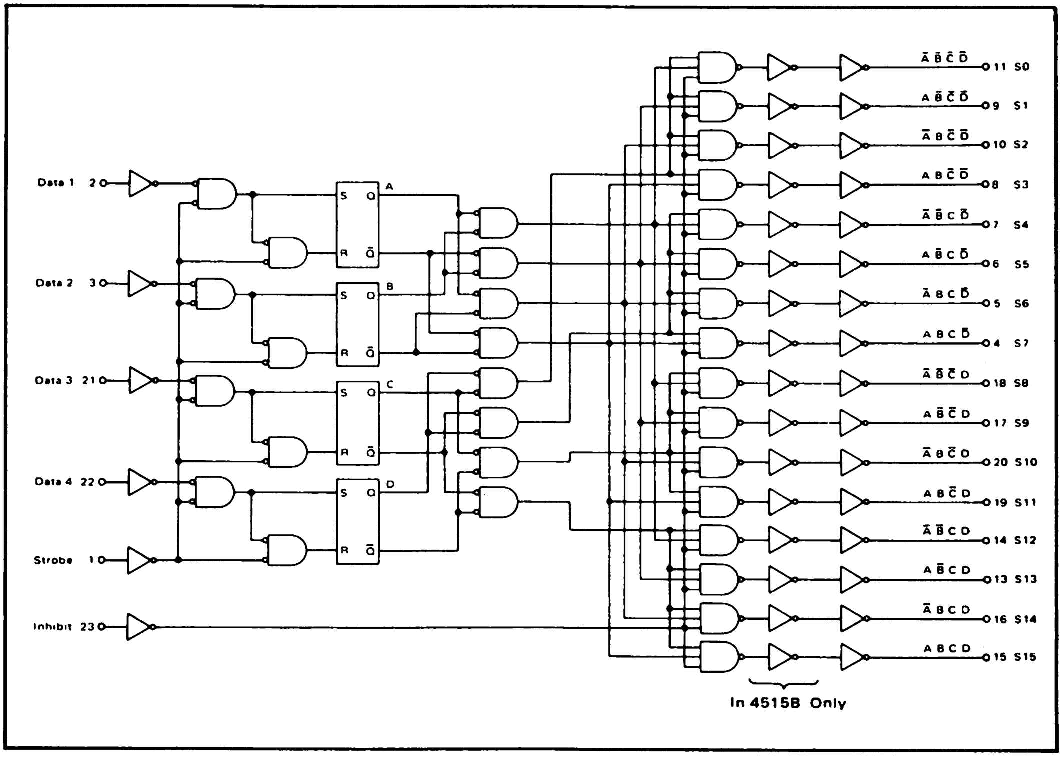


Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

LOGIC DIAGRAM



CMOS BINARY UP/DOWN COUNTER

FEATURES

- Internally Synchronous for High Speed
- Asynchronous Preset Enable
- Asynchronous Reset
- Logic Edge-Clocked Design
- 6MHz Counting Rate @ 10Vdc
- Carry Output for Cascading Stages

DESCRIPTION

The 4516B consists of a four-stage Up/Down Counter with provisions for "look-ahead" carry in both counting modes. The inputs consist of a single Clock, Carry-in (Clock Enable), Reset, Up/Down, Preset Enable, and four individual Jam signals. Four separate buffered Q signals and a Carry-out signal are provided as outputs.

A high Preset Enable signal allows information on the Jam inputs to preset the counter to any state asynchronously with the Clock. A high on the Reset line resets all stages to the "zero" state. The counter is advanced one count at the positive transition of the Clock when the Carry-in and Preset Enable signals are low. Advancement is inhibited when the Carry-in or Preset Enable signals are high. The Carry-out signal is normally high and goes low when the counter reaches its maximum count in the Up mode or the minimum count in the Down mode, provided the Carry-in signal is low. The Carry-in signal in the low state can thus be considered a "Clock Enable." The Carry-in terminal must be connected to V_{SS} when not in use.

The counter counts Up when the Up/Down input is high, and Down when the Up/Down input is low. Multiple packages can be connected in either a parallel-clocking or a ripple-clocking arrangement. Parallel clocking provides synchronous control and hence faster response from all counting outputs. Ripple-clocking allows for longer clock input rise and fall times.

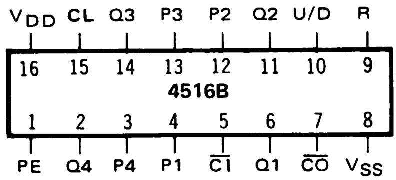
This counter finds primary use in up/down and differential counting and frequency synthesizer applications. It is also useful in A/D and D/A conversion and for magnitude and sign generation.

TRUTH TABLE

$\overline{\text{CARRY IN}}$	UP/DOWN	PRESET ENABLE	RESET	ACTION
1	X	0	0	No Count
0	1	0	0	Count Up
0	0	0	0	Count Down
X	X	1	0	Preset
X	X	X	1	Reset

X = Don't Care

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

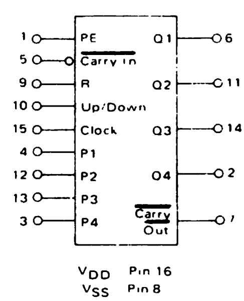
C 16-pin Cerdip
D 16-pin Ceramic
E 16-pin Epoxy
F 16-pin Flat
H Chip

RECOMMENDED OPERATING CONDITIONS

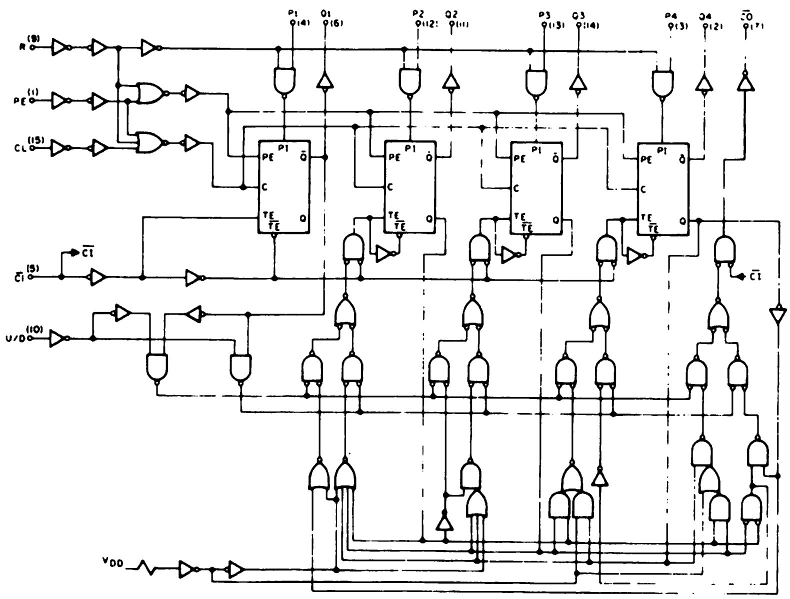
For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

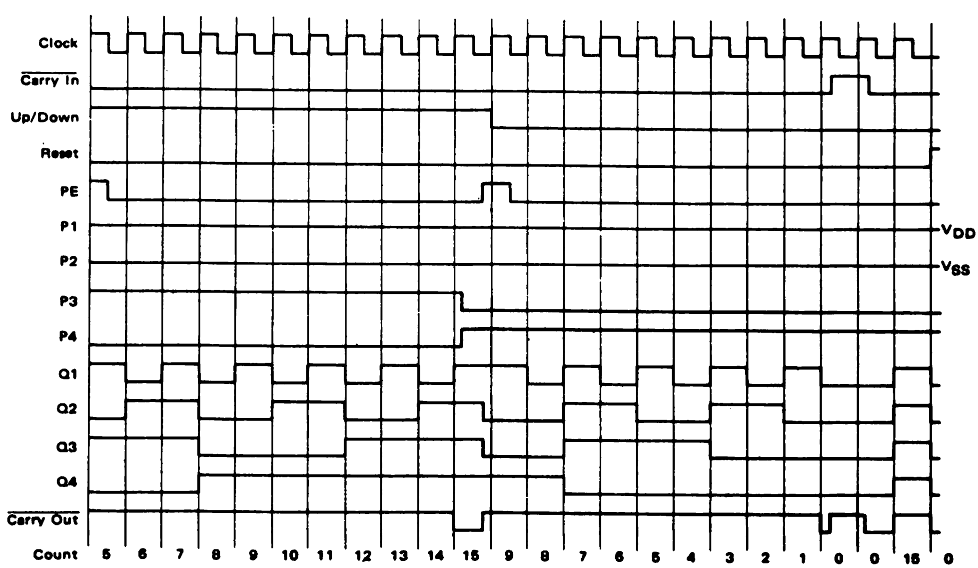
BLOCK DIAGRAM



LOGIC DIAGRAM



TIMING DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS[1]

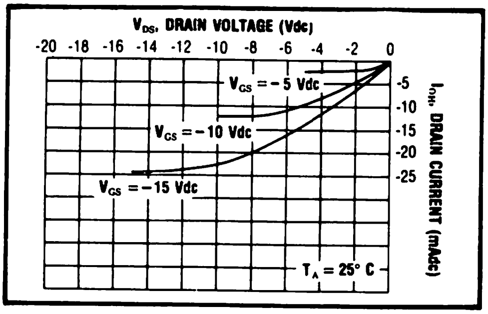
PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[2] Min.	T_{LOW}[2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH}[2] Min.	T_{HIGH}[2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5 10 15	$V_{IN} = V_{SS}$ or V_{DD} All valid input combinations	– – –	5 10 20	– – –	0.05 0.1 0.2	5 10 20	– – –	150 300 600	μAdc

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = –55°C for C, D, F, H device.
= –40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

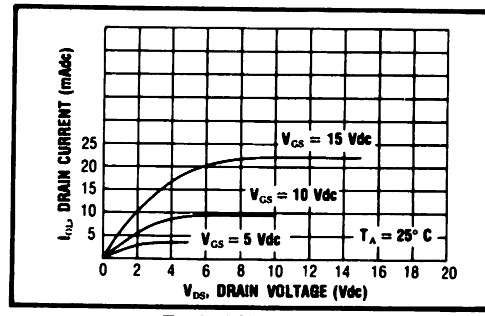
DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME Clock to Q	t_{PLH}, t_{PHL}	5 10 15	– – –	200 100 75	400 200 150	ns
Clock to $\overline{\text{Carry Out}}$		5 10 15	– – –	210 120 90	420 240 180	ns
$\overline{\text{Carry In}}$ to $\overline{\text{Carry Out}}$		5 10 15	– – –	125 60 50	250 120 100	ns
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5 10 15	– – –	100 50 40	200 100 80	ns
MINIMUM CLOCK PULSE WIDTH	PW_{CL}	5 10 15	– – –	170 85 70	340 170 140	ns
MAXIMUM CLOCK FREQUENCY	f_{CL}	5 10 15	2.0 4.0 5.5	4.0 8.0 11.0	– – –	MHz
MAXIMUM CLOCK RISE AND FALL TIME[1]	t_{rCL}, t_{fCL}	5 10 15	15 15 15	– – –	– – –	μs
MINIMUM SETUP TIME $\overline{\text{Carry In}}$	t_{setup}	5 10 15	– – –	130 65 50	260 130 100	ns
Up/Down		5 10 15	– – –	250 100 75	500 200 150	ns
PRESET OR RESET OPERATION						
PROPAGATION DELAY TIME Preset Enable or Reset to Q	t_{PLH}, t_{PHL}	5 10 15	– – –	210 105 90	420 210 180	ns
Preset Enable or Reset to $\overline{\text{Carry Out}}$		5 10 15	– – –	320 160 125	640 320 250	ns
MINIMUM PRESET ENABLE OR RESET PULSE WIDTH	PW_{PE}, PW_R	5 10 15	– – –	100 50 40	200 100 80	ns
PRESET ENABLE OR RESET REMOVAL TIME	t_{rem}	5 10 15	– – –	325 110 90	650 220 180	ns

[1] When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.



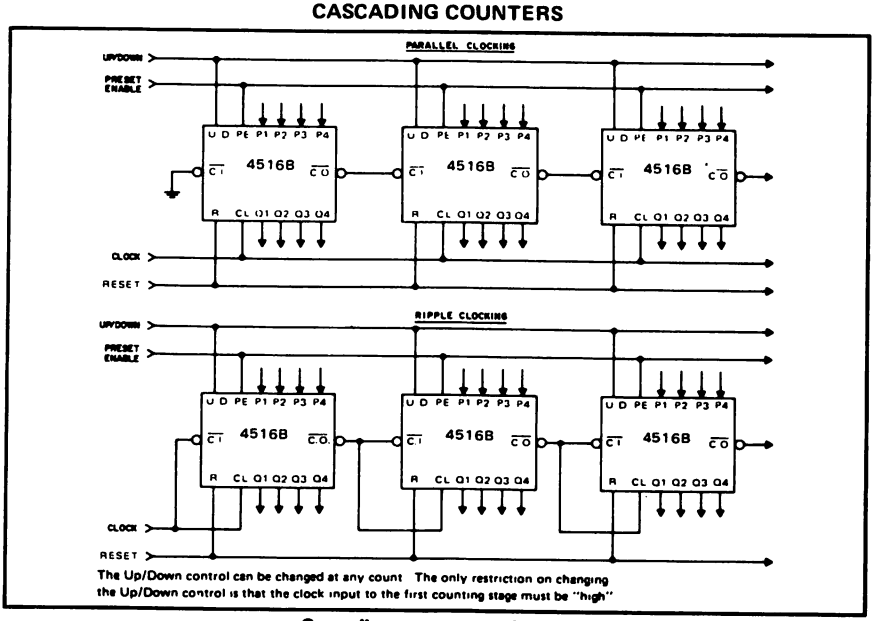
Typical P-Channel
Source Current Characteristics



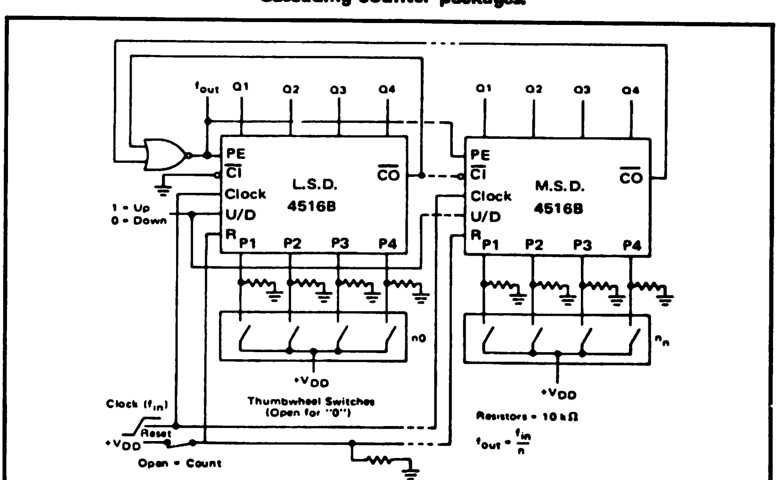
Typical N-Channel
Sink Current Characteristics

APPLICATIONS INFORMATION

CASCADING COUNTERS



Cascading counter packages.



Programmable Cascaded Frequency Divider

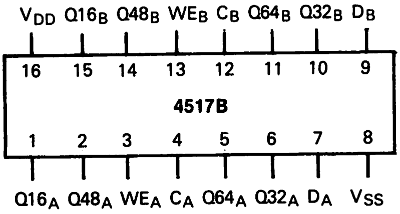
SOLID STATE SCIENTIFIC

CMOS 64-BIT DUAL SHIFT REGISTER

FEATURES

- **Independent Clock, Write Enable Inputs**
- **Static Operation**
- **Positive Edge-Clocked Design**
- **6.7MHz Toggle Rate @ 10 VDC**
- **Tri-State Output at 64th Bit**
- **Balanced Output Drive Current Specifications**

CONNECTION DIAGRAM



DESCRIPTION

The SCL4517B dual 64-bit static shift register consists of two identical, independent, 64-bit registers. Each register has separate clock and write enable inputs, as well as outputs at bits 16, 32, 48, and 64. Data at the data input is entered by clocking, regardless of the state of the write enable input. An output is disabled (open circuited) when the write enable input is high. During this time, data appearing at the data input as well as the 16-bit, 32-bit, and 48-bit taps may be entered into the device by application of a clock pulse. This feature permits the register to be loaded with 64 bits in 16 clock periods, and also permits bus logic to be used. This device is useful in time delay circuits, temporary memory storage circuits, and other serial shift register applications.

FUNCTIONAL TRUTH TABLE

CLOCK	WRITE ENABLE	DATA	16-BIT TAP	32-BIT TAP	48-BIT TAP	64-BIT TAP
0	0	X	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
0	1	X	High Impedance	High Impedance	High Impedance	High Impedance
1	0	X	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
1	1	X	High Impedance	High Impedance	High Impedance	High Impedance
↑	0	Data entered into 1st Bit	Content of 16-Bit Displayed	Content of 33-Bit Displayed	Content of 49-Bit Displayed	Content of 64-Bit Displayed
↑	1	Data entered Into 1st Bit	Data at tap entered into 17-Bit	Data at tap entered into 32-Bit	Data at tap entered into 48-Bit	High Impedance
↓	0	X	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
↓	1	X	High Impedance	High Impedance	High Impedance	High Impedance

X = Don't Care

ELECTRICAL CHARACTERISTICS

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	V_{DD}	+ 15 to − 0.5	V_{dc}
Input Voltage, all inputs	V_{IN}	V_{DD} to − 0.5	V_{dc}
DC Current Drain per Pin	1	10	mAdc
Operating Temperature Range	T_A		
C, D, F, H Device		− 55 to + 125	°C
E Device		− 40 to + 85	°C
Storage Temperature Range	T_{STG}	− 65 to + 150	°C

STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[2]		+ 25°C			T_{HIGH}[2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN} = V_{SS}$ or V_{DD}	—	0.05	—	0.0005	0.05	—	1.5	μAdc
		10	All valid input	—	0.10	—	0.001	0.10	—	3.0	
		15	combinations	—	0.20	—	0.002	0.20	—	6.0	

NOTES: 1 Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".

2 T_{LOW} = − 55°C for C, D, F, H device.
= − 40°C for E device.

T_{HIGH} = + 125°C for C, D, F, H device.
= + 85°C for E device.

SWITCHING CHARACTERISTICS* (T_A = 25°C)

CHARACTERISTIC	SYMBOL	V_{DD}	Min.	Typ. All Types	Max.	Unit
Output Transition Time (C_L = 15pF)	t_r	5.0	—	100	200	ns
	t_{TLH}	10	—	50	100	
	t_{THL}	15	—	40	80	
Propagation Delay Time (C_L = 15 pF)	t_{PLH}					
	t_{PHL}	5.0	—	200	400	ns
		10	—	110	220	
		15	—	90	180	
Minimum Clock Pulse Width	PW_C	5.0	—	170	250	ns
		10	—	75	100	
		15	—	60	75	
Maximum Clock Pulse Frequency	PRF	5.0	2.0	3.0	—	MHz
		10	5.0	6.7	—	
		15	6.7	8.3	—	
Maximum Clock Pulse Rise and Fall Time	t_r, t_f	5.0	—	—	No	—
		10	—	—	Limit	
		15	—	—	**	
Data to Clock Setup Time	t_{setup}	5.0	—	− 40	− 10	ns
		10	—	− 15	0	
		15	—	0	5	
Data to Clock Hold Time	t_{hold}	5.0	—	75	120	ns
		10	—	25	50	
		15	—	10	25	
Write Enable to Clock Setup Time	t_{setup}	5.0	—	170	300	ns
		10	—	65	130	
		15	—	50	80	
Write Enable to Clock Release Time	t_{rel}	5.0	—	160	280	ns
		10	—	55	120	
		15	—	40	70	

*The formula given is for the typical characteristics only.

**When shift register sections are cascaded, the maximum rise and fall time of the clock input should be equal to or less than the rise and fall time of the data outputs, driving data inputs, plus the propagation of the output driving stage for the output capacitance load.

AC TEST WAVEFORMS

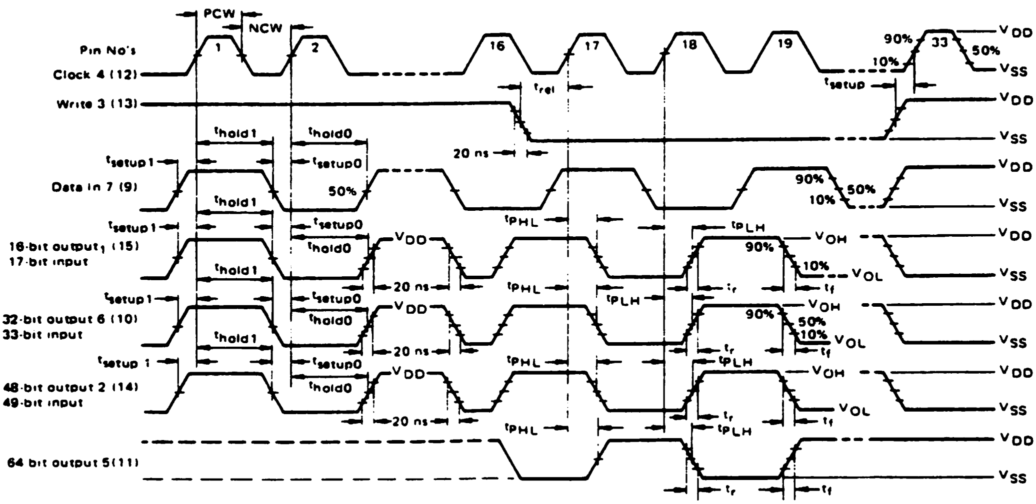
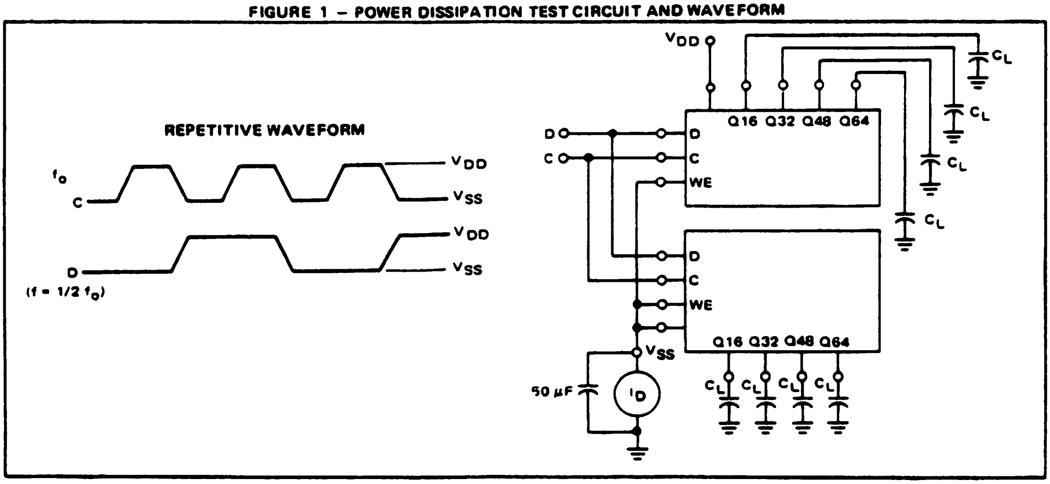
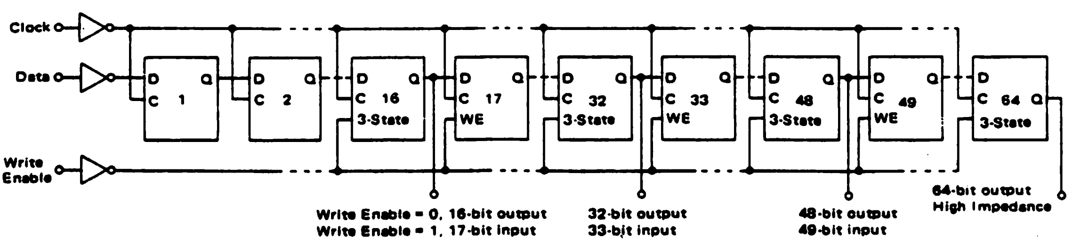


FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



EXPANDED BLOCK DIAGRAM
(1/2 OF DEVICE SHOWN)



SOLID STATE SCIENTIFIC

SCL4518B
SCL4520B

CMOS DUAL UP COUNTERS

FEATURES

- ♦ Two Independent 4-Bit Counters
- ♦ Internally Synchronous for High Speed
- ♦ Dual BCD (4518B) and Dual Binary (4520B) Configurations
- ♦ Direct Reset
- ♦ Logic Edge-Clocked Design
- ♦ Trigger from either Edge of Clock Signal
- ♦ Static Operation— DC to 5MHz @ 10Vdc

DESCRIPTION

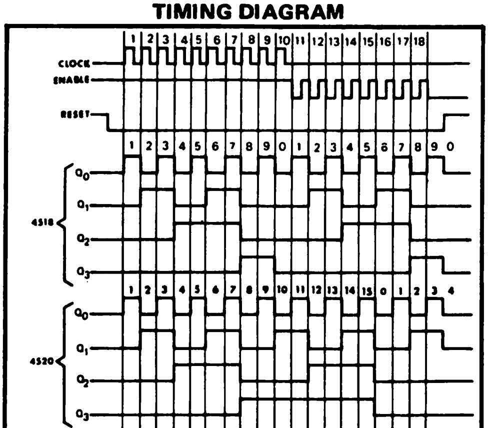
The 4518B Dual BCD Counter and the 4520B Dual Binary Counter are constructed with MOS P-channel and N-channel enhancement-mode devices in a single monolithic structure. Each consists of two identical, independent, internally synchronous 4-stage counters. The counter stages are type-D flip-flops, with interchangeable Clock and Enable lines for incrementing on either the positive-going or negative-going transition as required when cascading multiple stages. Each counter can be cleared by applying a high level on the Reset line. In addition, the 4518B will count out of all undefined states within two clock periods. These complementary MOS up counters find primary use in multi-stage synchronous or ripple counting applications requiring low power dissipation and/or high noise immunity.

TRUTH TABLE

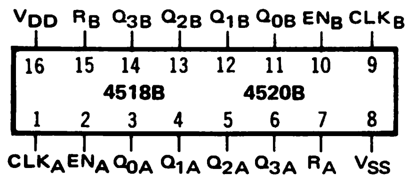
CLOCK	ENABLE	RESET	ACTION
↑	1	0	Increment Counter
0	↓	0	Increment Counter
↓	X	0	No Change
X	↑	0	No Change
↑	0	0	No Change
1	↓	0	No Change
X	X	1	Q0 thru Q3 = 0

X = Don't Care

TIMING DIAGRAM



CONNECTION DIAGRAM
(all packages)



Add suffix for package:

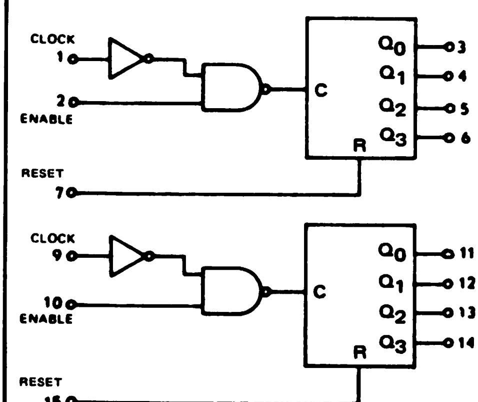
C	16-pin Cerdip
D	16-pin Ceramic
E	16-pin Epoxy
F	16-pin Flat
H	Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

BLOCK DIAGRAM



4518 — Dual BCD Up Counter
4520 — Dual Binary Up Counter

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS[1]

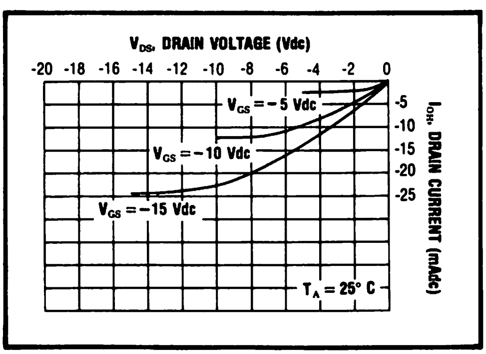
PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[2] Min.	T_{LOW}[2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH}[2] Min.	T_{HIGH}[2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN} = V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	μAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		15	combinations	–	20	–	0.2	20	–	600	

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

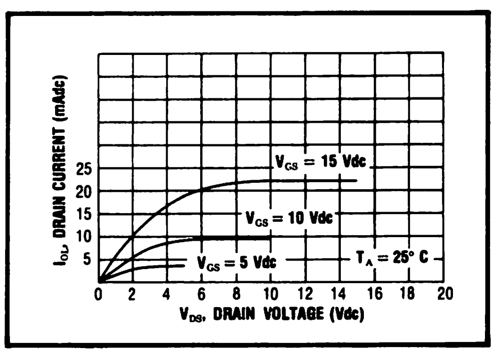
DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME From Clock or Clock Enable	t_{PLH}, t_{PHL}	5	–	225	450	ns
		10	–	100	200	
		15	–	80	160	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
MINIMUM CLOCK PULSE WIDTH	PW_{CL}	5	–	100	200	ns
		10	–	50	100	
		15	–	35	70	
MINIMUM CLOCK ENABLE PULSE WIDTH	PW_{CE}	5	–	200	400	ns
		10	–	100	200	
		15	–	70	140	
MAXIMUM CLOCK FREQUENCY	f_{CL}	5	1.5	3.0	–	MHz
		10	3.0	6.0	–	
		15	4.0	8.0	–	
MAXIMUM CLOCK OR CLOCK ENABLE RISE & FALL TIME[1]	t_{rCL}, t_{fCL}	5	15	–	–	μs
		10	5	–	–	
		15	5	–	–	
RESET OPERATION						
PROPAGATION DELAY TIME	t_{PHL}	5	–	225	450	ns
		10	–	100	200	
		15	–	80	160	
MINIMUM RESET PULSE WIDTH	PW_R	5	–	120	240	ns
		10	–	50	100	
		15	–	40	80	
RESET REMOVAL TIME	t_{rem}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	

[1] When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.

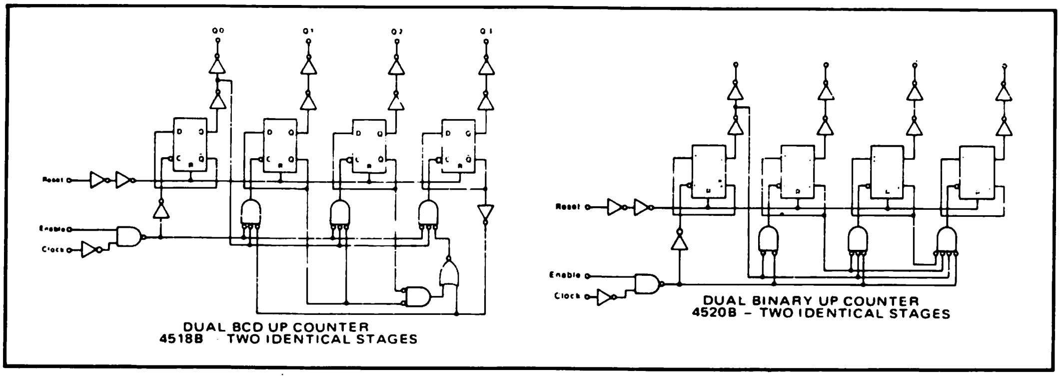


Typical P-Channel
Source Current Characteristics

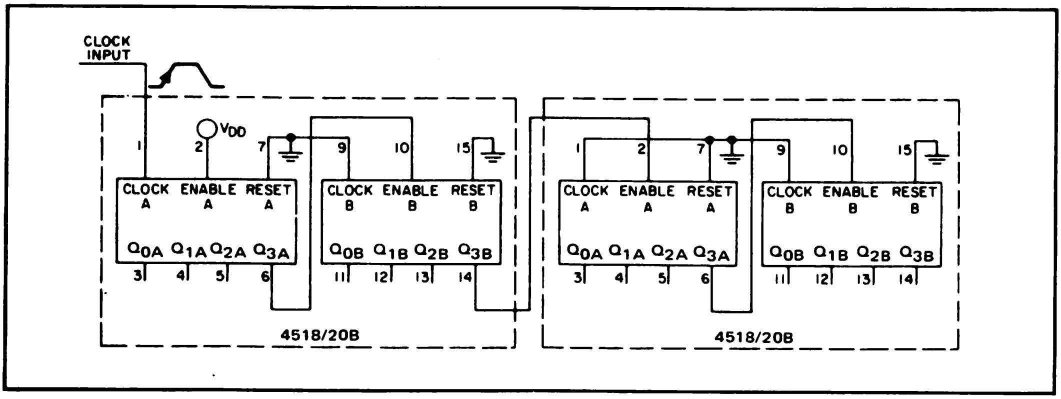


Typical N-Channel
Sink Current Characteristics

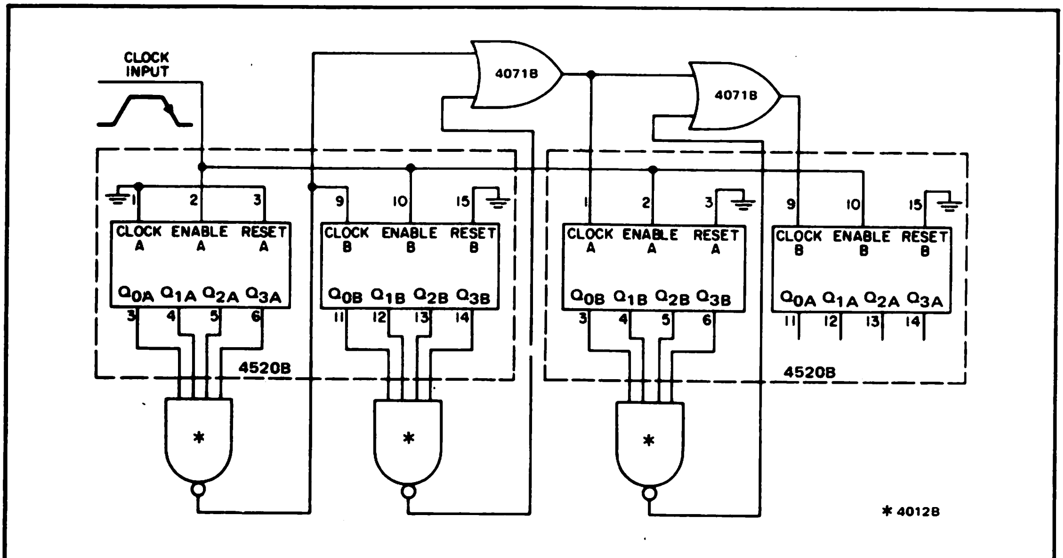
LOGIC DIAGRAMS



APPLICATIONS INFORMATION



Ripple cascading of four counters with positive-edge triggering.



Synchronous cascading of four binary counters with negative-edge triggering.

SOLID STATE SCIENTIFIC

SCL4522B
SCL4526B

CMOS PROGRAMMABLE DOWN COUNTERS

FEATURES

- Internally Synchronous for High Speed
- BCD Decade (4522B) or 4-Bit Binary (4526B) Down Counters
- Asychronous Preset Enable
- Asynchronous Reset
- Cascadable
- Logic Edge-Clocked Design
- Static Operation – DC to 5MHz @ 10Vdc
- Trigger from Either Edge of Clock Input

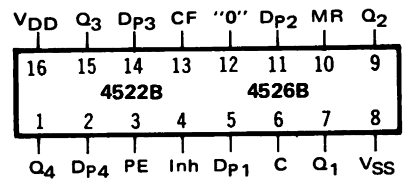
DESCRIPTION

The 4522B BCD Counter and the 4526B Binary Counter are constructed with MOS P-channel and N-channel enhancement-mode devices in a single monolithic structure.

These devices are programmable, cascadable down counters with a decoded "0" state output for divide-by-N applications. In single stage applications the "0" output is applied to the Preset Enable input. The Cascade Feedback input allows cascade divide-by-N operation with no additional gates required. The Master Reset function provides synchronous initiation of divide-by-N cycles. The Clock Inhibit input allows disabling of the pulse counting function.

These complementary MOS counters can be used in frequency synthesizers, phase-locked loops, and other frequency division applications requiring low power dissipation and/or high noise immunity.

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

C	16-pin Cerdip
D	16-pin Ceramic
E	16-pin Epoxy
F	16-pin Flat
H	Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	V_{DD} - V_{SS}	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

TRUTH TABLES

Both Types

Clock	Inhibit	Preset Enable	Master Reset	Action
0	0	0	0	No Count
$\uparrow$	0	0	0	Count-1
X	1	0	0	No Count
1	$\downarrow$	0	0	Count 1
X	X	1	0	Preset
X	X	X	1	Reset

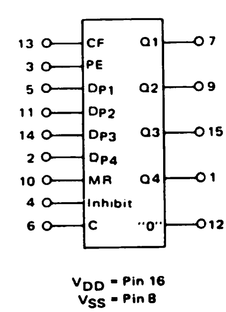
4522B

Count	Output Q4	Q3	Q2	Q1
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

4526B

Count	Output Q4	Q3	Q2	Q1
15	1	1	1	1
14	1	1	1	0
13	1	1	0	1
12	1	1	0	0
11	1	0	1	1
10	1	0	1	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS [1]

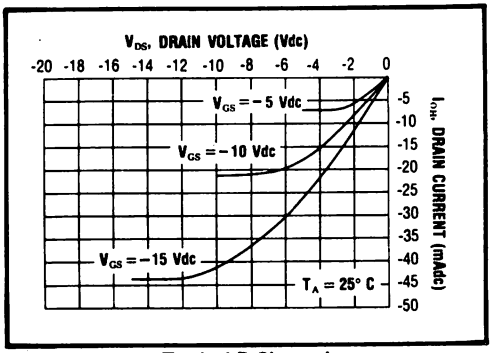
PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2]		+25°C			T_{HIGH} [2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5 10 15	$V_{IN}=V_{SS}$ or V_{DD} All valid input combinations	– – –	5 10 20	– – –	0.05 0.1 0.2	5 10 20	– – –	150 300 600	μAdc

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

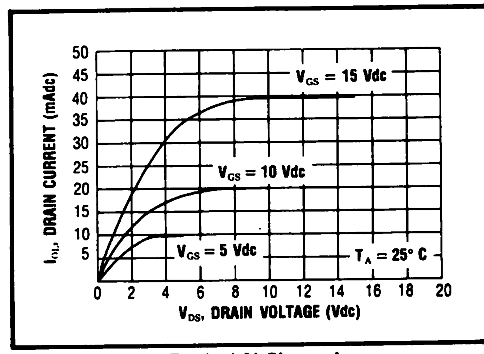
DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (V dc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME Clock or Inhibit to Q	t_{PLH}, t_{PHL}	5 10 15	– – –	415 160 120	830 320 240	ns
Clock or Inhibit to "O"		5 10 15	– – –	175 125 100	350 250 200	ns
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5 10 15	– – –	100 50 40	200 100 80	ns
MINIMUM CLOCK PULSE WIDTH	PW_{CL}	5 10 15	– – –	125 50 40	250 100 80	ns
MAXIMUM CLOCK FREQUENCY	f_{CL}	5 10 15	1.5 3.0 4.0	2.0 5.0 6.6	– – –	MHz
MAXIMUM CLOCK OR INHIBIT RISE AND FALL TIME[1]	t_{rCL}, t_{fCL}	5 10 15	15 15 15	– – –	– – –	μs
PRESET OPERATION						
PROPAGATION DELAY TIME PE to Q	t_{PLH}, t_{PHL}	5 10 15	– – –	415 160 120	830 320 240	ns
PE to "O"		5 10 15	– – –	175 125 100	350 250 200	ns
MINIMUM PRESET ENABLE PULSE WIDTH	PW_{PE}	5 10 15	– – –	125 50 40	250 100 80	ns
MINIMUM DATA INPUT HOLD TIME	t_{hold}	5 10 15	– – –	75 25 20	125 50 40	ns
RESET OPERATION						
PROPAGATION DELAY TIME MR to Q	t_{PHL}	5 10 15	– – –	415 160 120	830 320 240	ns
MR to "O"	t_{PLH}	5 10 15	– – –	175 125 100	350 250 200	ns
MINIMUM MASTER RESET PULSE WIDTH	PW_{MR}	5 10 15	– – –	150 125 100	300 250 200	ns

[1] When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.

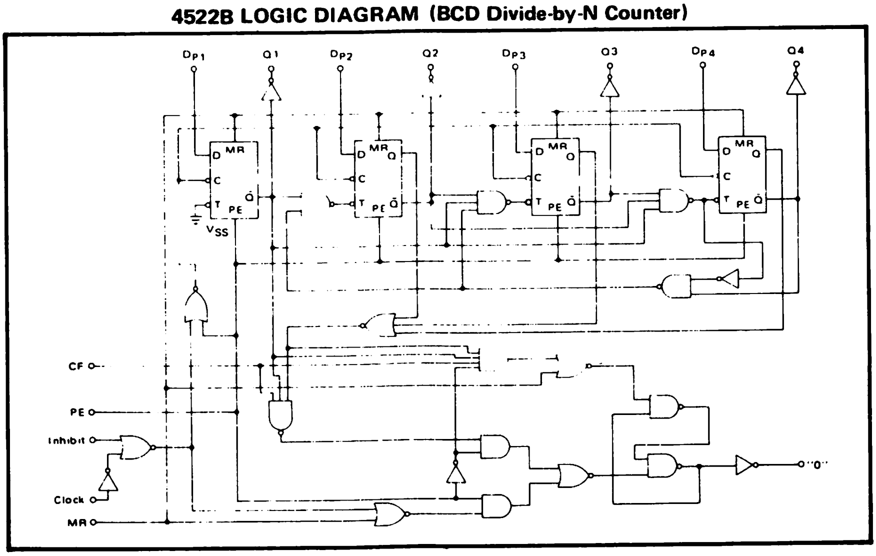


Typical P-Channel
Source Current Characteristics

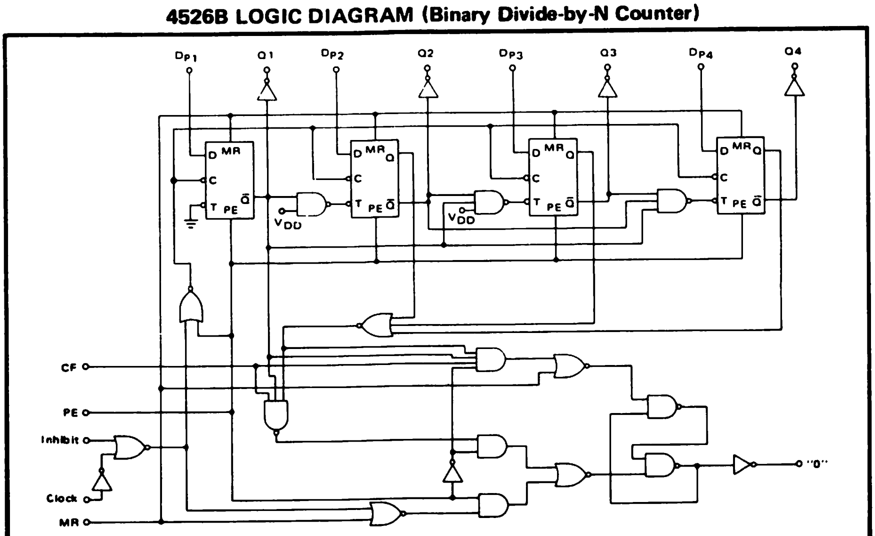


Typical N-Channel
Sink Current Characteristics

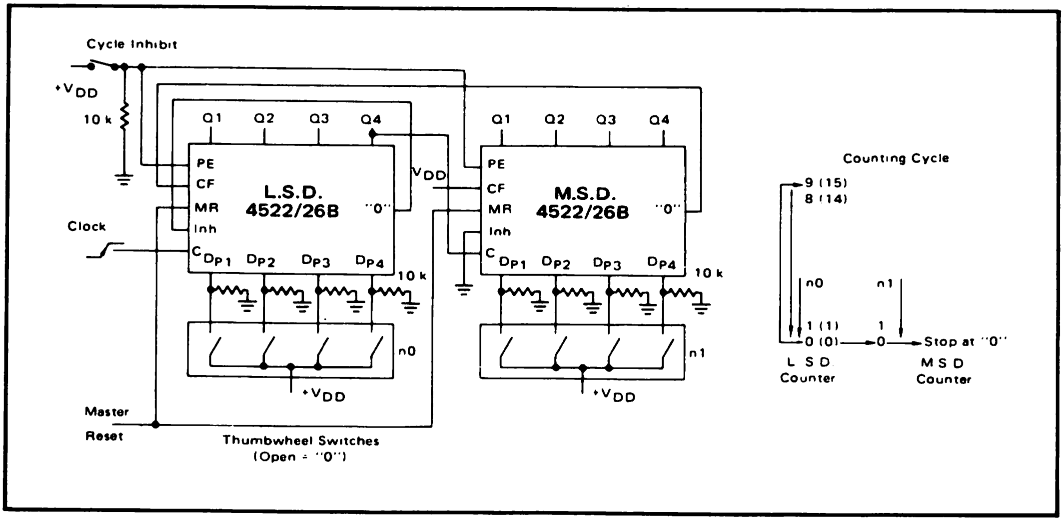
4522B LOGIC DIAGRAM (BCD Divide-by-N Counter)



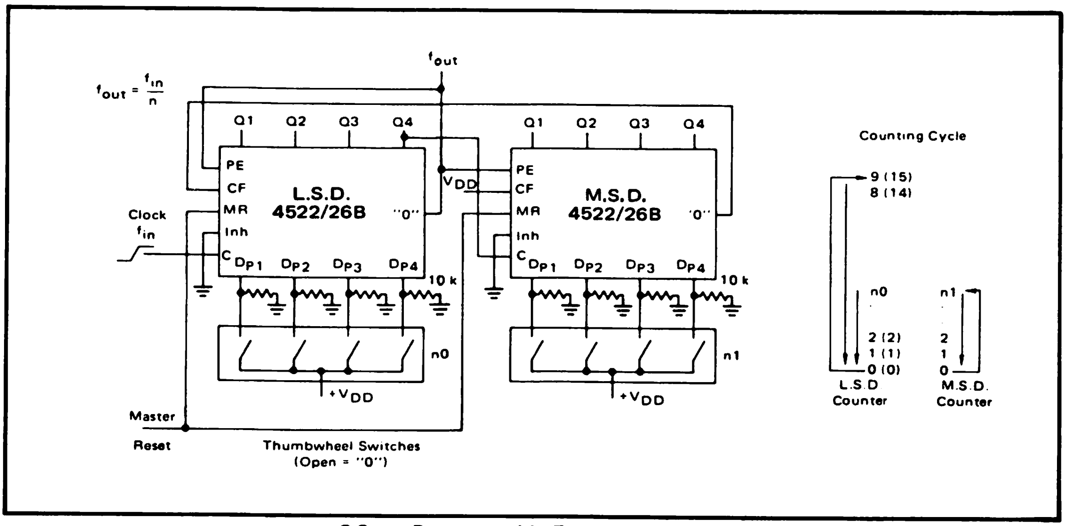
4526B LOGIC DIAGRAM (Binary Divide-by-N Counter)



APPLICATIONS INFORMATION



2-Stage Programmable Down Counter (One Cycle)



2-Stage Programmable Frequency Divider

CMOS BCD RATE MULTIPLIER

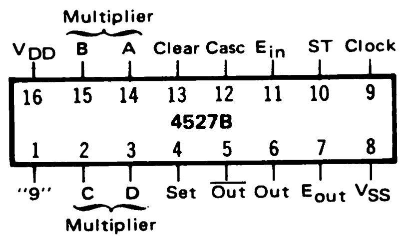
FEATURES

- Internally Synchronous for High Speed
- Strobe for Enabling or Inhibiting Outputs
- Enable and Cascade Inputs
- "9" Output Available for Cascading
- Complementary Outputs
- Clear and Set-To-Nine Inputs

DESCRIPTION

The 4527B is a BCD Digital Rate Multiplier (DRM) which provides an output pulse rate of the clock input pulse rate multiplied by 1/10 of the BCD input. For example, when the BCD input is 8, there will be 8 output pulses for every 10 input pulses. The output is clocked on the negative-going edge of the input clock. This device may be used to perform arithmetic operations, solve algebraic and differential equations, generate logarithms and trigonometric functions, A/D and D/A conversion, and frequency division.

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

C	16-pin Cerdip
D	16-pin Ceramic
E	16-pin Epoxy
F	16-pin Flat
H	Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

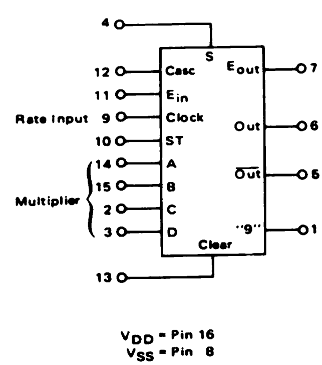
DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

TRUTH TABLE

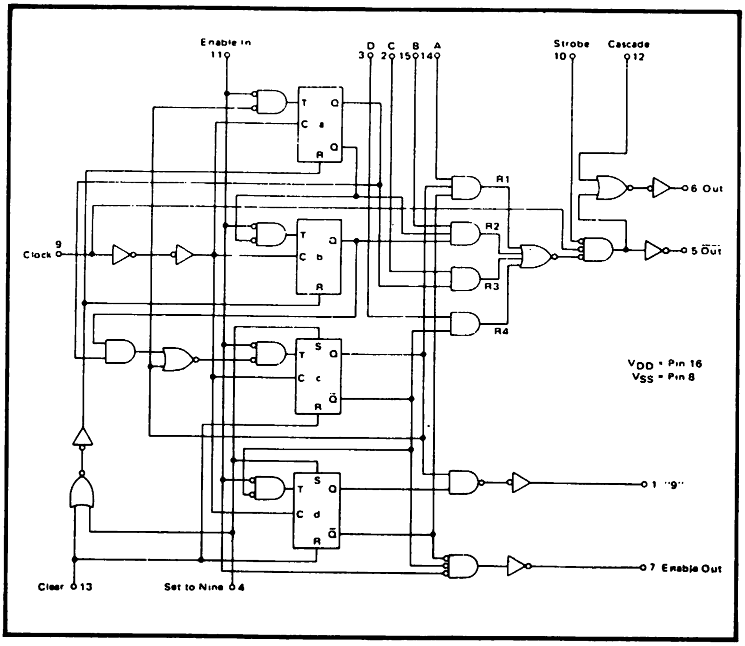
Inputs										Number of Pulses or Output Logic Level (H or L)			
D	C	B	A	No. of Clock Pulses	E_{IN}	Strobe	Cascade	Clear	Set	Pin 6 OUT	Pin 5 $\overline{OUT}$	Pin 7 E_{OUT}	Pin 1 "9"
0	0	0	0	10	0	0	0	0	0	L	H	1	1
0	0	0	1	10	0	0	0	0	0	1	1	1	1
0	0	1	0	10	0	0	0	0	0	2	2	1	1
0	0	1	1	10	0	0	0	0	0	3	3	1	1
0	1	0	0	10	0	0	0	0	0	4	4	1	1
0	1	0	1	10	0	0	0	0	0	5	5	1	1
0	1	1	0	10	0	0	0	0	0	6	6	1	1
0	1	1	1	10	0	0	0	0	0	7	7	1	1
1	0	0	0	10	0	0	0	0	0	8	8	1	1
1	0	0	1	10	0	0	0	0	0	9	9	1	1
1	0	1	0	10	0	0	0	0	0	8	8	1	1
1	0	1	1	10	0	0	0	0	0	9	9	1	1
1	1	0	0	10	0	0	0	0	0	8	8	1	1
1	1	0	1	10	0	0	0	0	0	9	9	1	1
1	1	1	0	10	0	0	0	0	0	8	8	1	1
1	1	1	1	10	0	0	0	0	0	9	9	1	1
X	X	X	X	10	1	0	0	0	0	Depends on internal state of counter			
X	X	X	X	10	0	1	0	0	0	L	H	1	1
X	X	X	X	10	0	0	1	0	0	H	*	1	1
1	X	X	X	10	0	0	0	1	0	10	10	H	L
0	X	X	X	10	0	0	0	1	0	L	H	H	L
X	X	X	X	10	0	0	0	0	1	L	H	L	H

*Output same as the first 16 lines of this truth table (depending on values of A, B, C, D).

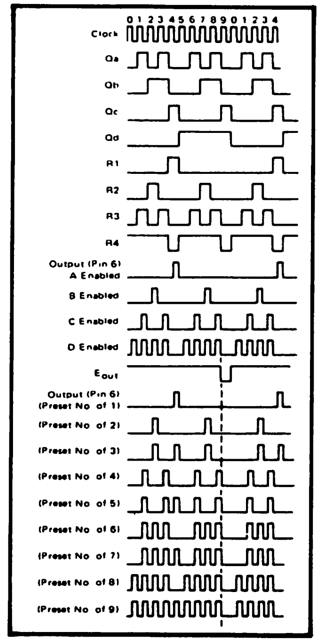
BLOCK DIAGRAM



LOGIC DIAGRAM



TIMING DIAGRAM

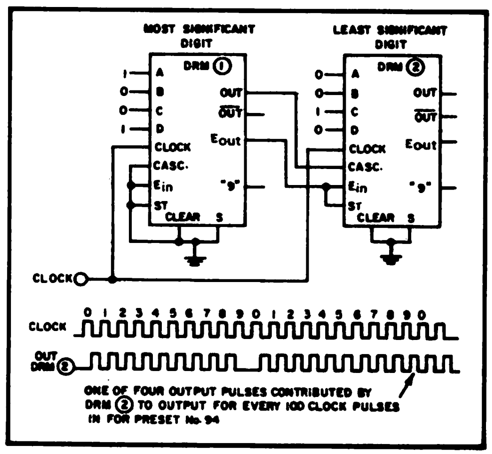


APPLICATIONS INFORMATION

Cascading Connections

For words of more than one digit, 4527B devices may be cascaded in two different modes: an Add mode and a Multiply mode.

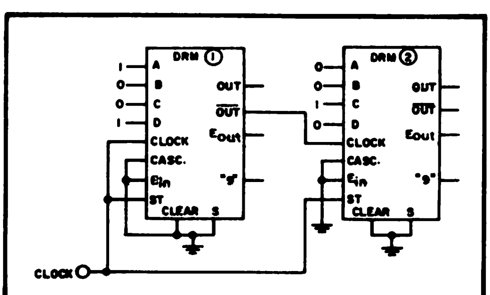
In the Add mode, some of the gaps left by the more significant unit at the count of 9 are filled in by the less significant units. Output Rate = Clock Rate X (0.1 BCD_1 + 0.01 BCD_2 + . . .)



Two 4527B's cascaded in the "Add" mode with a preset number of 94.

In the Multiply mode, the fraction programmed into the first DRM is multiplied by the fraction programmed into the second one.

$$\text{Output Rate} = \text{Clock Rate} \times \frac{BCD_1}{10} \times \frac{BCD_2}{10} \times \ldots$$



Two 4527B's cascaded in the "Multiply" mode with a preset number of 36.

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS[1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[2] Min.	T_{LOW}[2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH}[2] Min.	T_{HIGH}[2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN}=V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	μAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		15	combinations	–	20	–	0.2	20	–	600	

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME Clock to Out	t_{PLH}, t_{PHL}	5	–	150	300	ns
		10	–	75	150	
		15	–	60	120	
Clock to Out		5	–	95	190	ns
		10	–	50	100	
		15	–	35	70	
Clock to E_{out}		5	–	250	500	ns
		10	–	100	200	
		15	–	75	150	
Clock to "9"		5	–	300	600	ns
		10	–	125	250	
		15	–	100	200	
Cascade to Out		5	–	95	190	ns
		10	–	50	100	
		15	–	35	70	
Strobe to Out		5	–	175	350	ns
		10	–	80	160	
		15	–	60	120	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	130	260	ns
		10	–	65	130	
		15	–	50	100	
MINIMUM CLOCK PULSE WIDTH	PW_{CL}	5	–	165	330	ns
		10	–	85	170	
		15	–	65	130	
MAXIMUM CLOCK FREQUENCY	f_{CL}	5	1.5	3.0	–	MHz
		10	3.0	6.0	–	
		15	4.0	8	–	
MAXIMUM CLOCK RISE AND FALL TIME[1]	t_{rCL}, t_{fCL}	5	15	–	–	μs
		10	15	–	–	
		15	15	–	–	
MINIMUM ENABLE IN SETUP TIME	t_{setup}	5	–	175	350	ns
		10	–	60	120	
		15	–	45	90	
SET OR CLEAR OPERATION						
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}	5	–	350	700	ns
		10	–	150	300	
		15	–	115	230	
MINIMUM SET OR CLEAR PULSE WIDTH	PW_S, PW_C	5	–	90	180	ns
		10	–	35	70	
		15	–	30	60	
SET OR CLEAR REMOVAL TIME	t_{rem}	5	–	-20	0	ns
		10	–	-10	0	
		15	–	- 7.5	0	

[1] When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.

APPLICATIONS INFORMATION

Multiplication of Two Variables

$R_1 = f_{CLK}\left(\frac{A}{10}\right)$

$R_2 = f_{CLK}\left(\frac{A}{10}\right)\left(\frac{B}{10}\right) = f_{CLK}\left(\frac{AB}{100}\right)$

$R_3 = f_{CLK}\left(\frac{N}{10}\right)$

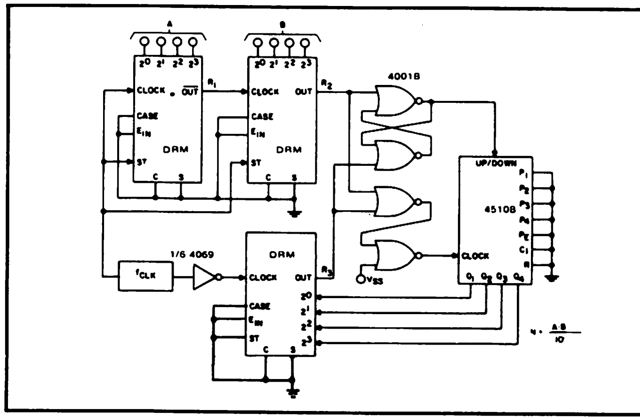
R_2 addresses "up" count, R_3 addresses "down" count. The interface circuit converts to a single clock with mode control. When loop stabilizes,

$R_2 = R_3$

$f_{CLK}\left(\frac{AB}{100}\right) = f_{CLK}\left(\frac{N}{10}\right)$

or $N = \frac{AB}{10}$

Note: To prevent simultaneous "up" and "down" commands, a multiphase clock input must be used.



Generation of $A^{2/3}$

$R_1 = f_{CLK}\left(\frac{A^2}{100}\right)\left(\frac{1}{10}\right) = f_{CLK}\left(\frac{A^2}{1000}\right)$

$R_2 = f_{CLK}\left(\frac{N^3}{1000}\right)$

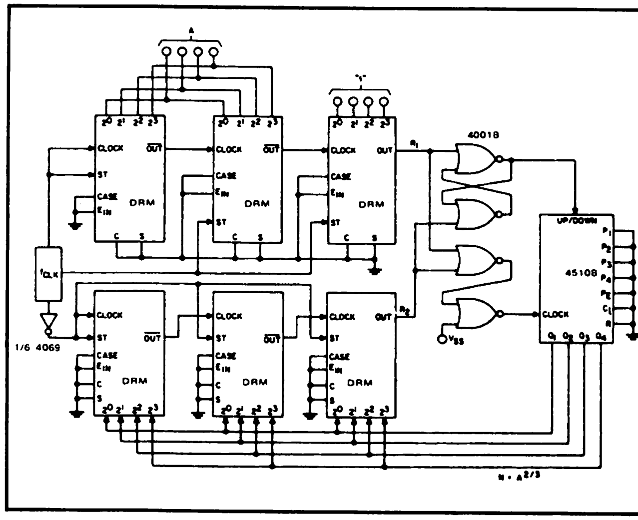
At equilibrium,

$R_1 = R_2$

$N^3 = A^2$

or $N = A^{2/3}$

Note: To prevent simultaneous "up" and "down" commands, a multiphase clock input must be used.



Frequency Ratios

$R_1 = f_1/10^n$

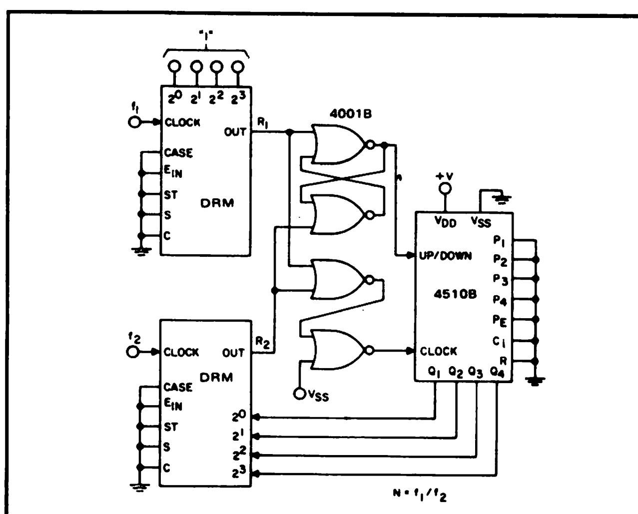
$R_2 = f_2N/10^n$ where n = number of stages

At equilibrium,

$R_1 = R_2$

$N = f_1/f_2$

Note: To prevent simultaneous commands (overlap), f_1 and f_2 may require preconditioning.



CMOS DUAL MONOSTABLE MULTIVIBRATOR

FEATURES

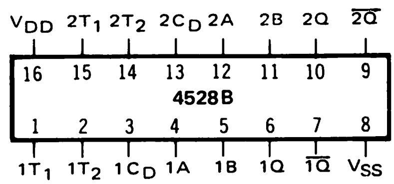
- Two Independent Multivibrators on One Chip
- Triggerable from Leading- or Trailing-Edge Pulse
- Retriggerable
- Resettable
- Q and $\overline{Q}$ Buffered Outputs Available
- Wide Range of Output Pulse Widths

DESCRIPTION

The 4528B Dual Multivibrator provides stable retriggerable/resettable one-shot operation for any fixed-voltage timing application. Timing for the circuit is controlled by an external resistor-capacitor combination (R_X-C_X). Adjustment of these components permits generation of output pulse widths from nanoseconds to minutes. Leading-edge and trailing-edge Trigger inputs are provided, and both positive-going and negative-going pulses are available from complementary outputs.

Timing pulses may be terminated at any time by applying a low logic level to the Reset input C_D.

CONNECTION DIAGRAM
(all packages)



RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

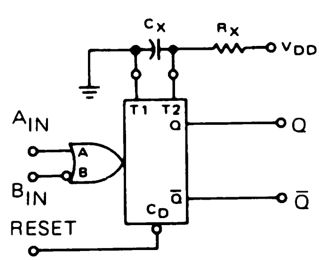
DC Supply Voltage	$V_{DD} \cdot V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

FUNCTION TABLE

INPUTS			OUTPUTS	
C_D	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	↑	H	⎍	⊔
H	L	↓	⎍	⊔

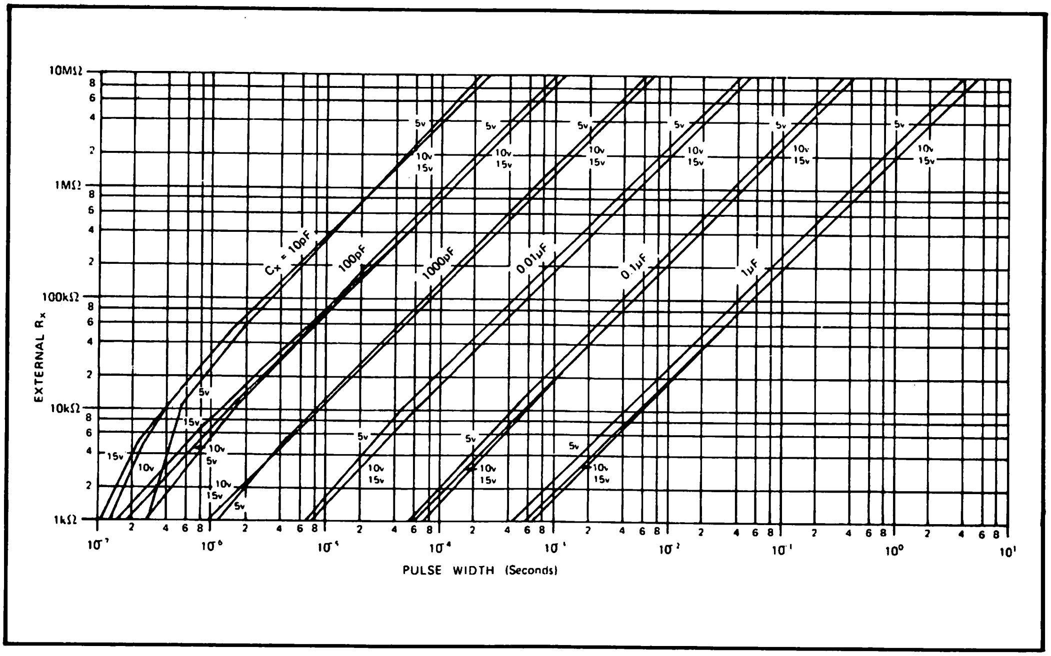
H = High Level (Steady State)
L = Low Level (Steady State)
↑ = Transition, Low-to-High
↓ = Transition, High-to-Low
X = Irrelevant (Inc. Transitions)
⎍ = One High-Level Pulse
⊔ = One Low-Level Pulse

BLOCK DIAGRAM
(one of two devices)

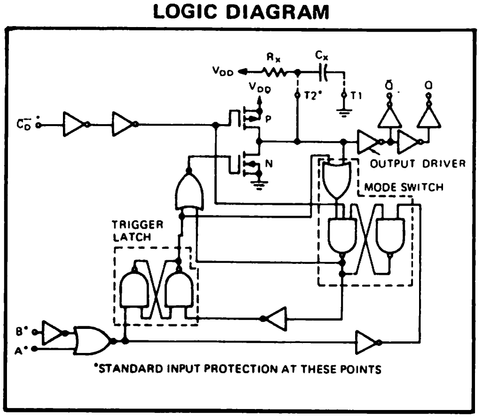


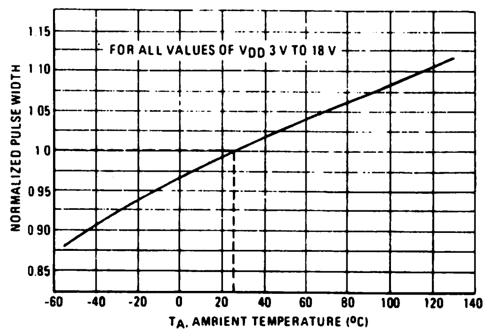
R_X and C_X are external components.

4528B PULSE WIDTH VS. R_X, C_X, V_{DD}



LOGIC DIAGRAM





Normalized Pulse Width versus Temperature

Notes:

There is no effective maximum limit on R_X; recommended minimum value for R_X is 1KΩ. There are no restrictions on the value of C_X.

For proper operation all unused inputs should be tied to a logic level. The mode point (T2) of a unused half of device should be tied high through an external resistor to V_{DD}.

ELECTRICAL CHARACTERISTICS

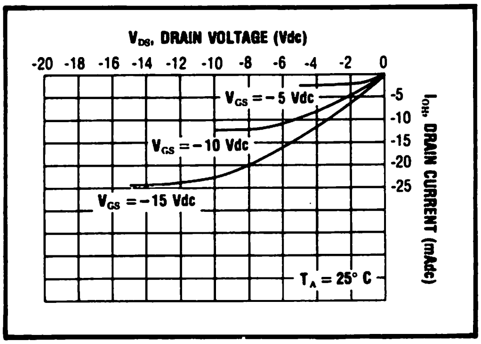
STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[2] Min.	T_{LOW}[2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH}[2] Min.	T_{HIGH}[2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN} = V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	μAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		20	combinations	–	20	–	0.2	20	–	600	

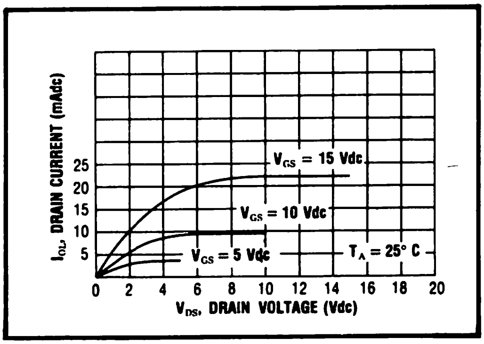
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		Cx (pF)	Rx (kΩ)	V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}							
From A or B		15	5	5	–	270	540	ns
				10	–	90	180	
				15	–	70	140	
		1000	10	5	–	510	1020	ns
				10	–	170	340	
				15	–	120	240	
From C_D		15	5	5	–	270	540	ns
				10	–	90	180	
				15	–	70	140	
		1000	10	5	–	550	1100	ns
				10	–	300	600	
				15	–	250	500	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	–	–	5	–	130	260	ns
				10	–	65	130	
				15	–	50	100	
Note: $\bar{Q}$ Output	t_{TLH}	15	5	5	–	130	260	ns
				10	–	65	130	
				15	–	50	100	
		1000	10	5	–	270	540	ns
				10	–	240	480	
				15	–	220	440	
MINIMUM INPUT PULSE WIDTH A or B Input	PW_{in}	–	–	5	–	70	140	ns
				10	–	30	60	
				15	–	25	50	
OUTPUT PULSE WIDTH MATCH Same package	ΔPW_{out}	1000	10	5	–	± 7.5	±15	%
				10	–	±10	±20	
				15	–	±10	±20	
Different packages		1000	10	5	–	–	±50	%
				10	–	–	±50	
				15	–	–	±50	

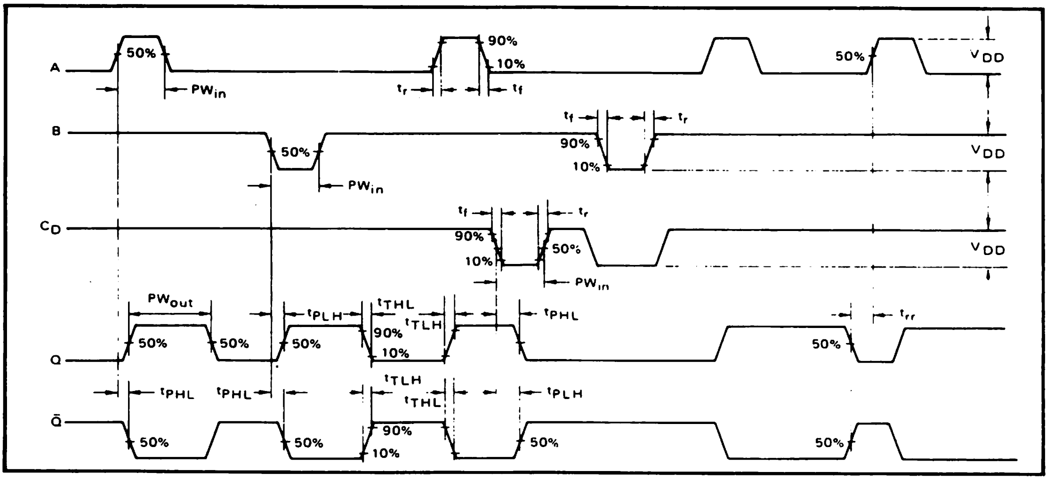


Typical P-Channel
Source Current Characteristics

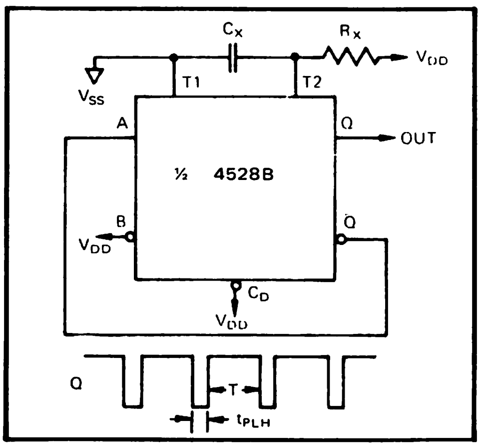


Typical N-Channel
Sink Current Characteristics

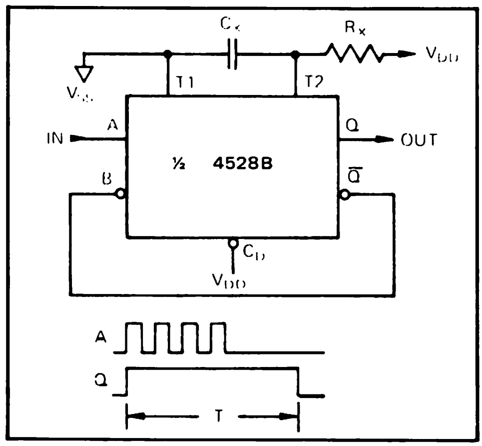
AC TEST WAVEFORMS



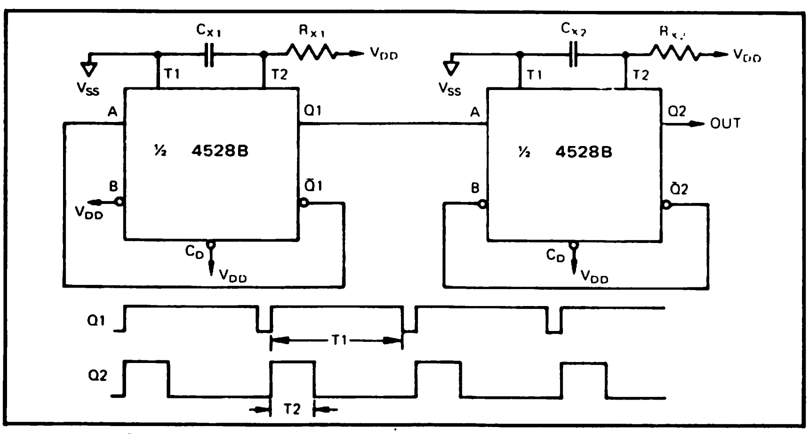
APPLICATIONS INFORMATION



Astable Operation



Connection for Non-Retriggerable Operation



Astable Multivibrator with Adjustable Period and Duty Cycle

SOLID STATE SCIENTIFIC

CMOS 12-BIT PARITY TREE

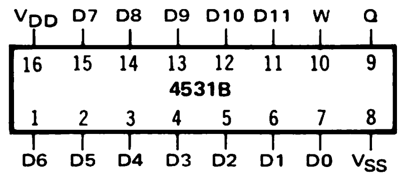
FEATURES

- Variable Word Length
- Buffered Output
- Parity Selection Input

DESCRIPTION

The 4531B 12-Bit Parity Tree is constructed with MOS P-channel and N-channel enhancement-mode devices in a single monolithic structure. The circuit consists of 12 Data-bit inputs (D0 thru D11), an even or odd Parity Selection input (W), and an output (Q). The Parity Selection input can be considered as an additional bit. Words of less than 13 bits can generate an even or odd parity output if the remaining inputs are selected to contain an even number of 1's. Words of greater than 12 bits can be accommodated by cascading other 4531B devices by using the W input. Applications include checking or including a redundant (parity) bit to a word for error detection/correction systems, controller for remote digital sensors or switches (digital event detection/correction), or as a multiple-input summer without carries.

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

C	16-pi-- Cerdip
D	16-pin Ceramic
E	16-pin Epoxy
F	16-pin Flat
H	Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

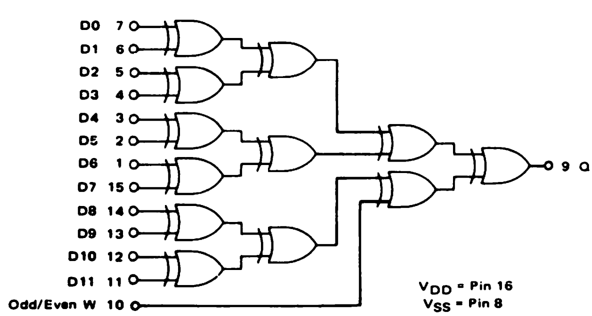
TRUTH TABLE

INPUTS								OUTPUT
W	D11	D10	. . .	D2	D1	D0	DECIMAL (OCTAL) EQUIVALENT	Q*
0	0	0	. . .	0	0	0	0 (0)	0
0	0	0	. . .	0	0	1	1 (1)	1
0	0	0	. . .	0	1	0	2 (2)	1
0	0	0	. . .	0	1	1	3 (3)	0
0	0	0	. . .	1	0	0	4 (4)	1
0	0	0	. . .	1	0	1	5 (5)	0
0	0	0	. . .	1	1	0	6 (6)	0
0	0	0	. . .	1	1	1	7 (7)	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	. . .	0	0	0	8184 (17770)	0
1	1	1	. . .	0	0	1	8185 (17771)	1
1	1	1	. . .	0	1	0	8186 (17772)	1
1	1	1	. . .	0	1	1	8187 (17773)	0
1	1	1	. . .	1	0	0	8188 (17774)	1
1	1	1	. . .	1	0	1	8189 (17775)	0
1	1	1	. . .	1	1	0	8190 (17776)	0
1	1	1	. . .	1	1	1	8191 (17777)	1

*0 = Even Parity
1 = Odd Parity

Note May redefine to suit application by manipulating W and/or other available D's

LOGIC DIAGRAM



$Q = D0 \oplus D1 \oplus D2 \oplus \ldots . \oplus D11 \oplus W$

ELECTRICAL CHARACTERISTICS

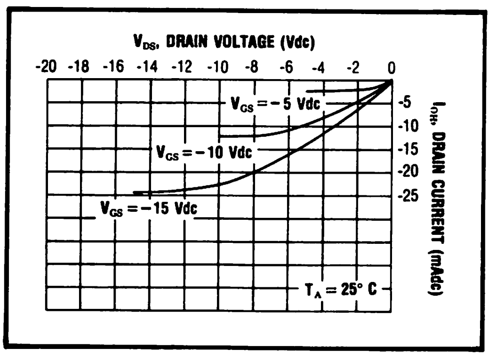
STATIC CHARACTERISTICS[1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[2] Min.	T_{LOW}[2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH}[2] Min.	T_{HIGH}[2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN} = V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	μAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		15	combinations	–	20	–	0.2	20	–	600	

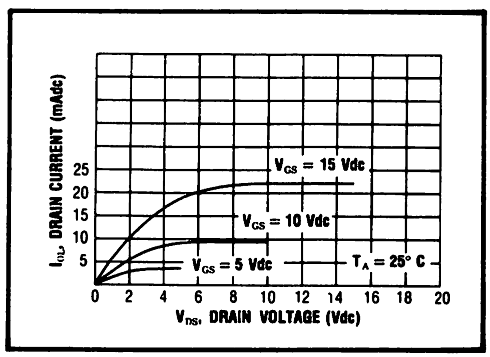
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME From D Inputs	t_{PLH}, t_{PHL}	5	–	420	840	ns
		10	–	175	350	
		15	–	120	240	
From W Input	t_{PLH}, t_{PHL}	5	–	250	500	ns
		10	–	100	200	
		15	–	70	140	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	130	260	ns
		10	–	65	130	
		15	–	50	100	



Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

CMOS 8-BIT PRIORITY ENCODER

FEATURES

- Converts from 1 of 8 binary
- Provides cascading features to handle any number of inputs
- group select indicates one or more priority inputs
- Standardized, symmetrical output characteristics
- Noise margin (full package-temperature range):
  - 1V at V_{DD} = 5V
  - 2V at V_{DD} = 10V
  - 2.5V at V_{DD} = 15V
- 5V, 10V, and 15V parametric ratings

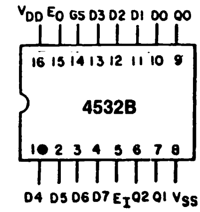
APPLICATIONS

- Priority encoder
- Binary or BCD encoder (keyboard encoding)
- Floating point arithmetic

DESCRIPTION

The 4532B consists of combinational logic that encodes the highest priority input (D7-D0) to a 3-bit binary code. The eight inputs, D7 through D0, each have an assigned priority; D7 is the highest priority and D0 is the lowest. The priority encoder is inhibited when the chip-enable input E_1 is low. Then E_1 is high, the binary representation of the highest-priority input appears on output lines Q2-Q0, and the group select line GS is high to indicate that priority inputs are present. The enable-out (E_0) is high when no priority inputs are present. If any one input is high, E_0 is low and all cascaded lower-order stages are disabled.

CONNECTION DIAGRAM

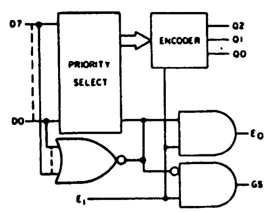


RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	Min.	Max.	Units
Supply Voltage Range (for T_A = Full Package Temp. Range)	3	15	V

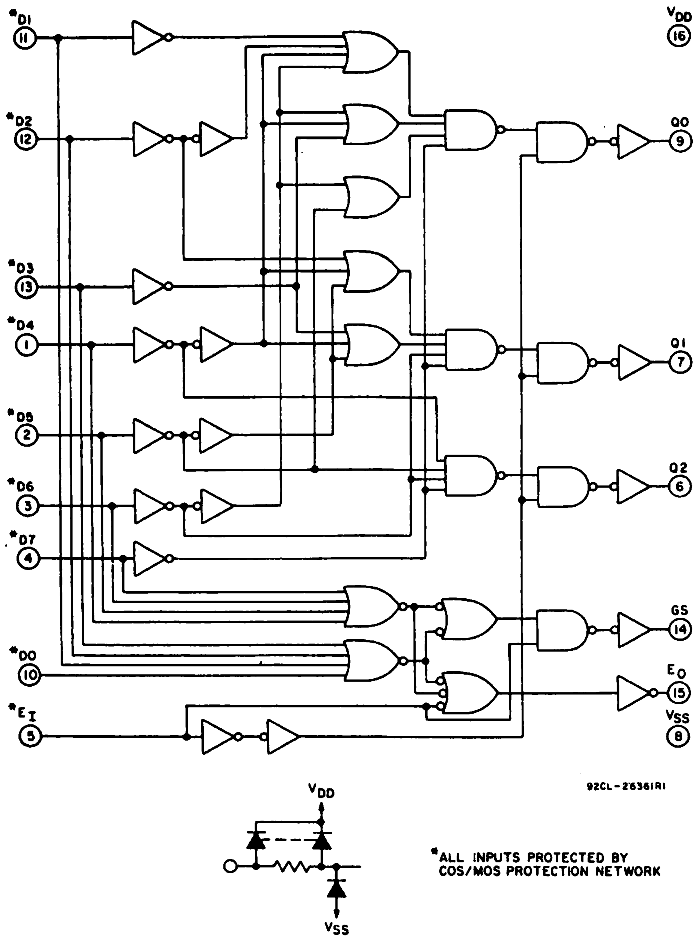
FUNCTIONAL DIAGRAM



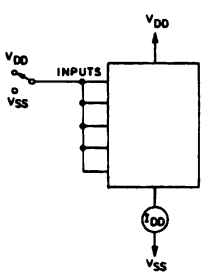
TRUTH TABLE

Input									Output				
E_I	D7	D6	D5	D4	D3	D2	D1	D0	GS	Q2	Q1	Q0	E_O
0	X	X	X	X	X	X	X	X	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	1
1	1	X	X	X	X	X	X	X	1	1	1	1	0
1	0	1	X	X	X	X	X	X	1	1	1	0	0
1	0	0	1	X	X	X	X	X	1	1	0	1	0
1	0	0	0	1	X	X	X	X	1	1	0	0	0
1	0	0	0	0	1	X	X	X	1	0	1	1	0
1	0	0	0	0	0	1	X	X	1	0	1	0	0
1	0	0	0	0	0	0	1	X	1	0	0	1	0
1	0	0	0	0	0	0	0	1	1	0	0	0	0

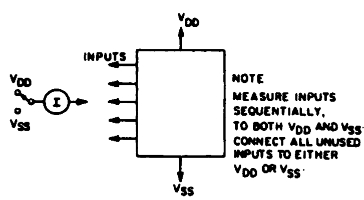
X = Don't Care Logic 1 ≡ High Logic 0 ≡ Low



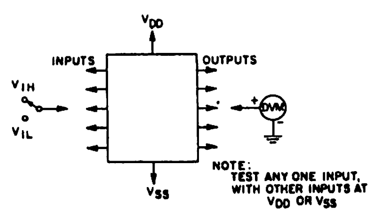
4532 logic diagram.



Quiescent device current test circuit.



Input current test circuit.



Input voltage test circuit.

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS[1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[2] Min.	T_{LOW}[2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH}[2] Min.	T_{HIGH}[2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN} = V_{SS}$ or V_{DD}	—	5	—	0.05	5	—	150	μAdc
		10	All Valid input	—	10	—	0.1	10	—	300	
		15	combinations	—	20	—	0.2	20	—	600	

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications"
[2] T_{LOW} = −55°C for C, D, F, H device.
= −40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device
= + 85°C for E device.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; C_L = 50 pF.

CHARACTERISTIC	TEST CONDITONS V_{DD} VOLTS	LIMITS ALL TYPES TYP.	LIMITS ALL TYPES MAX.	UNITS
PROPAGATION DELAY TIME t_{PHL}, t_{PLH} E_I to E_O, E_I to GS	5	110	220	ns
	10	55	110	
	15	45	85	
E_I to Qm, Dn to Gs	5	170	340	
	10	85	170	
	15	65	125	
Dn to QM	5	220	440	
	10	110	220	
	15	85	160	
TRANSITION TIME t_{THL}, t_{TLH}	5	100	200	ns
	10	50	100	
	15	40	80	
INPUT CAPACITANCE C_{IN}	Any Input	5	75	pF

AC TEST WAVEFORMS

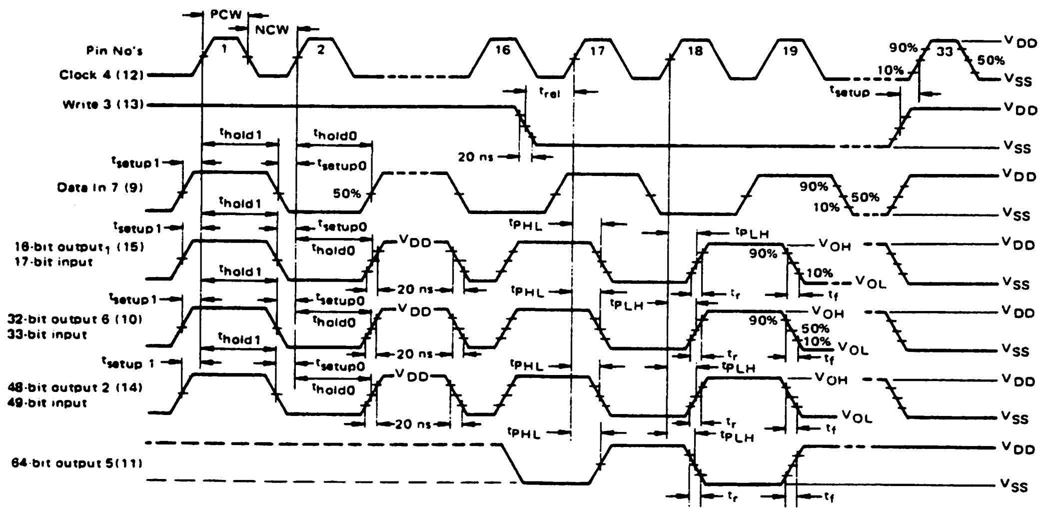
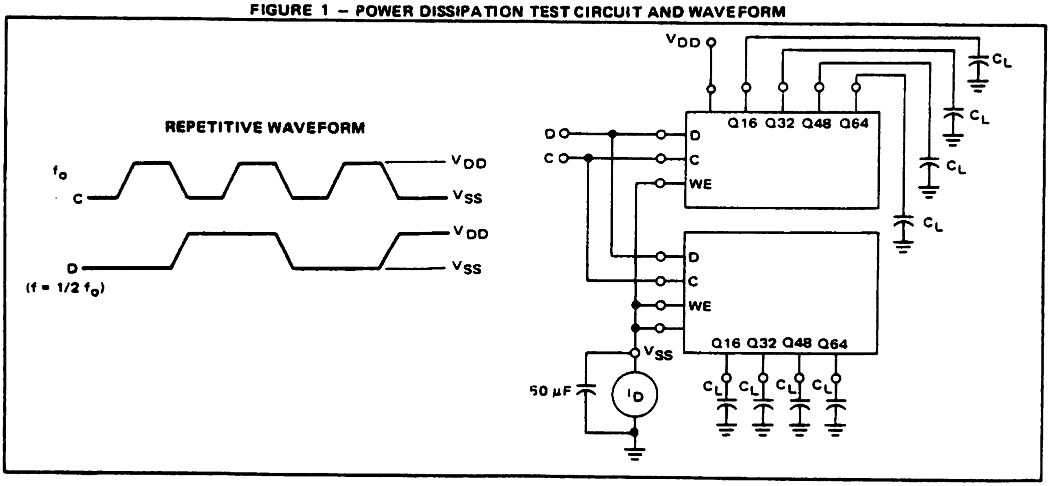
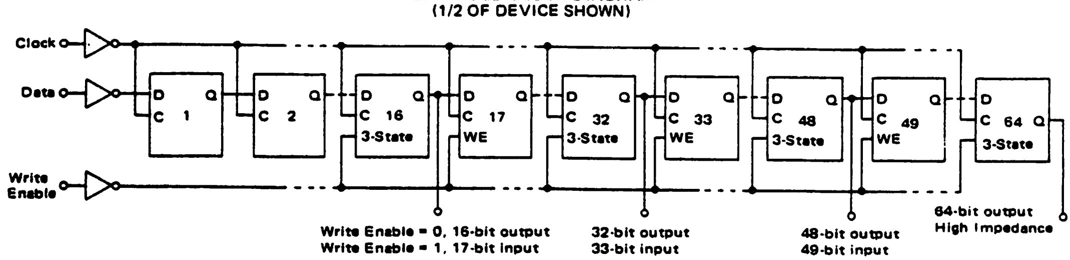


FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



EXPANDED BLOCK DIAGRAM
(1/2 OF DEVICE SHOWN)



SOLID STATE SCIENTIFIC

SCL4543B

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER

FEATURES

- **Phase Input Signal Reproduced on Outputs for Liquid Crystal Display**
- **Latched Storage of Input Code**
- **Blanking Input for Display Intensity Modulation**
- **Readout Blanking for Illegal Input Combinations**
- **Pin Compatible with CD4056A (with Pin 7 Tied to V_{SS})**

DESCRIPTION

The 4543B BCD-to-7 Segment Latch/Decoder/Driver is designed for use with liquid crystal readouts and is constructed with complementary MOS (CMOS) enhancement-mode devices. The circuit provides the functions of a 4-bit storage latch and a 8421 BCD-to-seven segment decoder and driver. The device has the capability to invert the logic levels of the output combinations. The Phase (Ph), Blanking (BI), and Latch Disable (LD) inputs are used to reverse the truth-table phase, blank the display, and store a BCD code, respectively. For liquid crystal readouts, a square wave is applied to the Ph input of the circuit and the electrically common backplane of the display. The outputs of the circuit are connected directly to the segments of the readout. For other types of readouts, such as light-emitting diode (LED), incandescent, gas discharge, and fluorescent readouts, connection diagrams are given on this data sheet.

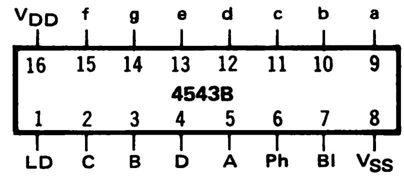
Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

TRUTH TABLE

INPUTS							OUTPUTS							
LD	BI	Ph*	D	C	B	A	a	b	c	d	e	f	g	Display
X	1	0	X	X	X	X	0	0	0	0	0	0	0	Blank
1	0	0	0	0	0	0	1	1	1	1	1	1	0	0
1	0	0	0	0	0	1	0	1	1	0	0	0	0	1
1	0	0	0	0	1	0	1	1	0	1	1	0	1	2
1	0	0	0	0	1	1	1	1	1	1	0	0	1	3
1	0	0	0	1	0	0	0	1	1	0	0	1	1	4
1	0	0	0	1	0	1	1	0	1	1	0	1	1	5
1	0	0	0	1	1	0	1	0	1	1	1	1	1	6
1	0	0	0	1	1	1	1	1	1	0	0	0	0	7
1	0	0	1	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	0	0	1	1	1	1	1	0	1	1	9
1	0	0	1	0	1	0	0	0	0	0	0	0	0	Blank
1	0	0	1	0	1	1	0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	0	0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	1	0	0	0	0	0	0	0	Blank
1	0	0	1	1	1	0	0	0	0	0	0	0	0	Blank
1	0	0	1	1	1	1	0	0	0	0	0	0	0	Blank
0	0	0	X	X	X	X	**							**
†	†	1	†				Inverse of Output Combinations Above							Display as above

X = Don't care
† = Above Combinations
* = For liquid crystal readouts, apply a square wave to Ph
For common cathode LED readouts, select Ph = 0.
For common anode LED readouts, select Ph = 1.
** = Depends upon the BCD code previously applied when LD = 1.

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

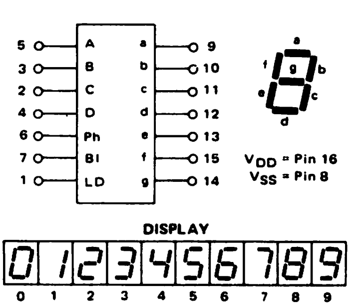
C	16-pin Cerdip
D	16-pin Ceramic
E	16-pin Epoxy
F	16-pin Flat
H	Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

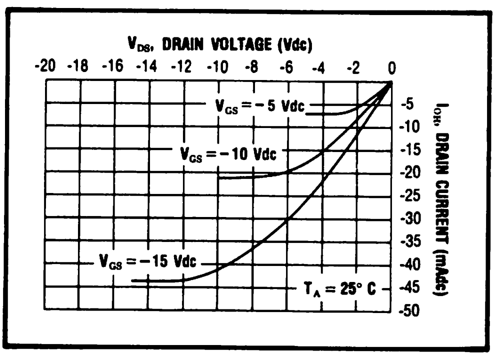
STATIC CHARACTERISTICS[1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[2] Min.	T_{LOW}[2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH}[2] Min.	T_{HIGH}[2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN}=V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	µAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		15	combinations	–	20	–	0.2	20	–	600	

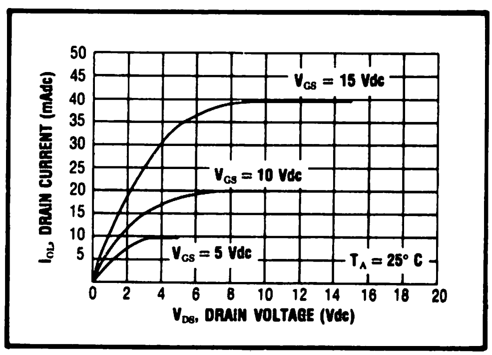
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}	5	–	550	1100	ns
		10	–	210	420	
		15	–	160	320	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
MINIMUM DATA INPUT SETUP TIME	t_{setup}	5	–	-40	0	ns
		10	–	-15	0	
		15	–	-10	0	
MINIMUM DATA INPUT HOLD TIME	t_{hold}	5	–	40	80	ns
		10	–	15	30	
		15	–	10	20	
MINIMUM LD PULSE WIDTH	PW_{LD}	5	–	125	250	ns
		10	–	50	100	
		15	–	40	80	

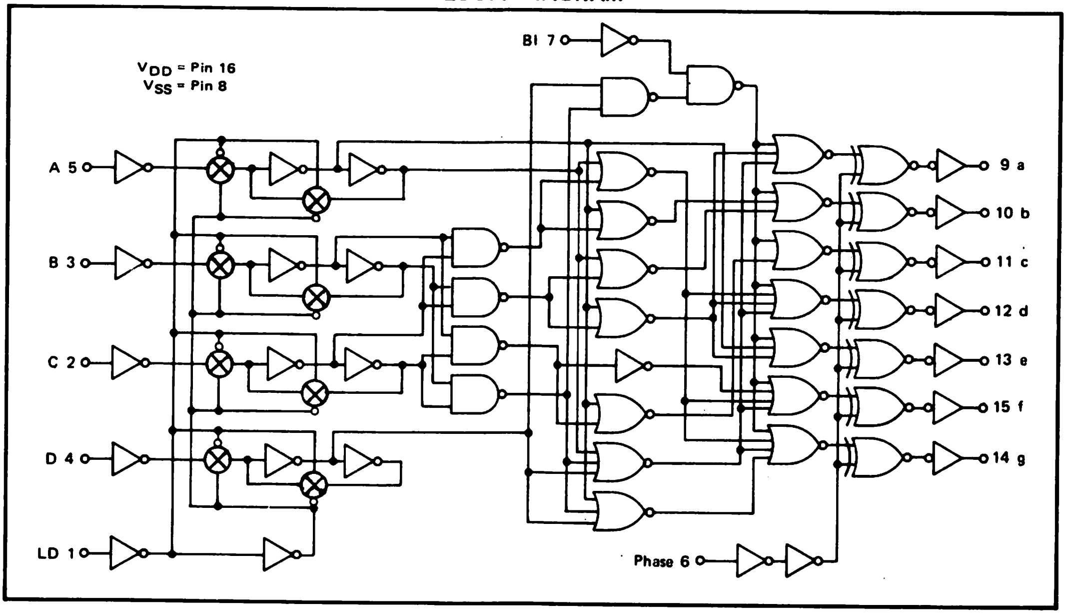


Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

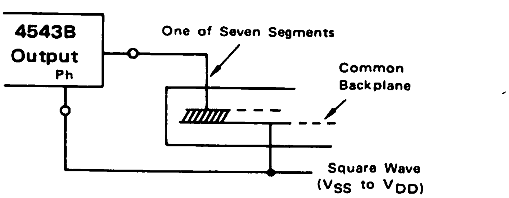
LOGIC DIAGRAM



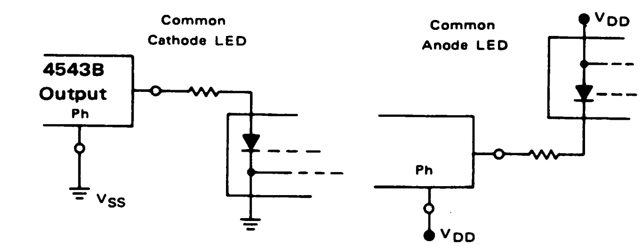
APPLICATIONS INFORMATION

CONNECTIONS TO VARIOUS DISPLAY READOUTS

LIQUID CRYSTAL (LC) READOUT

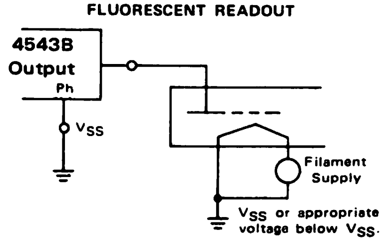


LIGHT EMITTING DIODE (LED) READOUT

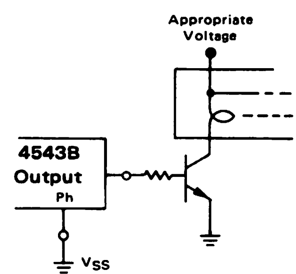


Note: Bipolar transistors may be added for gain (for $V_{DD} \leqslant 10V$ or $I_{out} \geqslant 10$ mA).

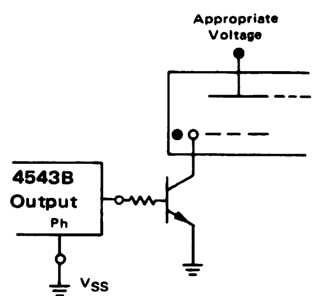
FLUORESCENT READOUT



INCANDESCENT READOUT



GAS DISCHARGE READOUT



SOLID STATE SCIENTIFIC

SCL4555B
SCL4556B

CMOS DUAL 2-TO-4 LINE DECODERS

FEATURES

- **Buffered Outputs**
- **Selected Output Active High (4555B) or Active Low (4556B)**
- **Expandable**

DESCRIPTION

The 4555B and 4556B are constructed with complementary MOS (CMOS) enhancement-mode devices. Each decoder/demultiplexer has two Select inputs (A and B), an active-low Enable input (E), and four mutually-exclusive outputs (Q0, Q1, Q2, Q3). The 4555B has the selected output go to the "high" state, and the 4556B has the selected output go to the "low" state. Expanded decoding such as binary-to-hexadecimal (1-of-16), etc., can be achieved by using other 4555B or 4556B devices.

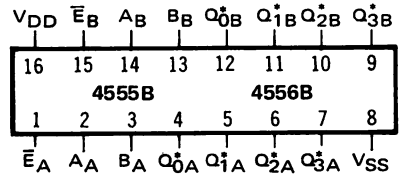
Applications include code conversion, address decoding, memory selection control, and demultiplexing (using the Enable input as a data input) in digital data transmission systems.

TRUTH TABLE

Inputs			Outputs 4555B				Outputs 4556B			
Enable	Select									
$\bar{E}$	B	A	Q3	Q2	Q1	Q0	$\bar{Q}3$	$\bar{Q}2$	$\bar{Q}1$	$\bar{Q}0$
0	0	0	0	0	0	1	1	1	1	0
0	0	1	0	0	1	0	1	1	0	1
0	1	0	0	1	0	0	1	0	1	1
0	1	1	1	0	0	0	0	1	1	1
1	X	X	0	0	0	0	1	1	1	1

X = Don't Care

CONNECTION DIAGRAM
(all packages)



*Inverted for 4556B

Add suffix for package:

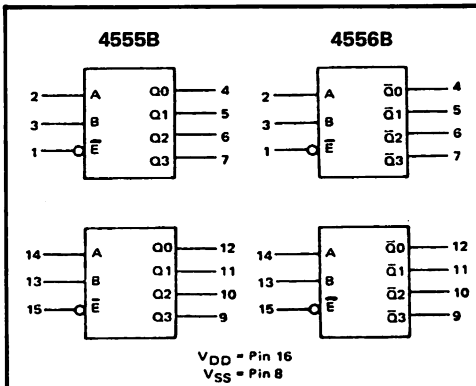
- C 16-pin Cerdip
- D 16-pin Ceramic
- E 16-pin Epoxy
- F 16-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

BLOCK DIAGRAMS



ELECTRICAL CHARACTERISTICS

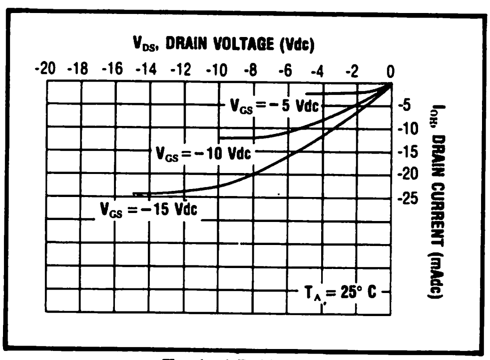
STATIC CHARACTERISTICS[1]

PARAMETER		VDD (Vdc)	CONDITIONS	TLOW[2] Min.	TLOW[2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	THIGH[2] Min.	THIGH[2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5 10 15	$V_{IN} = V_{SS}$ or V_{DD} All valid inputs combinations	– – –	5 10 20	– – –	0.05 0.1 0.2	5 10 20	– – –	150 300 600	μAdc

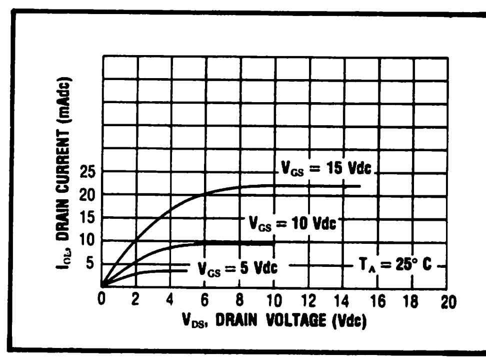
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = −55°C for C, D, F, H device.
= −40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		VDD (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME 4555B	t_{PLH}, t_{PHL}	5 10 15	– – –	140 65 50	280 130 100	ns
4556B	t_{PLH}, t_{PHL}	5 10 15	– – –	160 75 50	320 150 100	ns
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5 10 15	– – –	100 50 40	200 100 80	ns

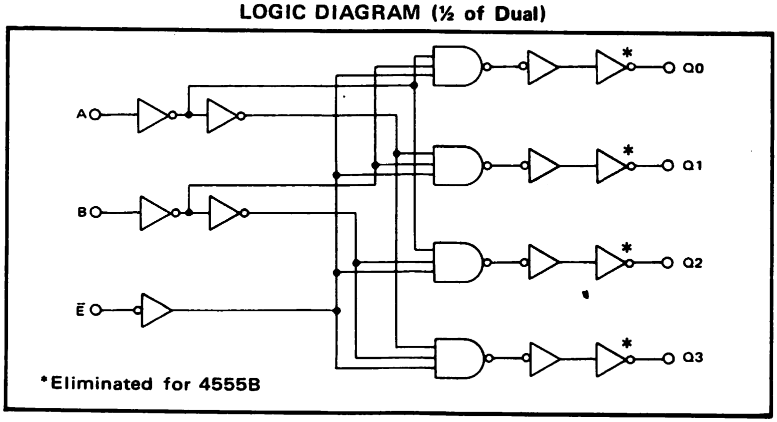


Typical P-Channel
Source Current Characteristics

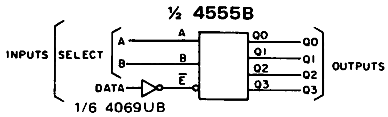


Typical N-Channel
Sink Current Characteristics

LOGIC DIAGRAM (½ of Dual)



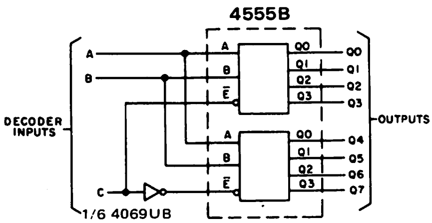
APPLICATIONS INFORMATION



TRUTH TABLE

SELECT INPUTS		OUTPUTS			
B	A	Q0	Q1	Q2	Q3
0	0	DATA	0	0	0
0	1	0	DATA	0	0
1	0	0	0	DATA	0
1	1	0	0	0	DATA

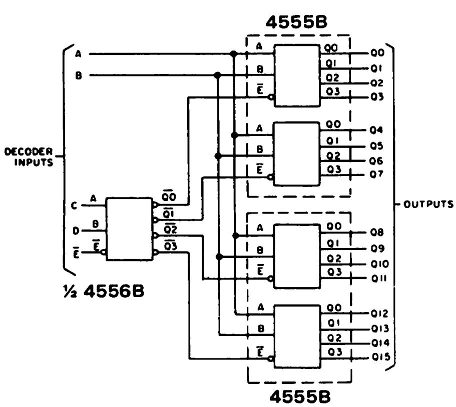
1-of-4 Line Data Demultiplexer Using 4555B



TRUTH TABLE

INPUTS			Q OUTPUTS							
C	B	A	0	1	2	3	4	5	6	7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

1-of-8 Decoder Using 4555B



TRUTH TABLE

INPUTS					Q OUTPUTS															
$\bar{E}$	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	1	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
1	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

X = don't care

1-of-16 Decoder Using 4555B/ 4556B

CMOS 4-BIT ARITHMETIC LOGIC UNIT

FEATURES

- Function and Pinout Equivalent to 74181
- Provides 16 Logic Functions and 16 Arithmetic Functions
- Comparator Function
- Positive or Negative Logic
- Full Look-Ahead for High-Speed Operations on Long Words

DESCRIPTION

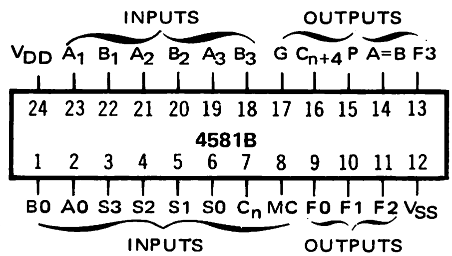
The 4581B is a CMOS 4-Bit Arithmetic Logic Unit (ALU) capable of providing 16 functions of two Boolean variables and 16 binary arithmetic operations on two 4-bit words. The level of the Mode Control input determines whether the output function is logic or arithmetic. The desired logic function is selected by applying the appropriate binary word to the Select inputs (S0 thru S3) with the Mode Control input high, while the desired arithmetic operation is selected by applying a low voltage to the Mode Control input, the required level to Carry in, and the appropriate word to the Select inputs. The Word inputs and Function outputs can be operated with either active-high or active-low data.

Carry propagate (P) and Carry generate (G) outputs are provided to allow a full look-ahead carry scheme for fast simultaneous carry generation for the four bits in the package. Fast arithmetic operations on long words are obtainable by using the 4582B as a second-order look-ahead block. An inverted Ripple-Carry input (C_n) and a Ripple-Carry output (C_{n+4}) are included for ripple-through operation.

ALU SIGNAL DESIGNATIONS

Designation	Pin Nos.	Function
A3, A2, A1, A0	19, 21, 23, 2	Word A Inputs
B3, B2, B1, B0	18, 20, 22, 1	Word B Inputs
S3, S2, S1, S0	3, 4 5, 6	Function-Select Inputs
C_n	7	Inv. Carry Input
MC	8	Mode Control Input
F3, F2, F1, F0	13, 11, 10, 9	Function Outputs
A = B	14	Comparator Output
P	15	Carry Propagate Output
C_{n+4}	16	Inv. Carry Output
G	17	Carry Generate Output

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

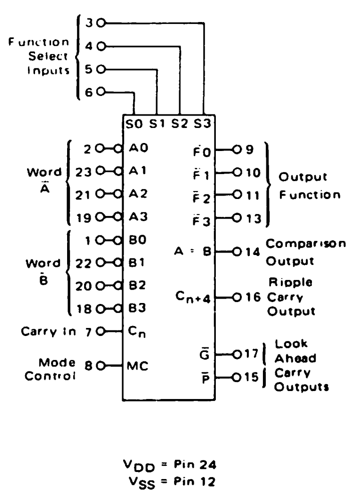
- D 24-pin Ceramic
- E 24-pin Epoxy
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
D, H Device		-55 to +125	°C
E Device		-40 to +85	°C

BLOCK DIAGRAM



ALU FUNCTION GENERATION

The 4581B can be used with the signal designations of either Figure 1 or Figure 2.

The logic functions and arithmetic operations obtained with signal designations as in Figure 1 are given in Table 1; those obtained with the signal designations of Figure 2 are given in Table 2.

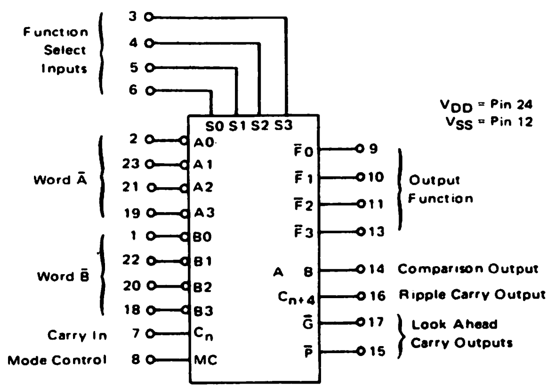


FIGURE 1
(Use with Table 1 for Positive logic, with Table 2 for negative logic)

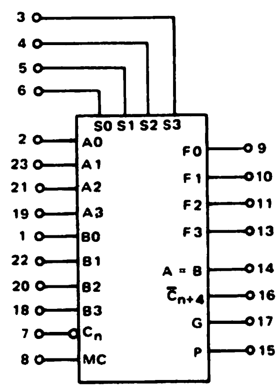


FIGURE 2
(Use with Table 2 for positive logic, with Table 1 for negative logic)

TABLE 1

SELECTION				ACTIVE-LOW DATA		
				MC = H	MC = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	C_n = L (no carry)	C_n = H (with carry)
L	L	L	L	$F = \overline{A}$	F = A MINUS 1	F = A
L	L	L	H	$F = \overline{AB}$	F = AB MINUS 1	F = AB
L	L	H	L	$F = \overline{A} + B$	$F = A\overline{B}$ MINUS 1	$F = A\overline{B}$
L	L	H	H	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	$F = \overline{A + B}$	$F = A$ PLUS $(A + \overline{B})$	$F = A$ PLUS $(A + \overline{B})$ PLUS 1
L	H	L	H	$F = \overline{B}$	$F = AB$ PLUS $(A + \overline{B})$	$F = AB$ PLUS $(A + \overline{B})$ PLUS 1
L	H	H	L	$F = \overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	$F = A + \overline{B}$	$F = A + \overline{B}$	$F = (A + \overline{B})$ PLUS 1
H	L	L	L	$F = \overline{A}B$	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H	L	L	H	$F = A \oplus B$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	$F = A\overline{B}$ PLUS (A + B)	$F = A\overline{B}$ PLUS (A + B) PLUS 1
H	L	H	H	F = A + B	F = (A + B)	F = (A + B) PLUS 1
H	H	L	L	F = 0	F = A PLUS A*	F = A PLUS A PLUS 1
H	H	L	H	$F = A\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H	H	H	L	F = AB	$F = A\overline{B}$ PLUS A	$F = A\overline{B}$ PLUS A PLUS 1
H	H	H	H	F = A	F = A	F = A PLUS 1

* Each bit is shifted to the next more significant position.

TABLE 2

SELECTION				ACTIVE-HIGH DATA		
				MC = H	MC = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	$\overline{C}_n$ = H (no carry)	$\overline{C}_n$ = L (with carry)
L	L	L	L	$F = \overline{A}$	F = A	F = A PLUS 1
L	L	L	H	$F = \overline{A + B}$	F = A + B	F = (A + B) PLUS 1
L	L	H	L	$F = \overline{A}B$	$F = A + \overline{B}$	$F = (A + \overline{B})$ PLUS 1
L	L	H	H	F = 0	F = MINUS 1 (2's COMPL)	F = ZERO
L	H	L	L	$F = \overline{AB}$	$F = A$ PLUS $A\overline{B}$	$F = A$ PLUS $A\overline{B}$ PLUS 1
L	H	L	H	$F = \overline{B}$	$F = (A + B)$ PLUS $A\overline{B}$	$F = (A + B)$ PLUS $A\overline{B}$ PLUS 1
L	H	H	L	$F = A \oplus B$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	$F = A\overline{B}$	$F = A\overline{B}$ MINUS 1	$F = A\overline{B}$
H	L	L	L	$F = \overline{A} + B$	F = A PLUS AB	F = A PLUS AB PLUS 1
H	L	L	H	$F = \overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	$F = (A + \overline{B})$ PLUS AB	$F = (A + \overline{B})$ PLUS AB PLUS 1
H	L	H	H	F = AB	F = AB MINUS 1	F = AB
H	H	L	L	F = 1	F = A PLUS A*	F = A PLUS A PLUS 1
H	H	L	H	$F = A + \overline{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H	H	H	L	F = A + B	$F = (A + \overline{B})$ PLUS A	$F = (A + \overline{B})$ PLUS A PLUS 1
H	H	H	H	F = A	F = A MINUS 1	F = A

When the device is in the subtract mode (LHHL), comparison of two 4-bit words present at the A and B inputs is provided using the A=B output. It assumes a high-level state when indicating equality. Also, when the ALU is in the subtract mode the C_{n+4} output can be used to indicate relative magnitude as shown in this table:

Data Level	C_n	C_{n+4}	Magnitude
Active High	H	H	A ≤ B
	L	H	A < B
	H	L	A > B
	L	L	A ≥ B
Active Low	L	L	A ≤ B
	H	L	A < B
	L	H	A > B
	H	H	A ≥ B

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS[1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[2] Min.	T_{LOW}[2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH}[2] Min.	T_{HIGH}[2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5 10 15	$V_{IN} = V_{SS}$ or V_{DD} All valid input combinations	– – –	5 10 20	– – –	0.05 0.1 0.2	5 10 20	– – –	150 300 600	μAdc

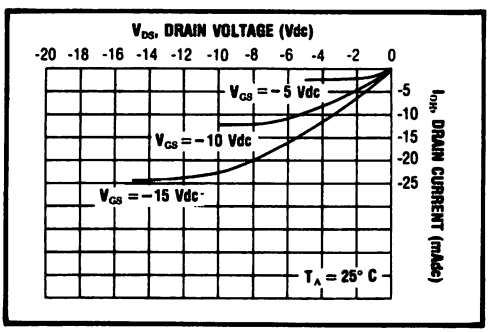
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for D, H device.
= -40°C for E device.
T_{HIGH} = +125°C for D, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

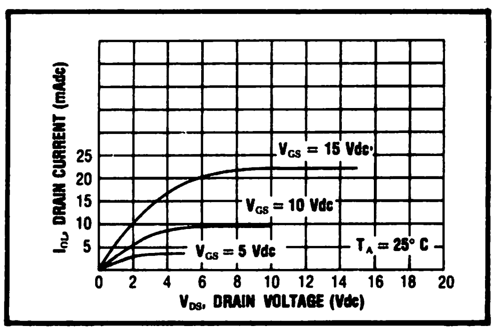
PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME Sum In to Sum Out	t_{PLH}, t_{PHL}	5 10 15	– – –	400 160 120	800 320 240	ns
Sum In to Sum Out (Logic Mode)		5 10 15	– – –	380 190 160	760 380 320	ns
Sum In to A = B		5 10 15	– – –	450 275 225	900 550 450	ns
Sum In to $\bar{P}$ or $\bar{G}$		5 10 15	– – –	300 150 125	600 300 250	ns
Sum In to C_{n+4}		5 10 15	– – –	300 150 125	600 300 250	ns
Carry In to Sum Out		5 10 15	– – –	200 100 70	400 50 35	ns
Carry In to C_{n+4}		5 10 15	– – –	200 100 70	400 50 35	ns
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5 10 15	– – –	100 50 40	200 100 80	ns

AC Test Setup Reference Table

TEST	AC PATHS INPUTS	AC PATHS OUTPUTS	DC DATA INPUTS TO V_{SS}	DC DATA INPUTS TO V_{DD}	MODE
Sum_{in} to Sum_{out} Delay Time	$\bar{A}0$	Any $\bar{F}$	Remaining A's C_n	All $\bar{B}$'s	Add
Sum_{in} to $\bar{P}$ Delay Time	$\bar{A}0$	P	Remaining $\bar{A}$'s C_n	All B's	Add
Sum_{in} to $\bar{G}$ Delay Time	$\bar{B}0$	C_{n+y}	All $\bar{A}$'s C_n	Remaining $\bar{B}$'s	Add
Sum_{in} to C_{n+4} Delay Time	$\bar{B}0$	$\bar{G}$	All $\bar{A}$'s C_n	Remaining $\bar{B}$'s	Add
C_n to Sum_{out} Delay Time	C_n	Any $\bar{F}$	All $\bar{A}$'s	All $\bar{B}$'s	Add
C_n to C_{n+4} Delay Time	C_n	C_{n+4}	All A's	All $\bar{B}$'s	Add
Sum_{in} to A = B Delay Time	A0	A = B	All $\bar{B}$'s Remaining A's	C_n	Sub
Sum_{in} to Sum_{out} Delay Time (Logic Mode)	All $\bar{B}$'s	Any $\bar{F}$	All A's	M	Exclusive OR



Typical P-Channel
Source Current Characteristics



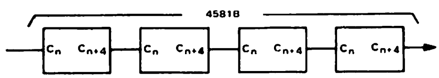
Typical N-Channel
Sink Current Characteristics

APPLICATIONS INFORMATION

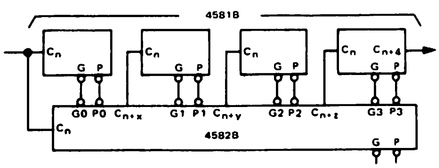
ADDITION REQUIREMENTS

Number of Bits	Package Count: Arithmetic/ Logic Units	Package Count: Look-Ahead Carry Generators	Carry Method Between ALU's
1 to 4	1		None
5 to 8	2		Ripple
9 to 16	3 or 4	1	Full Look-Ahead
17 to 64	5 to 16	2 to 5	Full Look-Ahead

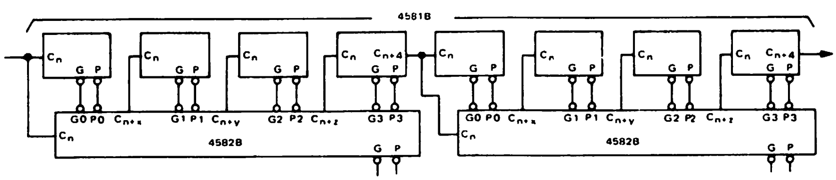
EXPANSION TECHNIQUES



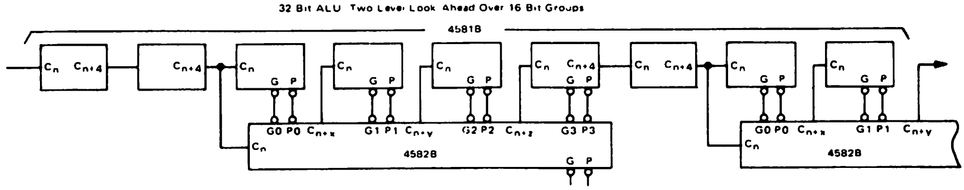
16 Bit ALU, Ripple Carry



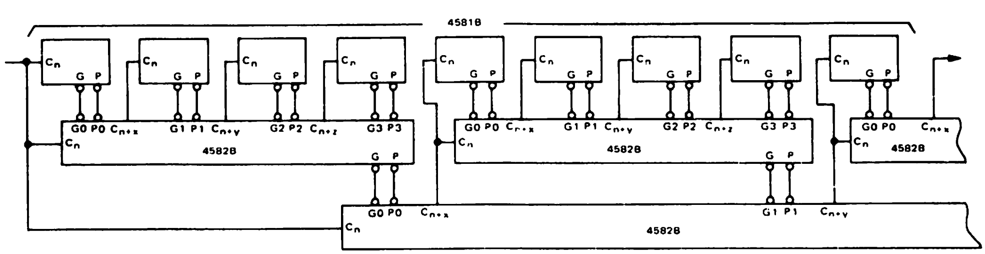
16 Bit ALU, Two Level Look Ahead



32 Bit ALU Two Level Look Ahead Over 16 Bit Groups



Combined two level look ahead and ripple carry ALU



64 Bit ALU Full Carry Look Ahead in Three Levels

A and B Inputs and F Outputs are not shown (4581B).

CMOS LOOK-AHEAD CARRY BLOCK

FEATURES

- Expandable to any Number of Bits
- High-Speed Operation
- Directly Compatible with 4581B ALU

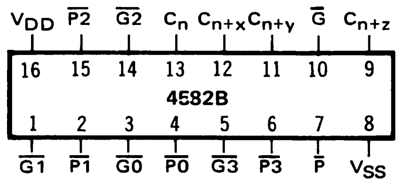
DESCRIPTION

The 4582B is a high-speed, Look-Ahead Carry Generator capable of anticipating a carry across four binary adders or group of adders. It is cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided.

When used in conjunction with the 4581B Arithmetic Logic Unit (ALU), these generators provide high-speed carry look-ahead capability for any word length. Each 4582B generates the look-ahead (anticipated carry) across a group of four ALU's and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits.

Carry input and output of the 4581B ALU are in their true form and the carry propagate (P) and carry generate (G) are in negated form; therefore, the carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connections to the ALU. Reinterpretations of carry functions as explained on the 4581B data sheet are also applicable to and compatible with the look-ahead generator.

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

C	16-pin Cerdip
D	16-pin Ceramic
E	16-pin Epoxy
F	16-pin Flat
H	Chip

RECOMMENDED OPERATING CONDITIONS

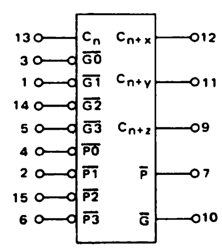
For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

PIN DESIGNATIONS

DESIGNATION	PIN NO's	FUNCTION
$\overline{G0}, \overline{G1}, \overline{G2}, \overline{G3}$	3,1,14,5	Active-Low Carry-Generate Inputs
$\overline{P0}, \overline{P1}, \overline{P2}, \overline{P3}$	4,2,15,6	Active-Low Carry-Propagate Inputs
C_n	13	Carry Input
C_{n+x}, C_{n+y}, C_{n+z}	12,11,9	Carry Outputs
$\overline{G}$	10	Active-Low Group Carry-Generate Output
$\overline{P}$	7	Active-Low Group Carry-Propagate Output

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

LOGIC EQUATIONS

$C_{n+x} = G0 + P0 \bullet C_n$
$C_{n+y} = G1 + P1 \bullet G0 + P1 \bullet P0 \bullet C_n$
$C_{n+z} = G2 + P2 \bullet G1 + P2 \bullet P1 \bullet G0 + P2 \bullet P1 \bullet P0 \bullet C_n$
$\overline{G} = G3 + P3 \bullet G2 + P3 \bullet P2 \bullet G1 + P3 \bullet P2 \bullet P1 \bullet G0$
$\overline{P} = P3 \bullet P2 \bullet P1 \bullet P0$

ELECTRICAL CHARACTERISTICS

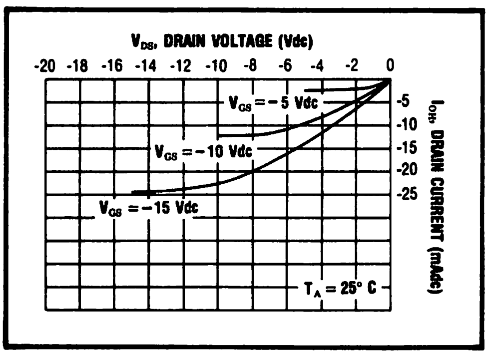
STATIC CHARACTERISTICS[1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[2] Min.	T_{LOW}[2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH}[2] Min.	T_{HIGH}[2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN}=V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	µAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		15	combinations	–	20	–	0.2	20	–	600	

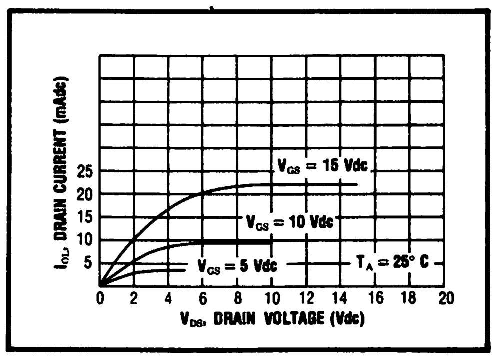
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}	5	–	200	400	ns
		10	–	100	200	
		15	–	85	160	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	

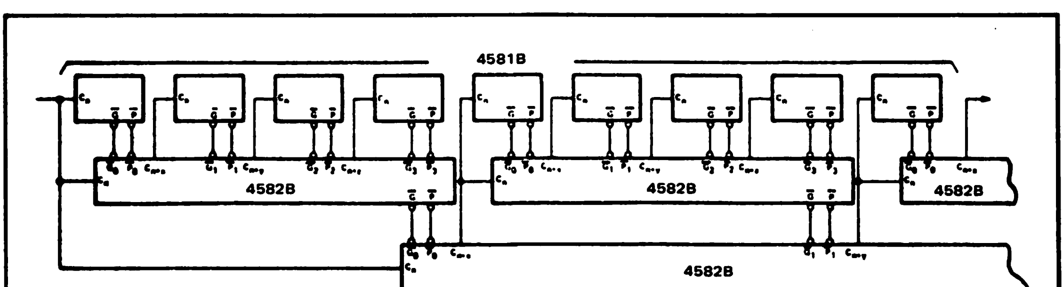


Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

APPLICATIONS INFORMATION



64-BIT ALU, FULL-CARRY LOOK-AHEAD IN THREE LEVELS

SOLID STATE SCIENTIFIC

SCL4584B

CMOS HEX INVERTING SCHMITT TRIGGER

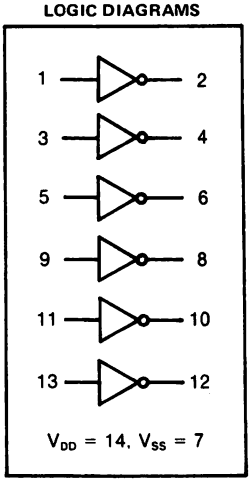
FEATURES:

- **Schmitt Trigger Action on each Input with no External Components**
- **Noise Immunity Greater than 30%**
- **No Limit on Input Rise and Fall Times**
- **Pin for Pin Replacement for CD40106B, MM74C14 and MCI4584B**
- **Also Pin Compatible with 74C04 and 4069 Hex Inverters**

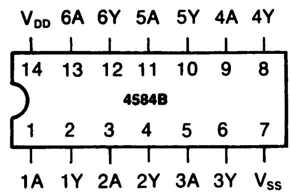
DESCRIPTION:

The 4584B consists of six Schmitt Trigger circuits, constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These devices find primary use where low power dissipation and/or high noise immunity is desired. The 4584B may be used in place of the MCI4069B hex inverter for enhanced noise immunity or to square up slowly changing waveforms.

LOGIC DIAGRAMS



CONNECTION DIAGRAM
(all packages)



Add suffix for package:

C 14-pin Cerdip
D 14-pin Ceramic
E 14-pin Epoxy
F 14-pin Flat
H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	V_{DD} - V_{SS}	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		−55 to +125	°C
E Device		−40 to +85	°C

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS[1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[2] Min.	T_{LOW}[2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH}[2] Min.	T_{HIGH}[2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5 10 15	$V_{IN} = V_{SS}$ or V_{DD} All valid input combinations	— — —	1.0 2.0 4.0	— — —	.005 .01 .02	1.0 2.0 4.0	— — —	30 60 120	μA
POSITIVE TRIGGER THRESHOLD VOLTAGE	V_{TP}	5 10 15		2.3 4.5 6.8	3.5 7.0 11.0	2.3 4.5 6.8	2.9 5.3 7.7	3.5 7.0 11.0	2.3 4.5 6.8	3.5 7.0 11.0	V
NEGATIVE TRIGGER THRESHOLD VOLTAGE	V_{TN}	5 10 15		1.5 3.0 4.0	2.7 5.5 8.2	1.5 3.0 4.0	2.15 4.4 6.5	2.7 5.5 8.2	1.5 3.0 4.0	2.7 5.5 8.2	V
HYSTERESIS VOLTAGE	V_H	5 10 15		.4 .7 .85	2.0 3.0 4.0	.4 .7 .85	.75 .95 1.2	2.0 3.0 4.0	.4 .7 .85	2.0 3.0 4.0	V

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = −55°C for C, D, F, H devices.
= −40°C for E Devices.
T_{HIGH} = +125°C for E, D, F, H devices.
= +85°C for E devices.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t_{PLH} t_{PHL}	5 10 15	86 42 30	107 48 35	150 60 40	ns
OUTPUT TRANSITION TIME	t_{TLH} t_{THL}	5 10 15	44 24 19	62 29 23	200 100 80	ns

CMOS 4-BIT MAGNITUDE COMPARATOR

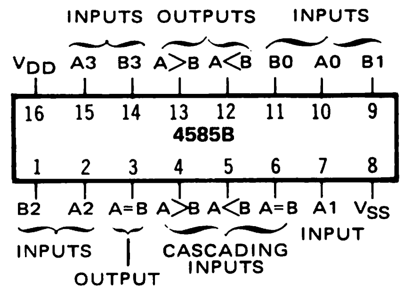
FEATURES

- Binary or BCD Comparison
- Expandable
- A<B, A=B, A>B Outputs Available

DESCRIPTION

This 4-Bit Magnitude Comparator performs comparison of straight binary and straight BCD (8-4-2-1) codes. Three decisions about two 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The A<B and A=B outputs of a stage handling less-significant bits are connected to the corresponding A<B and A=B inputs of the next stage handling more-significant bits. The A>B cascading input is connected to a high level. The stage handling the least-significant bits must have a high-level voltage applied to the A=B and A>B inputs. An alternate method of cascading which reduces the comparison time is shown under Applications Information.

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

C	16-pin Cerdip
D	16-pin Ceramic
E	16-pin Epoxy
F	16-pin Flat
H	Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

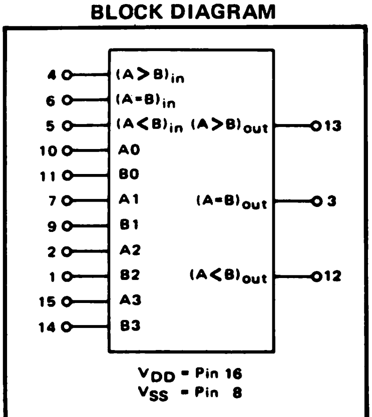
DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

TRUTH TABLE

Inputs							Outputs		
Comparing				Cascading					
A3, B3	A2, B2	A1, B1	A0, B0	A<B	A=B	A>B	A<B	A=B	A>B
A3>B3	X	X	X	X	X	1	0	0	1
A3=B3	A2>B2	X	X	X	X	1	0	0	1
A3=B3	A2=B2	A1>B1	X	X	X	1	0	0	1
A3=B3	A2=B2	A1=B1	A0>B0	X	X	1	0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	0	0	1	0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	0	1	X	0	1	0
A3=B3	A2=B2	A1=B1	A0=B0	1	0	X	1	0	0
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	1	0	0
A3=B3	A2=B2	A1<B1	X	X	X	X	1	0	0
A3=B3	A2<B2	X	X	X	X	X	1	0	0
A3<B3	X	X	X	X	X	X	1	0	0
X	X	X	X	X	X	0	—	—	0

X = Don't Care

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

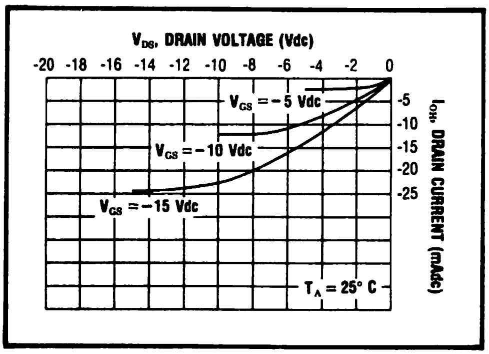
STATIC CHARACTERISTICS[1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[2]		+25°C			T_{HIGH}[2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN}=V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	μAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		15	combinations	–	20	–	0.2	20	–	600	

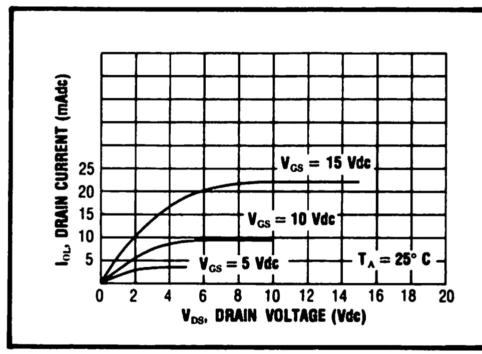
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}	5	–	300	600	ns
		10	–	125	250	
		15	–	80	160	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	

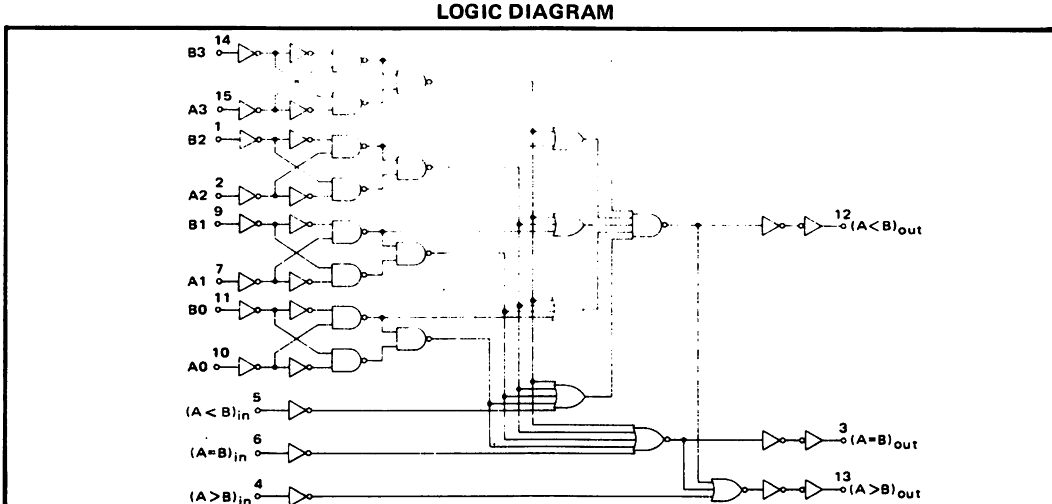


Typical P-Channel
Source Current Characteristics



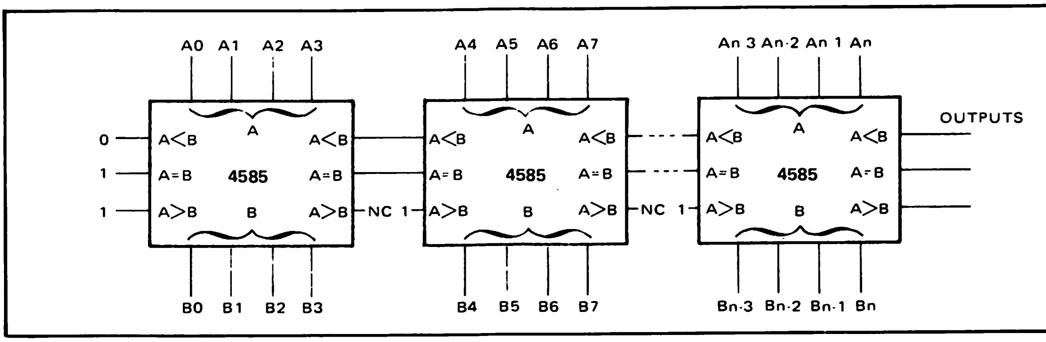
Typical N-Channel
Sink Current Characteristics

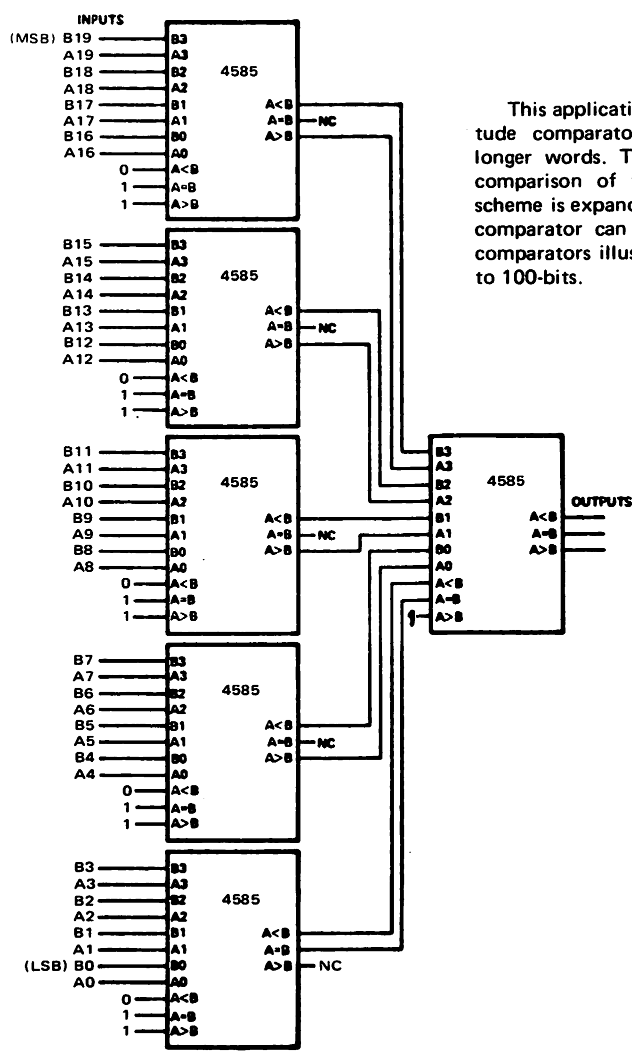
LOGIC DIAGRAM



APPLICATIONS INFORMATION

COMPARISON OF TWO N-BIT WORDS

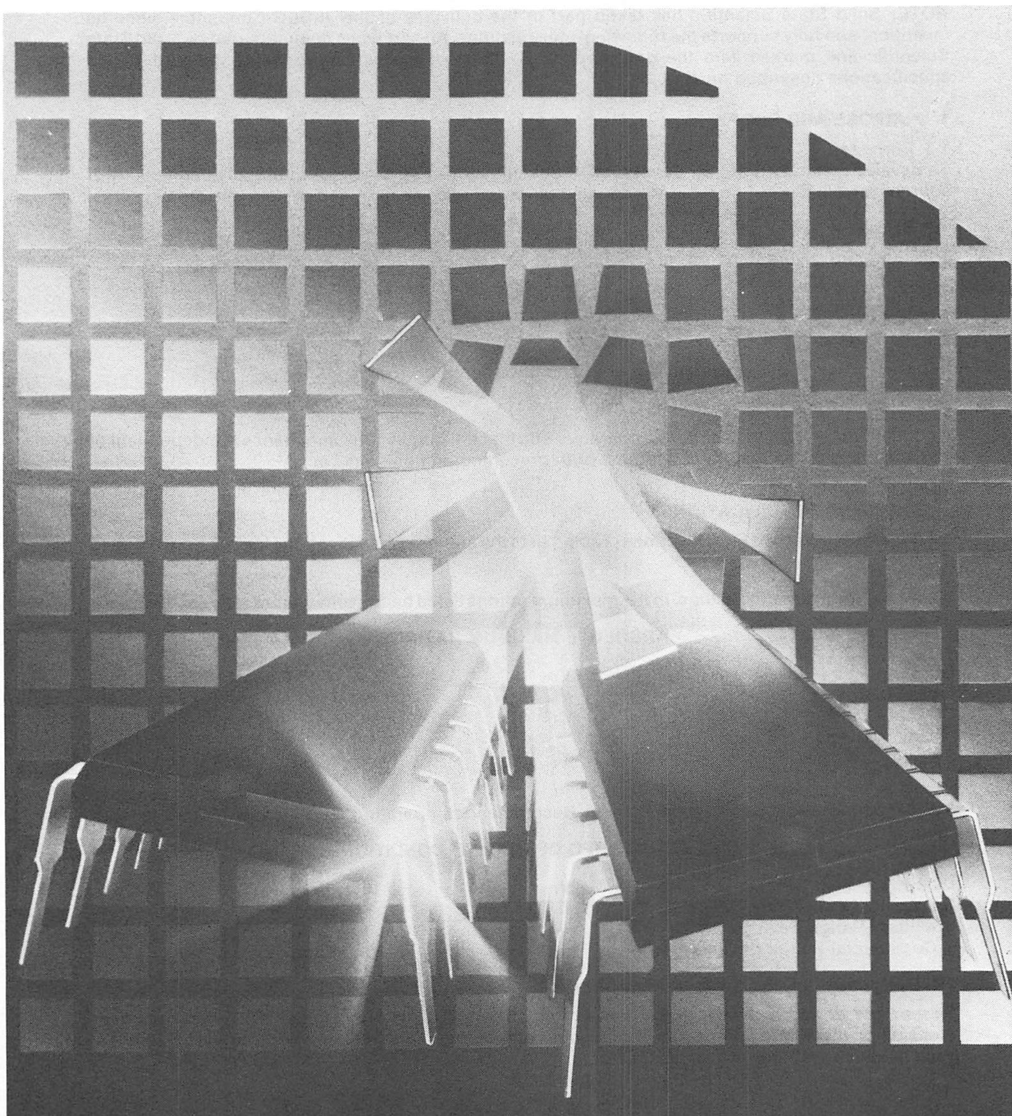




This application demonstrates how these magnitude comparators can be cascaded to compare longer words. The example illustrated shows the comparison of two 20-bit words; however, the scheme is expandable to n-bits. As an example, one comparator can be used with five of the 20-bit comparators illustrated to expand the word length to 100-bits.

WORD LENGTH	NUMBER OF PKGS
1-4 bits	1
5-20 bits	2-6
21-100 bits	8-31

JEDEC Standard Specifications



JEDEC STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES

MAY 1976

Formulated by JEDEC Solid State Products Council

NOTE: Solid State Scientific has taken part in the activities of the JEDEC Committee since its inception, and fully supports the following specifications. All part types manufactured by Solid State Scientific and marked with the designation "B" meet or exceed the industry standard CMOS specifications described herein.

1. PURPOSE AND SCOPE

1.1 Purpose

To develop a standard of "B" Series CMOS Specifications to provide for uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and system design by users.

1.2 Scope

This Standard covers standard specifications for description of "B" Series CMOS devices.

2. DEFINITIONS

2.1 "B" Series

"B" Series CMOS includes both buffered and unbuffered devices.

2.2 "Buffered"

A buffered output is one that has the characteristic that the output "on" impedance is independent of any and all valid input logic conditions, both preceding and present.

3. STANDARD SPECIFICATIONS

3.1 Listing of Standard Specifications. Table 1 lists the standard specifications for "B" Series CMOS devices.

3.2 Absolute Maximum Ratings. In the maximum ratings listed below voltages are referenced to V_{SS}.

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage	V_{DD}	−0.5 to + 18	Vdc
Input Voltage	V_{IN}	−0.5 to V_{DD}+ 0.5	Vdc
DC Input Current (any one input)	I_{IN}	±10	mAdc
Storage Temperature Range	T_S	−65 to + 150	°C

3.3 Recommended Operating Conditions. Recommended operating conditions are listed below.

RECOMMENDED OPERATING CONDITIONS

DC Supply Voltage	V_{DD}	+3 to + 15	Vdc
Operating Temperature Range	T_A		
Military-Range Devices		−55 to + 125	°C
Commercial-Range Devices		−40 to + 85	°C

3.4 Designation of "B" Series CMOS Devices

Those parts which have analog inputs and/or outputs shall be included in the "B" Series providing those parts' maximum ratings and logical input and output parameters conform to the "B" Series, such as (including, but not limited to):

4051B	4053B
4052B	4066B

Products that meet "B" Series specifications except that the logical outputs are not buffered and the V_{IL} and V_{IH} specifications are 20% and 80% of V_{DD}, respectively, shall be marked with the *UB* designation, such as (including, but not limited to):

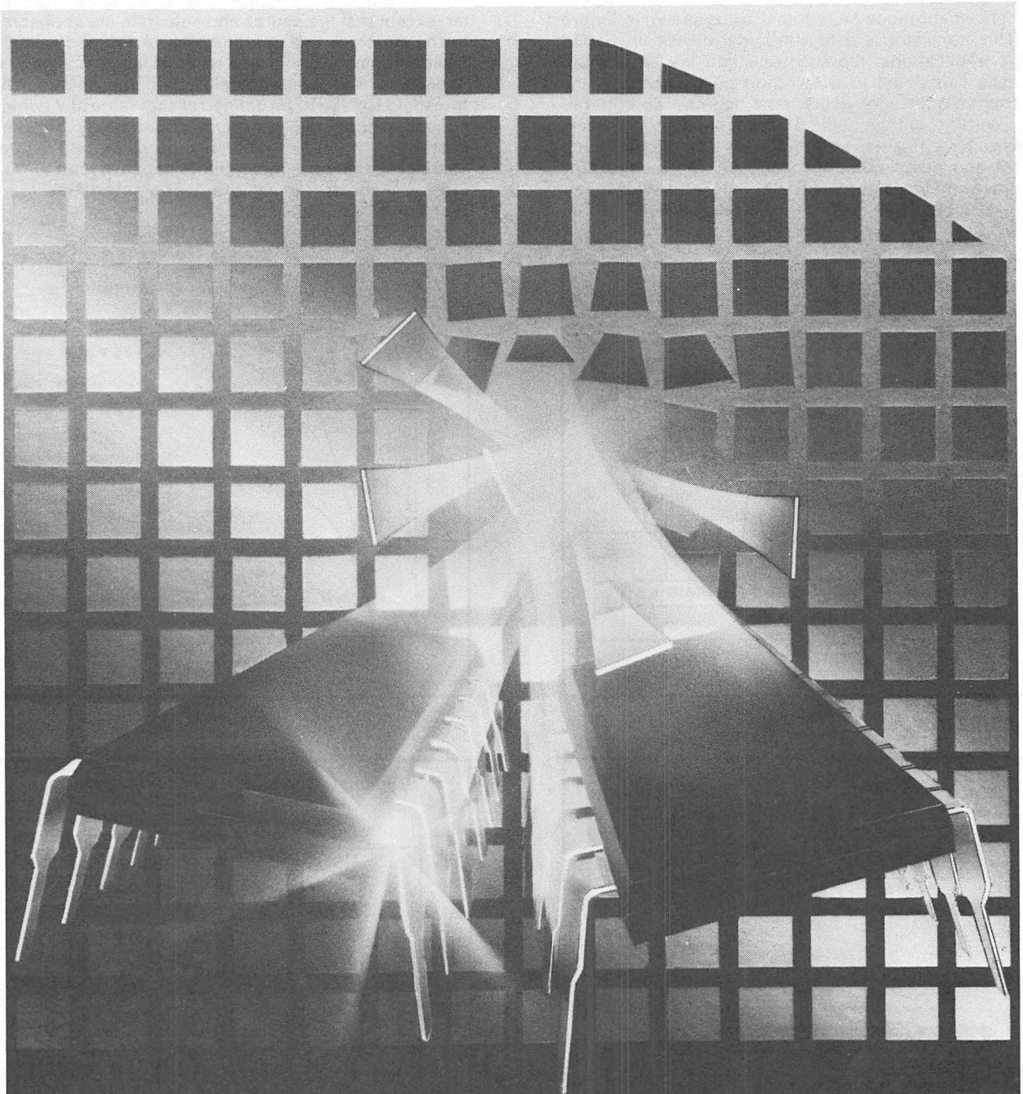
4000UB	4002UB	4011UB	4023UB	4041UB	4069UB
4001UB	4007UB	4012UB	4025UB	4049UB	

STATIC CHARACTERISTICS

	PARAMETER	TEMP. RANGE	V_{DD} (Vdc)	CONDITIONS	LIMITS T_{LOW}* Min.	LIMITS T_{LOW}* Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH}* Min.	T_{HIGH}* Max.	UNITS
I_{DD}	Quiescent Device Current GATES	Mil	5	$V_{IN}=V_{SS}$ or V_{DD}	–	0.25	–	–	0.25	–	7.5	µAdc
			10		–	0.5	–	–	0.5	–	15	
			15		–	1.0	–	–	1.0	–	30	
		Comm	5	All valid input combinations	–	1.0	–	–	1.0	–	7.5	µAdc
			10		–	2.0	–	–	2.0	–	15	
			15		–	4.0	–	–	4.0	–	30	
	BUFFERS, FLIP-FLOPS	Mil	5	$V_{IN}=V_{SS}$ or V_{DD}	–	1.0	–	–	1.0	–	30	µAdc
			10		–	2.0	–	–	2.0	–	60	
			15		–	4.0	–	–	4.0	–	120	
		Comm	5	All valid input combinations	–	4.0	–	–	4.0	–	30	µAdc
			10		–	8.0	–	–	8.0	–	60	
			15		–	16.0	–	–	16.0	–	120	
	MSI	Mil	5	$V_{IN}=V_{SS}$ or V_{DD}	–	5	–	–	5	–	150	µAdc
			10		–	10	–		10	–	300	
			15		–	20	–	–	20	–	600	
		Comm	5	All valid input combinations	–	20	–	–	20	–	150	µAdc
			10		–	40	–	–	40	–	300	
			15		–	80	–	–	80	–	600	
V_{OL}	Low-Level Output Voltage	All	5	$V_{IN}=V_{SS}$ or V_{DD} $\lvert I_O \rvert \leq 1\mu A$	–	0.05	–	–	0.05	–	0.05	Vdc
			10		–	0.05	–	–	0.05	–	0.05	
			15		–	0.05	–	–	0.05	–	0.05	
V_{OH}	High-Level Output Voltage	All	5	$V_{IN}=V_{SS}$ or V_{DD} $\lvert I_O \rvert \leq 1\mu A$	4.95	–	4.95	–	–	4.95	–	Vdc
			10		9.95	–	9.95	–	–	9.95	–	
			15		14.95	–	14.95	–	–	14.95	–	
V_{IL}	Input Low Voltage	All	5	$V_O=$ 0.5V or 4.5V	–	1.5	–	–	1.5	–	1.5	Vdc
			10	1.0V or 9.0V	–	3.0	–	–	3.0	–	3.0	
			15	1.5V or 13.5V $\lvert I_O \rvert \leq 1\mu A$	–	4.0	–	–	4.0	–	4.0	
V_{IH}	Input High Voltage	All	5	$V_O=$ 0.5V or 4.5V	3.5	–	3.5	–	–	3.5	–	Vdc
			10	1.0V or 9.0V	7.0	–	7.0	–	–	7.0	–	
			15	1.5V or 13.5V $\lvert I_O \rvert \leq 1\mu A$	11.0	–	11.0	–	–	11.0	–	
I_{OL}	Output Low (Sink) Current	Mil	5	$V_O=0.4V$, $V_{IN}=0$ or 5V	0.64	–	0.51	–	–	0.36	–	mAdc
			10	$V_O=0.5V$, $V_{IN}=0$ or 10V	1.6	–	1.3	–	–	0.9	–	
			15	$V_O=1.5V$, $V_{IN}=0$ or 15V	4.2	–	3.4	–	–	2.4	–	
		Comm	5	$V_O=0.4V$, $V_{IN}=0$ or 5V	0.52	–	0.44	–	–	0.36	–	mAdc
			10	$V_O=0.5V$, $V_{IN}=0$ or 10V	1.3	–	1.1	–	–	0.9	–	
			15	$V_O=1.5V$, $V_{IN}=0$ or 15V	3.6	–	3.0	–	–	2.4	–	
I_{OH}	Output High (Source) Current	Mil	5	$V_O=4.6V$, $V_{IN}=0$ or 5V	-0.25	–	-0.2	–	–	-0.14	–	mAdc
			10	$V_O=9.5V$, $V_{IN}=0$ or 10V	-0.62	–	-0.5	–	–	-0.35	–	
			15	$V_O=13.5V$, $V_{IN}=0$ or 15V	-1.8	–	-1.5	–	–	-1.1	–	
		Comm	5	$V_O=4.6V$, $V_{IN}=0$ or 5V	-0.2	–	-0.16	–	–	-0.12	–	mAdc
			10	$V_O=9.5V$, $V_{IN}=0$ or 10V	-0.5	–	-0.4	–	–	-0.3	–	
			15	$V_O=13.5V$, $V_{IN}=0$ or 15V	-1.4	–	-1.2	–	–	-1.0	–	
I_{IN}	Input Current	Mil	15	$V_{IN}=0$ or 15V	–	±0.1	–	–	±0.1	–	±1.0	µAdc
		Comm	15	$V_{IN}=0$ or 15V	–	±0.3	–	–	±0.3	–	±1.0	µAdc
C_{IN}	Input Capacitance per Unit Load	All	–	Any Input	–	–	–	–	7.5	–	–	pF

*T_{LOW} = -55°C for Military Temp. Range device, -40°C for Commercial Temp. Range device.
*T_{HIGH} = +125°C for Military Temp. Range device, +85°C for Commercial Temp. Range device.

CMOS Fundamentals



MOS DEVICES

Complementary MOS (CMOS) logic, memory, and switching circuits are constructed with P-channel and N-channel enhancement-mode MOS transistors diffused on a monolithic silicon chip. Field-effect transistors are unipolar devices; that is, their operation is based on a function of only one type of charge carrier — holes in P-channel types, and electrons in N-channel types.

A simplified cross-section of an N-channel enhancement-mode MOS transistor is shown in Figure 1. This transistor is a four-terminal device. In CMOS logic applications, the substrate and the source are usually connected to a common point, which in the N-channel transistor is the most negative potential or V_{SS}. With no voltage applied between gate and source, the two N+ diffusions are electrically isolated from each other and no conduction occurs. As an increasingly positive voltage is applied to the gate, an N-type inversion layer begins to form at the surface between source and drain. When a threshold voltage V_{TN} is reached, the inversion layer just begins to connect source and drain, allowing some conduction. As the gate voltage increases further, the inversion layer is driven deeper, resulting in greater conductivity from source to drain. A saturation point is reached when $+V_{DS}$ is forced higher than V_G-V_{TN}; the device, therefore, is self-current-limiting. Figure 2 shows typical drain characteristics for an N-channel MOS transistor. Note the similarity to equivalent vacuum tube characteristics.

Operation of the P-channel device (Figure 3) is similar, except that the source and substrate are connected to the most positive potential, V_{DD}. A P-type inversion layer, or channel, is formed when a negative voltage is applied to the gate with respect to the source. The threshold voltage V_{TP} is defined as that value of V_G which causes a specified minimum conductivity between source and drain. Saturation occurs when the drain-to-source voltage V_{DS} is forced more negative than V_G-V_{TN}. Figure 4 shows typical drain characteristics for a P-channel MOS transistor.

N–Channel MOSFET Operation

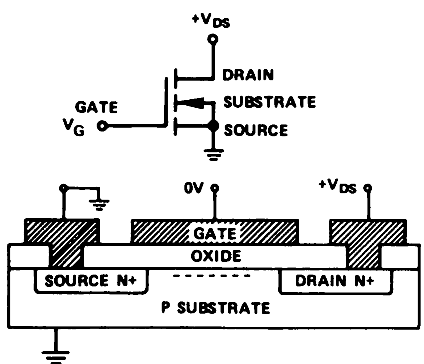


Figure 1

Typical N-Channel Drain Characteristics

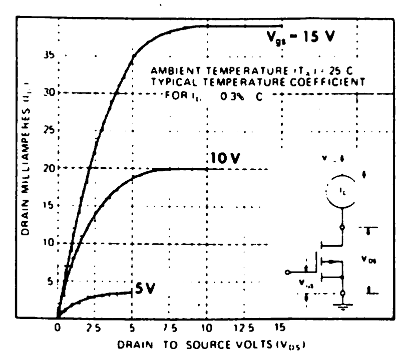


Figure 2

P–Channel MOSFET Operation

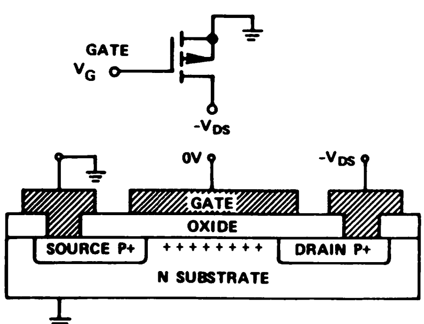


Figure 3

Typical P-Channel Drain Characteristics

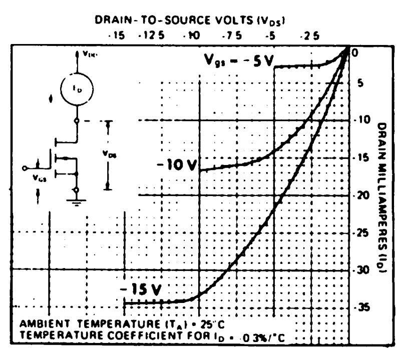


Figure 4

Basic CMOS Inverter Circuit

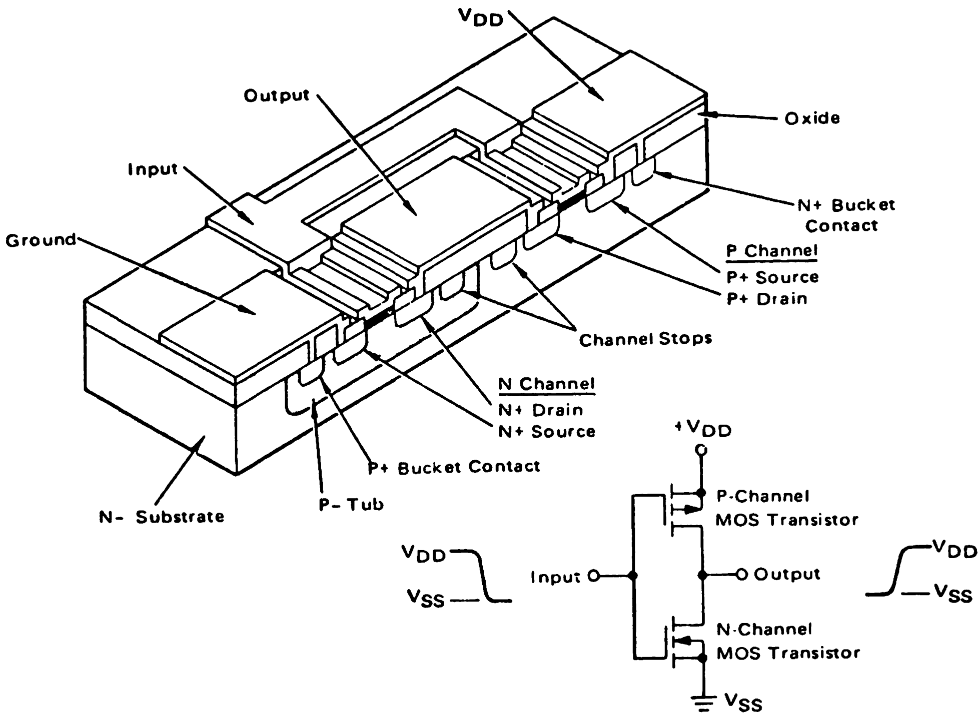


Figure 5

A major feature of the metal oxide semiconductor is the very high input resistance resulting from the dielectric oxide isolation between the gate and the channel. The input resistance is virtually unaffected by the polarity of the gate bias. Also, whatever leakage current does exist between gate and source is relatively independent of ambient temperature variations.

CMOS DEVICES

Complementary MOS logic circuits employ both P-channel and N-channel enhancement-mode MOS transistors. They have opposite, or complementary, switching characteristics and can therefore be used as virtually ideal switching components. Consider the implementation shown in Figure 5. The circuit consists of one P-channel device and one N-channel device. Note that to form the N-channel device, a P-doped "tub" must be created into which the device is placed. "Channel stops" must also be placed between the P-tub and the P-drain to prevent parasitic channeling effects.

When a positive voltage V_{DD} is applied at the input, the P-channel switches off and the N-channel switches on. Thus, the output is connected to V_{SS} through the low on-resistance of the N-channel device. Alternatively, applying V_{SS} to the input turns off the N-channel and turns on the P-channel. In this state, the output is connected to V_{DD} through the equivalent on-resistance of the P-channel device. Therefore, an input voltage of V_{DD} results in an output voltage of V_{SS}, and an input voltage of V_{SS} results in an output voltage of V_{DD}. The circuit is a simple digital inverter.

Gates

Any logic function capable of being constructed with ideal switches can be implemented in CMOS. Adding a parallel P-channel device and a series N-channel device to the basic inverter transforms the circuit into a positive-logic 2-input NAND gate (Figure 6). Adding a parallel N-channel and a series P-channel device instead transforms the inverter into a 2-input NOR gate.

CMOS NAND Gate

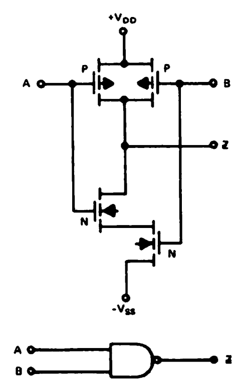


Figure 6

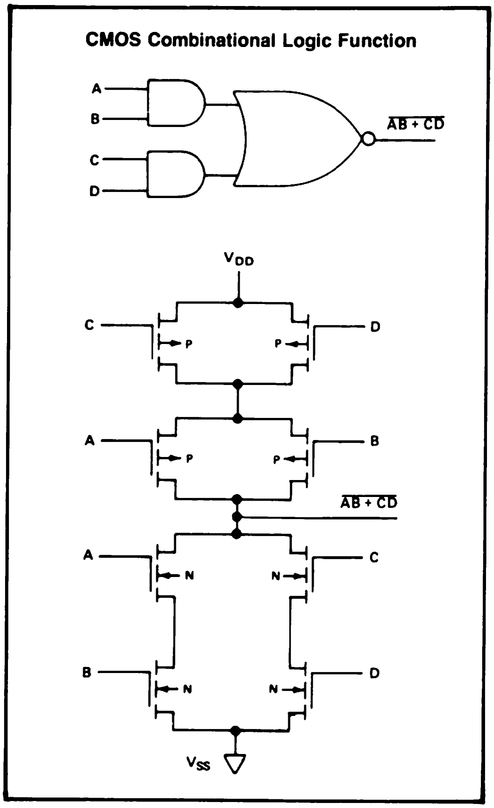


Figure 7

Note that in each circuit there exists no DC path from V_{DD} to V_{SS}: if a connection is made to V_{SS} through the N-channels, a corresponding P-channel blocks the connection to V_{DD}; alternatively, if the P-channels are on, then a corresponding N-channel is off. Therefore, very low power dissipation results without sacrificing low output impedance.

Combinational Logic

Numerous functional logic combinations are easily implemented in CMOS. A rule of thumb is series N-channel devices for AND/NAND functions, and parallel N-channel devices for OR/NOR functions. The P-channel devices are then configured in the circuit dual of the N-channel devices. Figure 7 shows the common AND/OR/INVERT (AOI) construction.

Transmission Gates (Analog Switches)

The CMOS transmission gate, or analog switch, is a single-pole single-throw (SPST) switch formed by the parallel connection of a P-channel and an N-channel

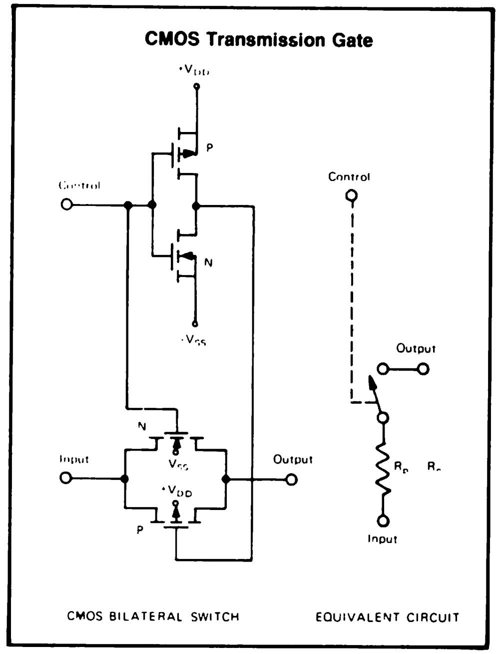


Figure 8

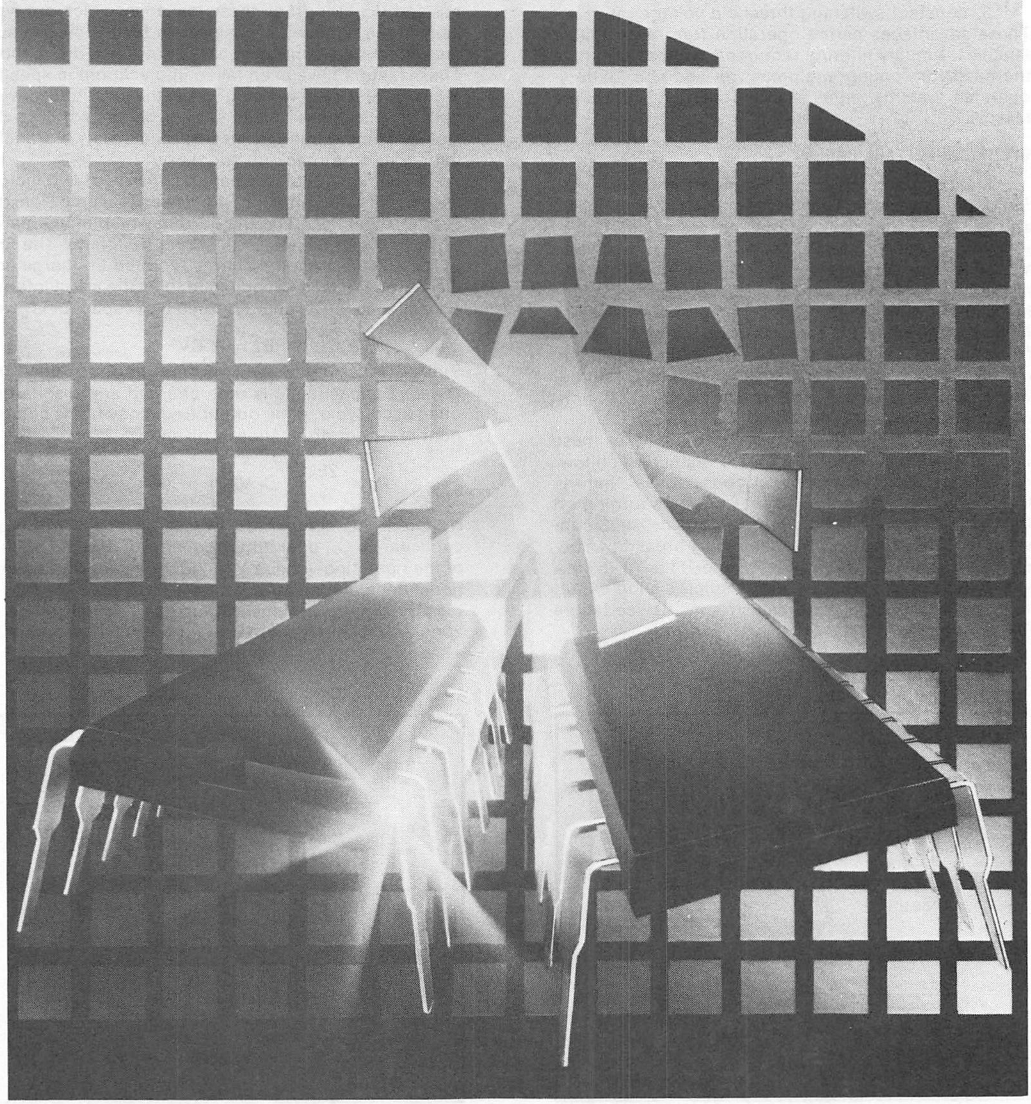
device (Figure 8). The inverter is required to apply the correct polarity gate voltage to both transistors simultaneously. The switch is purely ohmic, with an ON-resistance of about 200 - 400Ω and OFF-resistance typically about 10^{11}Ω. There is no offset voltage across the switch. These characteristics approach those of the ideal switch ($R_{ON} = 0$, $R_{OFF} = \infty$). A single-transistor switch results in a source-follower circuit in which gate cut-off occurs and limits the load to charge only to within one threshold of the gate. When two complementary devices are operated in parallel, one of the two channels is always being operated as a drain-loaded stage, permitting a low-impedance path for all switched signal voltages.

The transmission gate is useful in digital applications as well. Combinational logic functions can be implemented, and the device provides a simple method for constructing 3-state (bussed) systems.

4000 SERIES DEVICES

Using basic CMOS techniques, Solid State Scientific has developed the SCL4000 Series Family of building block elements and complex functions. Devices numbered 40xx and 45xx are equivalents to industry 40xx and 45xx types. The designation 44xx indicates proprietary devices: they are usually variations on standard 40xx devices, making them more suitable for specific applications.

Design Information



CMOS DESIGN CONSIDERATIONS

This section is presented as an aid to the systems designer in proper application and use of CMOS devices. Areas such as power supply techniques and dissipation characteristics, thermal factors, operating considerations, interfacing parameters, and ac fan-out are covered in some detail.

POWER SUPPLY CONSIDERATIONS

CMOS offers the designer several important advantages over other technologies:

1. wide operating voltage range
2. very low power dissipation
3. constant switching threshold voltage ratio

These advantages permit operation from unregulated supplies, simplify filtering requirements, and eliminate the need for cooling equipment. In addition, battery-operated systems, either stand-alone or back-up, are feasible.

OPERATING VOLTAGE RANGE

Minimum and maximum operating voltages for all Solid State Scientific CMOS devices are specified as 3 and 15 Vdc, respectively, with an absolute limitation of -0.5 and 18 Vdc, applied at the V_{DD} terminal relative to V_{SS}. The minimum value of 3 Vdc represents the maximum expected value of either P-channel or N-channel transistor threshold voltages. Operation at lower voltages may, therefore, prevent half of the device from turning on. The absolute limitation of -0.5 Vdc merely prevents the internal device junctions from becoming forward-biased: the circuit is obviously non-operational under this condition.

The maximum value prevents avalanche of these internal junctions. While the 18 Vdc restriction on low-current avalanche is somewhat conservative, there is the possibility of on-chip current transients turning on the parasitic bipolar transistors inherent in CMOS construction. The chip can enter secondary breakdown because these transients can easily exceed the 10 - 50 mA sustaining current required. The result is a short circuit reflected at the supply and catastrophic device failure (see Figure 1).

POWER DISSIPATION

The quiescent, or DC, power dissipation component consists normally of only leakage currents across reverse-biased diode junctions. This is true because, in the quiescent state, there exists no direct path between V_{DD} and V_{SS} other than these leakages, which are typically in the nanoampere region. In reality, certain surface effects will contribute to the quiescent dissipation. These factors have been taken into account in specifying the worst-case values given in the individual device data sheets; these values should be used by the designer in determining the necessary capacity of standby battery or other back-up supplies.

Dynamic, or ac, dissipation consists of two factors associated with switching: the power delivered from the supply to the load, and the current which momentarily flows between the supplies during switching. The first of these represents the energy required to charge and discharge the load capacitance (plus the small internal capacitances). The energy stored by a capacitor is given by:

$$E_S = \tfrac{1}{2} CV^2$$

Since CMOS outputs switch from supply to supply, and the load capacitance is both charged and discharged once each cycle of the output frequency f, this component of power dissipation is given by:

$$P_D = \frac{2E_S}{t} = C_L V_{DD}^2 f \qquad (V_{SS} = 0 \text{ Vdc})$$

Note that this component increases linearly with load capacitance C_L, operating frequency f, and the square of the operating voltage V_{DD}. Figure 2 shows this functional dependence for a typical CMOS gate.

The Figure assumes input rise and fall times of 20ns. As these transition times increase, however, cur-

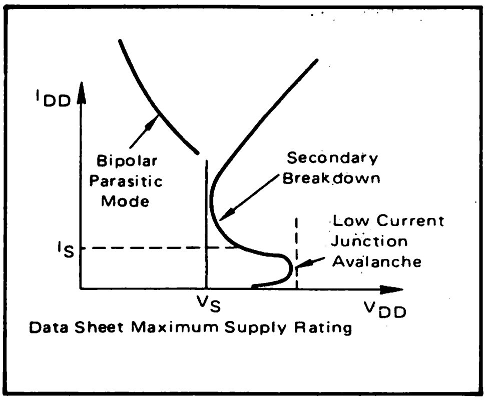


Fig. 1 — Secondary breakdown characteristics

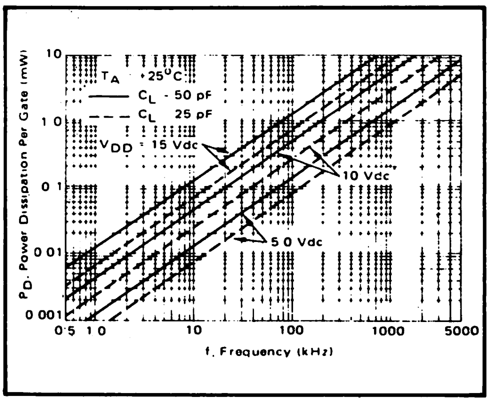


Fig. 2 — Typical gate power dissipation characteristics

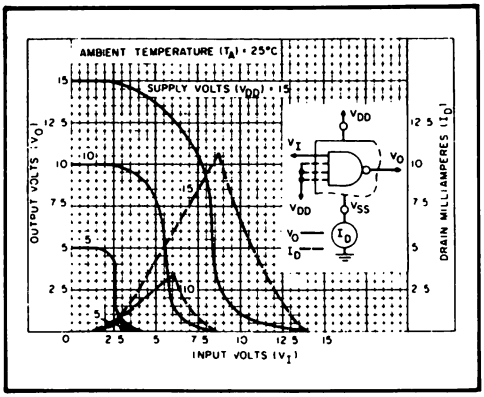


Fig. 3 – Typical current and voltage transfer characteristics

rent flows between the supplies because both P-channel and N-channel transistors are biased on momentarily. This through-current is a complex function of fabrication parameters, device geometries, operating voltage, temperature, rise and fall times, and operating frequency. A typical waveform of through-current I_{TC} in relation to voltage transfer characteristics is shown in Figure 3.

Power dissipation due to through-current can be shown to be proportional to the factors described above in the following way:

$$P_{TC} \propto f\,(t_r + t_f)V_{DD}^3$$

where the constant of proportionality is dependent upon device parameters.

The relationship between supply current I_{DD} and I_{SS}, load capacitance, and input rise and fall time is illustrated in Figure 4.

The waveforms (a) show I_{DD}, I_{SS}, and the through-current I_{TC} for a load capacitance of 15pF and t_r, t_f of 10μs. The smaller of the I_{DD} and I_{SS} pulses represents the maximum through-current of the device. The slight amplitude differences between pulses represent the current delivered to the load. The magnitude of the through-current pulses in (a) is used as the standard for (b) and (c).

The input rise and fall times are decreased to 400ns in (b). Here again, the smaller current pulses represent through-current, which has somewhat decreased from (a). Note that since the width of the current pulse has also decreased, the magnitude of the current delivered to the 15pF load has increased (to deliver the same charge).

Load capacitance in (c) is increased to 65pF, and input transition times decreased to 40ns. Through-current pulses have virtually disappeared, except for the current charging and discharging internal capacitance. The magnitude of the load current, however, has increased due to the increased load and narrower current pulse width.

All complex CMOS functional devices employ buffered inputs to minimize the through-current effects described here. Caution is urged when using high-current buffers and unbuffered gates in conjunction with large loads and high operating voltages; long input rise and fall times may cause the device power dissipation restriction to be exceeded.

REGULATION AND BATTERY OPERATION

The wide operating voltage range and constant switching voltage ratio of CMOS permit use of simple unregulated supplies, as shown in Figure 5.

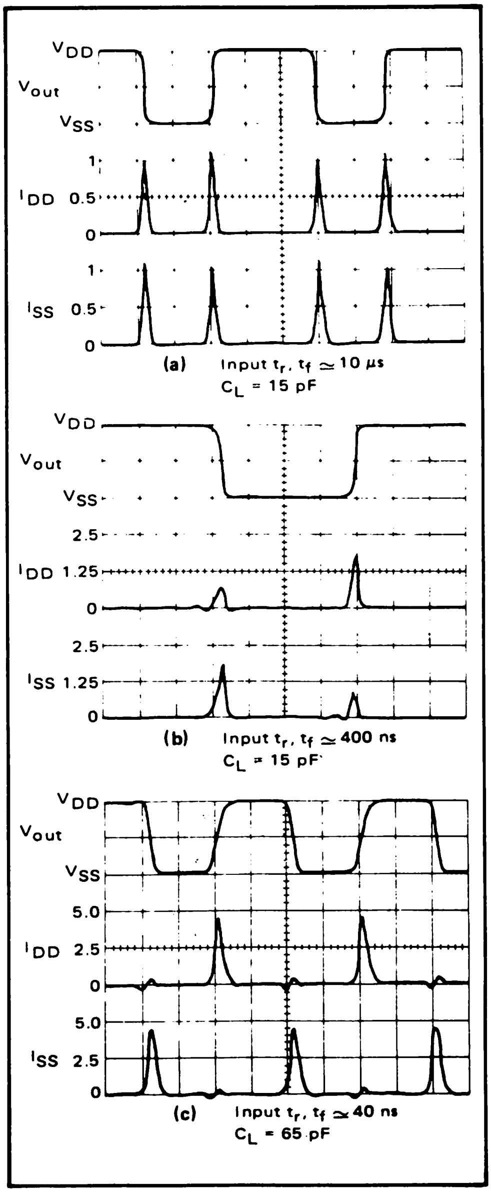


Fig. 4 – Switching current waveforms

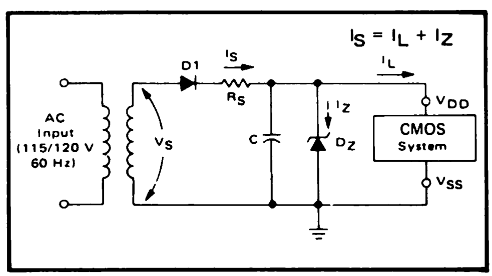


Fig. 5 – CMOS unregulated power supply

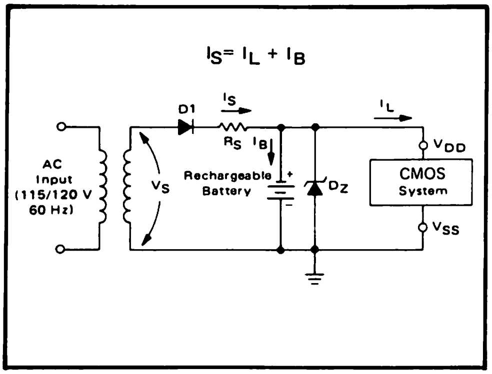


Fig. 6 — CMOS battery back-up power supply

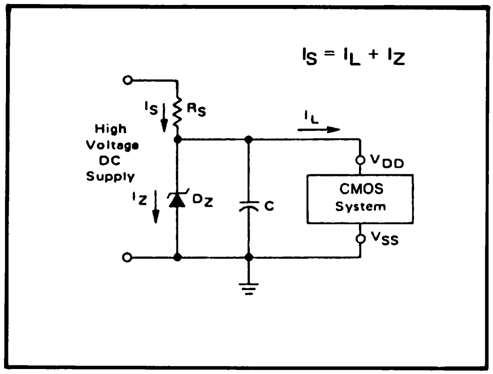


Fig. 7 — Deriving CMOS power from high voltage DC source

The primary considerations with a supply of this type are:

1. The resulting voltage must at all times fall within the specified limits of the system. This is the purpose of the zener diode.
2. The lowest instantaneous voltage must permit the system to operate at the worst-case system speed parameters.
3. The filter capacitor must be able to furnish the worst-case system switching current. R_S is selected to supply the peak transient current of the system plus the necessary zener current when diode D_1 is forward biased (high portion of V_S cycle). The capacitor is selected to supply the system switching current and quiescent current when D_1 is reverse biased (low portion of V_S cycle).

Replacing the filter capacitor with a rechargeable battery provides an easy method of implementing a back-up supply (see Figure 6). Here, R_S supplies also the charging current for the battery. The zener diode has a breakdown voltage between the battery voltage and the maximum device rating. It prevents power line transients from developing damaging voltage spikes due to the characteristic impedance of the battery. Systems may be kept operating over long periods of time on such a supply.

CMOS power supplies may also be derived from higher-voltage dc supplies as shown in Figure 7. The zener diode regulates the CMOS supply voltage; resistor R_S supplies the load and zener currents, while the filter capacitor maintains the voltage during switching transients.

FILTERING

Most CMOS systems require less filtering on supply busses than other logic families. While V_{DD} and V_{SS} line drops are generally small due to the small currents involved, a few capacitors per board are recommended to prevent switching transients from causing excessive voltage variations. This is especially true with devices which have long rise and fall time input signals. As described in the discussion of through-current, large supply currents can result under these conditions. An extra 0.1 μ F capacitor may be required to supply the current surge without causing excessive supply voltage drops. Similarly, devices which operate synchronously, such as counters and shift registers, supply large charging currents to several loads during switching. Here again, 0.1 μ F bypass capacitors may be indicated in such cases.

THERMAL FACTORS

Transfer characteristics of CMOS devices exhibit excellent stability over temperature. This feature allows the ambient temperature range of CMOS devices to be a function of package type. This section discusses techniques of thermal management and the variation of device characteristics with temperature.

THERMAL MANAGEMENT

Circuit performance and long-term reliability are maximized at low junction temperatures. Power dissipation is the common source of heat in any system; the negligible power consumed in the quiescent state in CMOS circuits is a major factor in maintaining performance and reliability. In general, operation at moderate speeds and voltages does not require consideration of the package dissipation restriction of 300 mW. In high-frequency, high-voltage, large-load, or analog applications, however, these considerations become important.

The average junction temperature is a function of device power dissipation and the ability of the packaging system to remove the generated heat. This is expressed in the following formula:

$$T_J = T_A + P_D(\Theta_{JA})$$

where T_J = junction temperature
T_A = ambient temperature
P_D = calculated power dissipation
Θ_{JA} = thermal resistance, junction-to-ambient

Worst-case and typical values of Θ_{JA} for common IC package types in still air and without heat sinking are shown in the table:

Package Type	Θ_{JA}(°C/watt) Typ	Max
Epoxy B Dual-in-line 14- or 16-lead	135	200
Cerdip Dual-in-line 14- or 16-lead	100	155
Epoxy B Dual-in-line 24-lead	95	140
Ceramic Dual-in-line 24-lead	70	100

These figures should be consulted in cases where there is reason to believe that device dissipation may be excessive.

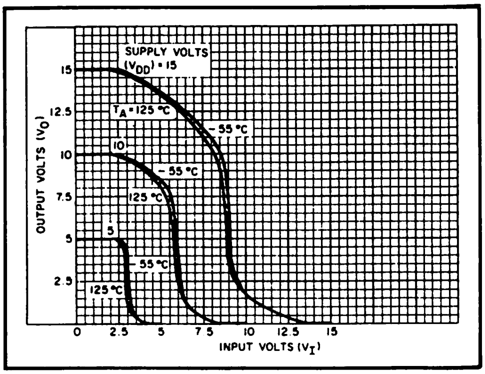


Fig. 8 — Typical inverter voltage transfer characteristics as a function of temperature

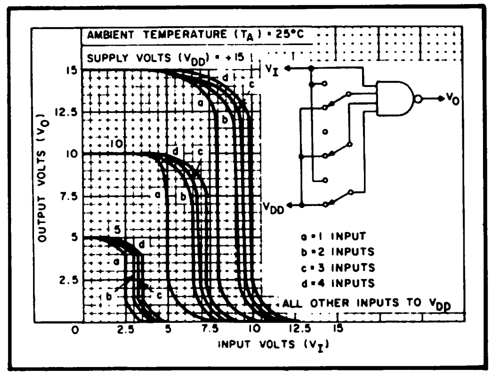


Fig. 9 — Typical multiple-input switching transfer characteristics for conventional 4-input NAND gate

PARAMETRIC THERMAL VARIATION

All operational parameters vary to some degree with temperature. Since CMOS devices may be used over very wide temperature ranges, the designer should be familiar with the effects of these thermal variations. They fall into three categories: transfer characteristics, leakage current, and channel resistance effects.

1. Transfer Characteristics
   Figure 8 illustrates the negligible variation in transfer voltage over the entire military temperature range. This results from the tendency of P-channel and N-channel transistor threshold voltages to track together. Under similar conditions, a bipolar device threshold may vary more than 40%. This features makes threshold-dependent circuits such as oscillators and multi-vibrators feasible in systems with a wide range of operating temperature.
2. Leakage Current
   As expected, since device leakage current is normally leakage across reverse-biased silicon junctions, temperature variation of this parameter follows the traditional diode leakage characteristic, i.e., approximately doubling with each 11°C rise in temperature.
3. Channel Resistance
   Such parameters as output drive current (I_{OH}, I_{OL}), switching through-current (I_{TC}), propagation delays (t_{PLH}, t_{PHL}), and output transition times (t_{TLH}, t_{THL}) are direct effects of channel resistance. These parameters vary as channel resistance varies—0.3%/°C. Current characteristics decrease with increasing temperature at this rate; this factor is employed in specifying low- and high-temperature limits for these parameters on device data sheets. Switching parameters increase at this rate with temperature; this dependence must be considered by the designer in order to guarantee system dynamic performance over temperature.

INPUT RATINGS

The high impedance of a CMOS input results from the insulating oxide between the gate and the channel. This high impedance coupled with the 5pF input capacitance make CMOS inputs excellent energy storage nodes, allowing buildup of large voltages. Input diode protection networks are used, therefore, to conduct excess energy to the supply rails, thus protecting the gate regions from damage. These diodes affect certain device operations, as described in the following discussion of general input characteristics.

INPUT VOLTAGE RANGE

Input signals should never exceed the range from 0.5 Vdc more negative than V_{SS} to 0.5 Vdc more positive than V_{DD}. This prevents forward biasing the input diodes, with the attendant possibility of entering a latch-up mode due to high-current transients. Further details may be found in the preceding discussion of "Power Supply Considerations" and later on in this section.

NOISE IMMUNITY

Noise immunity as specified in CMOS data sheets refers to the worst-case input voltage levels which will maintain guaranteed output conditions and will not produce a change in logic state. Specifically, the data sheets specify the minimum input high-level voltage (V_{IH}) and maximum input low-level voltage (V_{IL}) which guarantee an output voltage of no lower than 90% of V_{DD} or no higher than 10% of V_{DD} under no-load conditions ($|I_O|<1\mu A$). Since the switching threshold voltage of a CMOS inverter is typically 50% of the supply and fairly sharp, and output voltages are close to the supplies, these input voltages tend to be symmetric and close to the ideal situation of 50% noise immunity. In fact, V_{IH} is typically 55% of V_{DD}, and V_{IL} is 45% of V_{DD}. (Note: the older designations of V_{NH} and V_{NL} can be related to V_{IH} and V_{IL} by the following:

$$V_{NH} = V_{DD} - V_{IH}\ (\text{min})$$
$$V_{NL} = V_{IL}\ (\text{max}) - V_{SS}.)$$

Worst-case specifications under these output voltage requirements are 20% of V_{DD} for the conventional SSI devices (Note: the older 30% noise immunity specification allowed much greater output voltage variations). This specification can be greatly improved by making the transfer voltage characteristic sharper, i.e., increasing device gain. In 1970, Solid State Scientific developed the technique of buffering gate outputs for increased gain; since that time, all CMOS gates in the 4000 series have been buffered. The industry began to realize the superiority of this structure for digital logic applications only with the recent agreement on "B" series CMOS.

Buffered outputs become even more important in maintaining noise immunity with the variation in transfer voltage with input pattern on multiple input gates. Figure 9 shows the typical range in switching voltage for a conventional 4-input NAND gate. Observe that V_{IH} (min) degrades as a function of the number of inputs switching. This pattern sensitivity is reversed for NOR

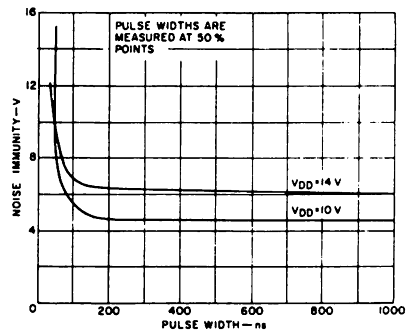


Fig. 10 — Typical signal-line noise-immunity

gate types. Buffering the device outputs, although the variations in switching voltage are unaffected, maintains greater noise immunity over all input conditions resulting from the much more nearly ideal transfer characteristic. Further improvement is attained by the requirement that CMOS gate structures consist of no more than three inputs per section; this decreases the variation in switching voltage, as compared with the 4-input gate in Figure 9. There are many other advantages to the buffered-gate concept. Each one is fully discussed in following sections.

Note that Solid State Scientific specifies and measures noise immunity under worst-case input combinations. This factor gives the designer a more realistic description of device operation, in view of the above discussion.

Noise immunity specifications refer to input signals; however, a similar discussion applies to noise introduced on power and ground lines. CMOS devices are sensitive only to negative power line transients and positive ground line transients. The magnitude of power- and ground-line noise immunity approaches that of signal-line noise immunity because of the close tracking of output voltage with supply in either state.

The relatively slow response times of CMOS devices tend to act as a noise filter: extremely short spikes of greater magnitude than the dc noise immunity limits are prevented from propagating through the device. A typical example of dc noise immunity is shown in Figure 10.

Another source of noise introduction into CMOS devices is crosstalk from high noise voltages coupled through small capacitances. Since CMOS devices have much higher output impedance than equivalent TTL types, they are much more sensitive than TTL to such capacitively-coupled noise. The designer should consult the individual device data sheets to determine the magnitude of current which will pull a CMOS output into the threshold region of the driven CMOS inputs, and use good interconnection techniques to prevent this type of crosstalk from interfering with system operation.

INPUT CURRENT

The high input impedance of CMOS results in an input current of typically 10pAdc. Worst-case specifications provide allowance for surface effects, and guarantee no higher than 100nAdc at room temperature.

These characteristics apply for input voltages within the permitted range, as described above. There are a certain class of applications, however, such as oscillators and multivibrators, for which input voltages normally exceed the supplies by large margins. In these instances, the input protection diodes can be utilized as clamps if the input current is restricted to 10mAdc or less. This is usually accomplished by adding a series resistor at the affected input. The minimum value of this resistor is calculated from the worst-case input voltage and the input current limitation; the maximum value should be determined by the effect which the combination of this resistor and the 5pF input capacitance has on operating speed and frequency.

UNUSED INPUTS

If a CMOS input is left unterminated, it can acquire unpredictable voltages through coupling with stray external capacitances and internal crosstalk. Since these voltages are normally within the supply range, the input protection diodes cannot conduct away this accumulated energy. Since both P- and N-channel transistors spend significant time in their "on" states, both power dissipation and device noise immunity degrade. Even catastrophic failure can result from these conditions. Therefore, all inputs should be connected to an appropriate supply voltage, or to another driven CMOS input. If a portion of a device is not loaded, its inputs must also be properly terminated.

INPUT WAVEFORMS

The maximum input rise and fall time specification for sequential circuits is typically in the 3μs to 15μs range, depending on supply voltage. This prevents ambiguous logic states and false clocking due to switching voltage variations and skew problems. Power dissipation also increases as logic elements spend more time in the switching region.

When sequential circuits are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load. If setup and hold times are specified on device data sheets, they must also be taken into account.

Schmitt trigger constructions may be indicated to bring rise and fall times within indicated bounds.

INPUT PROTECTION NETWORKS

Because the gate oxide of a CMOS transistor has extremely high resistance, even a very-low-energy source (such as a static charge) is capable of developing the breakdown voltage of approximately 100V. This results in permanent damage to the device. Therefore, gate protection structures are employed to conduct excess energy away from the gate region. These structures, however, are only capable of protecting from overvoltages of less than 1000V. While this is normally sufficient for in-system transients, device handling can produce overvoltages of one or two orders of magnitude greater. Handling precautions are recommended when using CMOS devices. Some suggested procedures appear in the section entitled "Handling Precautions for CMOS Devices".

The input protection structure utilized on 4000 Series devices is shown in the diagram of a typical

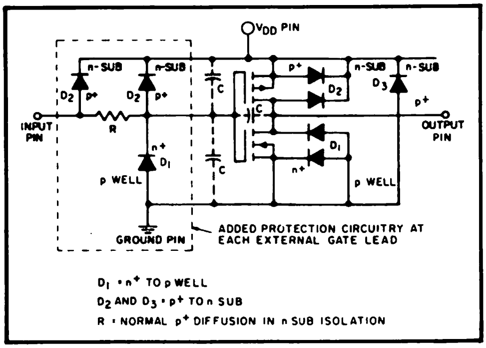


Fig. 11 — Gate-oxide protection circuit used in 4000 Series integrated circuits

CMOS device in Figure 11. The circuit consists of diodes D1 and D2, which clamp the input voltage to V_{SS} and V_{DD}, respectively, and series resistor R, whose nominal value is 1.5KΩ. Avalanche voltages of the diodes are well below the breakdown voltage of the gate oxide. The resistor provides a small delay with the 5pF input capacitance which allows excess energy to be conducted away before reaching the gate region.

When the diodes are used as clamps for oscillators, multivibrators, etc., input current must be limited to less than 10mA to protect against both possible latchup and long-term degradation due to metal migration.

In a system power-up or power-down sequence, power must be applied to the device before the introduction of low-impedance driving signals. This sequence must also be maintained while troubleshooting systems where devices or modules must be removed from or inserted into a system.

OUTPUT CHARACTERISTICS

The amount of current which a CMOS output is capable of sinking or sourcing is a function of the channel impedance of the driving structure. These characteristics vary with voltage and temperature; these variations were discussed previously. Transistor characteristics are illustrated on most device data sheets.

BUFFERED OUTPUTS

Consider the conventional CMOS 2-input NAND gate structure of Figure 12. Since the N-channel devices are in series, their on-resistance must be decreased (larger chip area) to hold the output low impedance (or sink current parameter) within specification. As the number of gate inputs increases, even larger N-channel transistors are required. Also, since the P-channel devices are connected in parallel, the output high impedance (and, therefore source current) is a function of input pattern, i.e., the number of devices turned on. Solid State Scientific gates have buffered outputs: small geometry logic transistors are used to generate the required function, while only one large P-channel and one large N-channel device form the output. This technique reduces chip size; in addition, output impedance is no longer a function of input pattern. This means that dc and ac fanout are constant, and the user need not concern himself with several sets of loading requirements for each device.

OUTPUT LOADING

Since CMOS outputs driving CMOS inputs switch essentially from supply to supply while the driven inputs draw very little current (typically 10 pAdc), dc fanout can usually be ignored, except in bus-oriented systems. Of much greater importance is ac fanout, discussed below. However, several precautions are necessary to prevent damaging the output structure.

The outputs of most CMOS devices consist of a complementary pair. This structure prohibits the connection of outputs in a "wire-OR" configuration. Three-state output devices should be used to achieve this configuration. It is possible, however, to parallel inputs and outputs of devices to provide increased drive. This practice should be restricted to devices within the same package to avoid current hogging.

Note that because of the negative temperature coefficient of MOS transistors, there is built-in short-term burn-out protection. In general, devices with standard output characteristics may be shorted to the supply rails at low operating voltages. Precautions are necessary with higher voltages and/or high-current buffers, in which saturation currents can cause the maximum dissipation limitation to be exceeded.

CMOS drive capability is limited if the outputs are required to maintain a specified logic level. However, if the output is used to drive a discrete device such as a transistor or LED, large currents (within maximum ratings) can be achieved by operating the device in the saturated region.

The output impedance of a CMOS device can be employed as an effective means of providing delay and integrator functions when loaded with a capacitor. However, in any application which places a sizable capacitive load on a CMOS output, care must be taken to prevent damaging transient currents when power is removed. If the capacitive load is charged when the power supply is removed, the diode from the output to the supply (output D2 in Figure 11) forms the discharge path as it becomes forward biased. Series resistance should be added to the output in order to prevent discharge currents above 1mA.

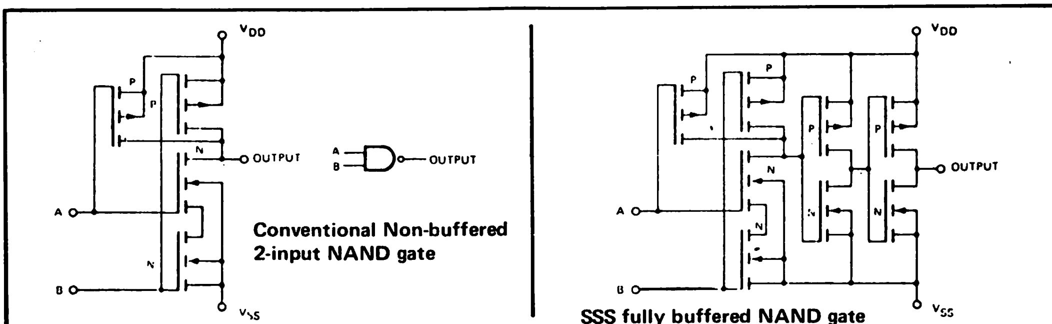


Figure 12

INTERFACE PARAMETERS

Table I provides interface parameters between CMOS and other logic families under the following conditions:

1. The power-supply voltage level and tolerances are chosen to accommodate the interfaced elements, since CMOS devices will operate over a much wider range.
2. The logic levels at the interface will meet or exceed the specified worst-case logic levels of the other elements.
3. Fan-out rules at the interface are derived from the current sourcing or sinking capability of the driving element.

TABLE I. CMOS INTERFACE PARAMETERS

INTERFACE	INTERFACE NOISE MARGIN "1"	INTERFACE NOISE MARGIN "0"	INTERFACE LOGIC LEVELS "1"	INTERFACE LOGIC LEVELS "0"	INTERFACE MAXIMUM FAN OUT	REMARKS
CMOS-CMOS	1.5V	1.5V	3.5V	1.5V	> 50	5-volt system
	3.0V	3.0V	7.0V	3.0V	> 50	10-volt system
	4.0V	4.0V	11.0V	4.0V	> 50	15-volt system
CMOS-TTL/DTL	2.5V	0.4V	2.0V	0.8V	2	Buffers only
TTL/DTL-CMOS	1.1V	1.1V	3.5V	1.5V	See Remarks	2KΩ pull-up resistor for TTL or open-collector DTL. Fan-out determined by dynamic requirements
CMOS-LTTL	2.5V	0.5V	2.0V	0.7V	2	Standard "B" Series Output Drive
LTTL-CMOS	1.1V	1.2V	3.5V	1.5V	See Remarks	3KΩ pull-up resistor. Fan-out determined by dynamic requirements
CMOS-LSTTL	2.5V	0.4V	2.0V	0.8V	1	Standard "B" Series Output Drive
LSTTL-CMOS	1.1V	1.1V	3.5V	1.5V	See Remarks	3KΩ pull-up resistor. Fan-out determined by dynamic requirements.
CMOS-HTL	5.0V	5.0V	8.5V	6.5V	1	
HTL-CMOS	2.5V	2.5V	11.0V	4.0V	> 50	Active pull-up HTL
	3.5V	3.5V			> 50	Passive pull-up HTL with 2KΩ to 5KΩ pull-up resistor.
CMOS-MOS	3.0V	4.0V	-3.0V	-9.0V	> 50	High threshold PMOS: V_{SS}-V_{DD}=13V
	2.5V	6.0V	2.5V	1.0V	> 50	Low threshold PMOS: V_{SS}-V_{DD}=10V
MOS-CMOS	3.9V	3.9V	-3.9V	-9.1V	> 50	High threshold PMOS: V_{SS}-V_{DD}=13V
	3.0V	3.0V	2.0V	-2.0V	> 50	Low threshold PMOS: V_{SS}-V_{DD}=10V
CMOS-ECL	0.225V	4.325V	-1.105	-1.475	2	V_{DD}=ground V_{SS}= -5.2V
ECL-CMOS	0.66V*	1.56V*	-1.56V	-3.64V	> 50	V_{DD}=ground V_{SS}= -5.2V

* typical with transistor driver

NOTES: 1. Interface Noise Margin
For "1" Column — difference between output high level of one device and input high level of next device.
For "0" Column — difference between output low level of one device and input low level of next device.
2. Interface Logic Level Worst-case threshold level going from one device to the input of another.

DYNAMIC CONSIDERATIONS

The operating speed of a CMOS logic system is dependent upon signal propagation delays. output transition times. and associated characteristics. These parameters vary as a function of output load capacitance (ac fanout). operating voltage. and device temperature.

All device data sheets give dynamic characteristics at V_{DD} 5. 10. and 15 Vdc. 50pF load capacitance. and 25 C ambient temperature.

CAPACITIVE LOADING

The higher output impedance of CMOS devices. in comparison to TTL. make them more sensitive to capacitive loading (ac fan-out). A linear relationship exists between dynamic parameters and load capacitance. which is to be expected: loads are charged and discharged by the resistance of the driving transistor channel.

The buffered gate output structure pioneered by Solid State Scientific in 1970 provides significantly better performance than conventional CMOS gate structures. The single stage output makes delays and transition times independent of input pattern and less sensitive to capacitive loading In addition. the extra gain stages provide significant pulse shaping of slow transition inputs — when input rise and fall times increase. the conventional gate exhibits an increase in output transition time. while the buffered gate transition times remain unchanged. This feature eliminates progressive deterioration of pulse characteristics in a system. These buffered outputs are designed for symmetric transition times. as opposed to the conventional types.

Special considerations must be given to output transition times and propagation delays when driving synchronous systems with edge triggered inputs. Consult the section on "Input Waveforms".

It should be noted that the extra gain stages in a buffered-output gate exhibit very sharp transfer characteristics. In certain applications. notably oscillators. multivibrators. or poor input transitions. this may result in ringing or even oscillation at the switching point. For this reason. Solid State Scientific manufactures several simple unbuffered inverters (4007UB. 4069UB. 4449UB) and unbuffered 2-input gates (4001UB. 4011UB). Since these types exhibit none of the features of buffered outputs. it is recommended that some pulse shaping be employed to permit use of the buffered structures wherever possible.

VOLTAGE EFFECTS

Increasing the supply voltage from 5Vdc to 10Vdc at least doubles the operating speed of CMOS devices. Increasing to 15V results in another increase. usually far less. at a substantial penalty in power dissipation. The increase in speed is a direct effect of the lower channel resistance; the increase in power dissipation is a symptom of higher charging currents to load capacitances.

Dynamic characteristics at voltages not given on device data sheets may be interpolated from specified data.

TEMPERATURE VARIATIONS

As the temperature of a CMOS device increases. carrier mobility decreases. resulting in an increase in channel impedance. Therefore. dynamic parameters change in proportion to the factor given previously: -0.3%/ C for operating frequency. +0.3%/ C for all other parameters. Consequently. this factor must be considered in designing a system which must operate at a given frequency over a wide temperature range.

THREE STATE LOGIC

Devices such as the 4016 and 4066 provide a means for constructing bus-oriented systems. Several devices in the 4000 Series employ variations in this structure to provide their own high-impedance output state. Leakage currents and capacitances are specified on individual data sheets. to allow the user to determine fan-out and system speed.

ANALOG SIGNAL SWITCHING

When using the analog switch device types. care must be taken to prevent the input signal from exceeding the supply voltage. Latch-up conditions may result if this precaution is not observed.

The ON-resistance characteristics of the switch are specified on the device data sheets. This enables the user to calculate power dissipation for high-current-drive requirements.

All CMOS switches are make-before-break. Therefore. in multiplexing applications. the low-impedance path between signal drivers which occurs during the overlap must be considered when generating control-input signals.

Further information is contained on individual data sheets.

HANDLING CMOS DEVICES

Care must be exercised in handling any CMOS device. Although all SSS CMOS devices have a built-in protective diode network which protects the device against damage due to static electric discharge, additional precautions should be followed to assure trouble-free performance after assembly. The following guidelines for handling CMOS devices are suggested:

A. GENERAL

- Use a conductive, grounded work surface.
- Keep operators at ground potential (use conductive wrist bands and a 1 megohm resistor to ground)
- Don't use nylon smocks.
- Repack devices in conductive or anti-static containers; keep devices at a common potential.
- Use conductive or anti-static envelopes for storing and shipping devices — never use untreated plastic.

B. CLEANING

- Use static neutralizing ion blower when manually cleaning with brushes.
- Ground all automatic equipment.
- Ground cleaning baskets.

C. ASSEMBLY

- Insert CMOS devices last to avoid overhandling.
- Use conductive handling trays.
- Use conductive material between edge connections.
- Ground all automatic insertion equipment.
- Ground solder machines and metallic parts of conveyor systems.
- Ground soldering irons.

D. TESTING

- Use grounded metallic fixtures where possible.
- Use static neutralizing ion air blower when using automatic handlers.
- Use conductive handling trays.
- Don't insert or remove boards with power turned ON.

CMOS CHIPS

Solid State Scientific CMOS integrated circuits are provided in chip form to permit customer design of special or hybrid circuits to suit individual needs. CMOS chips are electrically identical to (temperature range −55°C to +125° C) and offer the features of their packaged counterparts. For maximum ratings, electrical characteristics, schematics, and features, see the individual data sheets in this catalog.

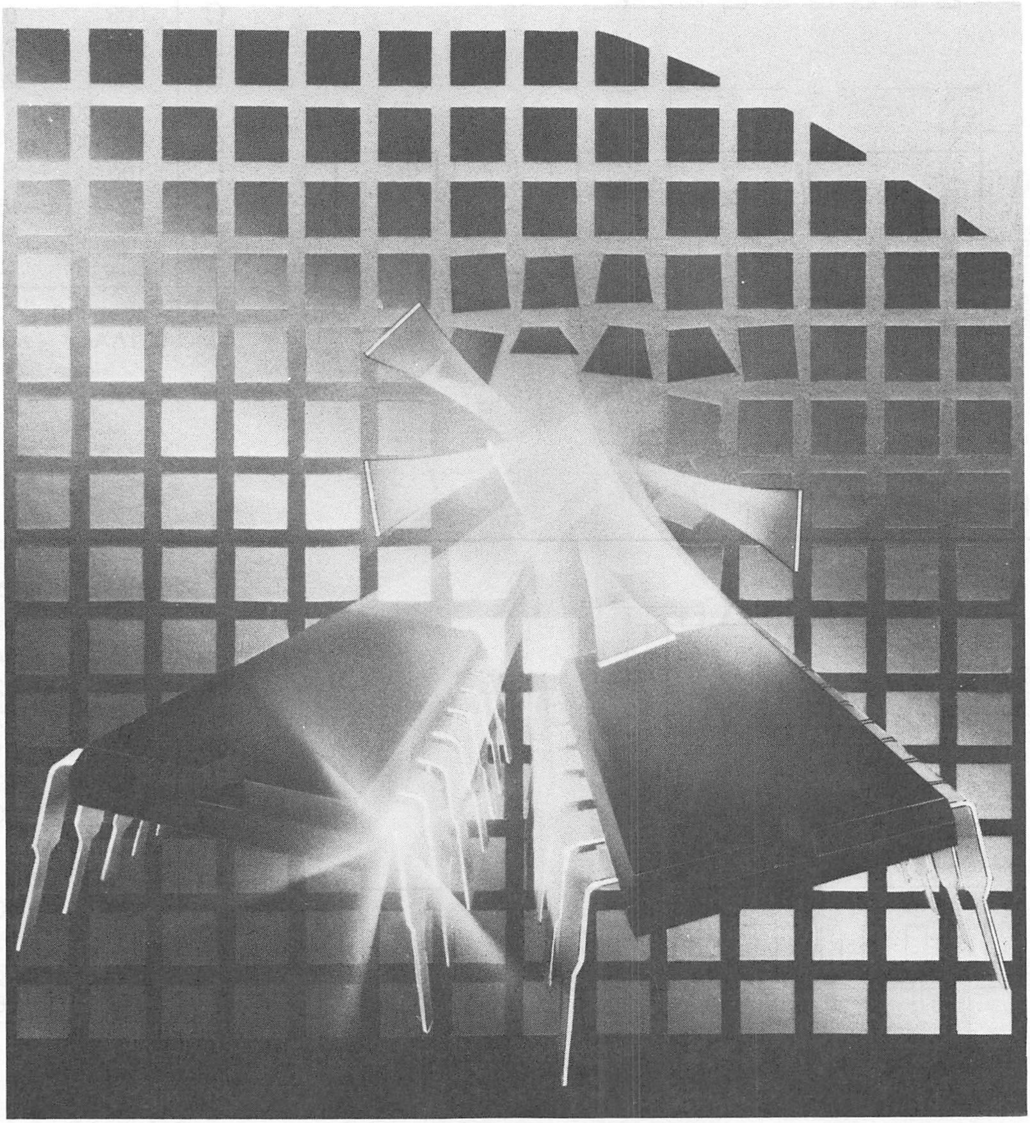
CHIP PREPARATION

- All chips are glass passivated.
- All chips have been electrically tested for all static and functional parameters.
- Chip inspection and packaging is performed under laminar flow hoods in a temperature- and humidity-controlled dust-free atmosphere.

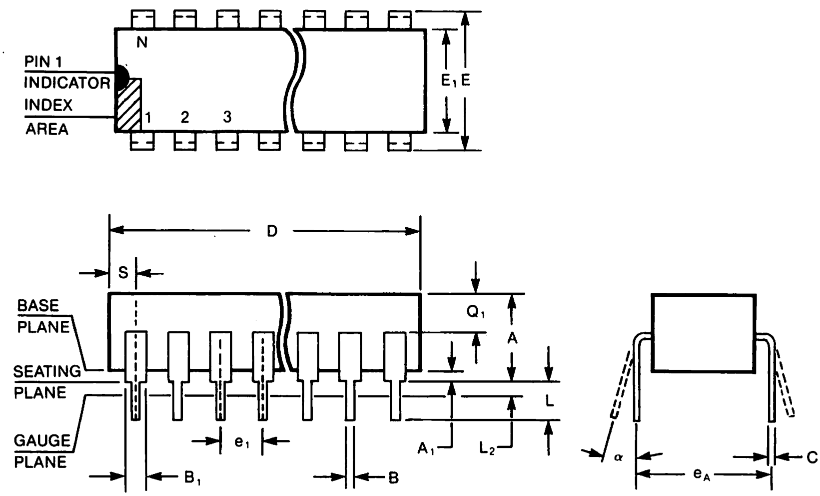
CHIP HANDLING

- Chips should be stored in a clean, dry atmosphere preferably below 40° C and 50% relative humidity.
- The user should exercise proper care when handling chips to prevent even the slightest mechanical damage to the chip.
- Individual handling should be done with nonmetallic vacuum pick-ups.
- Proper mounting and lead bonding techniques must be used to obtain optimum electrical, mechanical and thermal performance.
- The back surface of the chip is electrically connected to the P-channel substrates which should be the most positive potential (V_{DD}). Care must be taken to keep the active substrate isolated from ground or other circuit elements in the assembly. It is recommended that the $+V_{DD}$ pad on the front of the chip be wire bonded to the chip substrate mount for optimum performance.
- After mounting and bonding, necessary procedures must be followed to insure that the chips are not subjected to mechanical abuse or to moist or contaminated atmosphere which might permit electrical conductive paths across the relatively small insulating surfaces.
- Bonders, pick-up tools, table tops, sealing and die attach equipment, and other apparatus used in chip handling should be properly grounded.
- The operator should be properly grounded.
- Assemblies or sub-assemblies of chips should be transported and stored in conductive carriers.
- All external leads of assemblies should be shorted together.

Typical Package Outlines



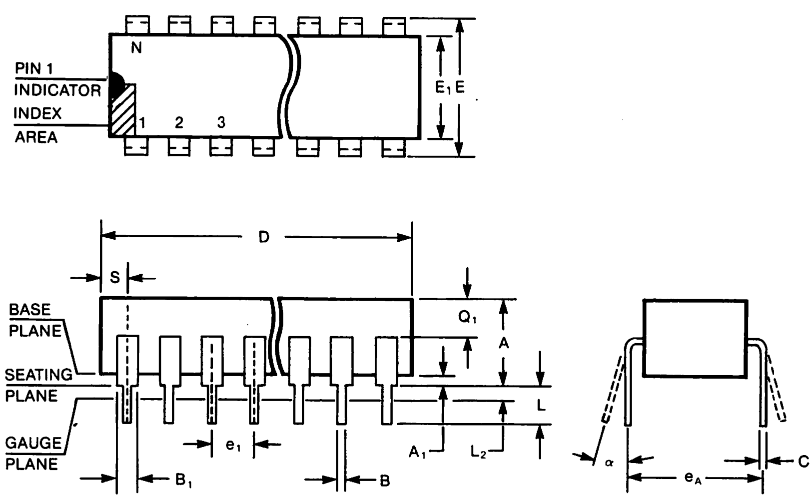
14 Lead Cerdip*



	MIN.	MAX.
A	—	.200
A_1	.020	—
B	.015	.023
B_1	.030	.070
C	.008	.015
D	.660	.785
E_1	.220	.280
e_1	.100 Typ.	
e_A	.300 Typ.	
L	.100	—
α	0°	15°
Q_1	—	—
S	—	—

*JEDEC drawing #MO-001AA

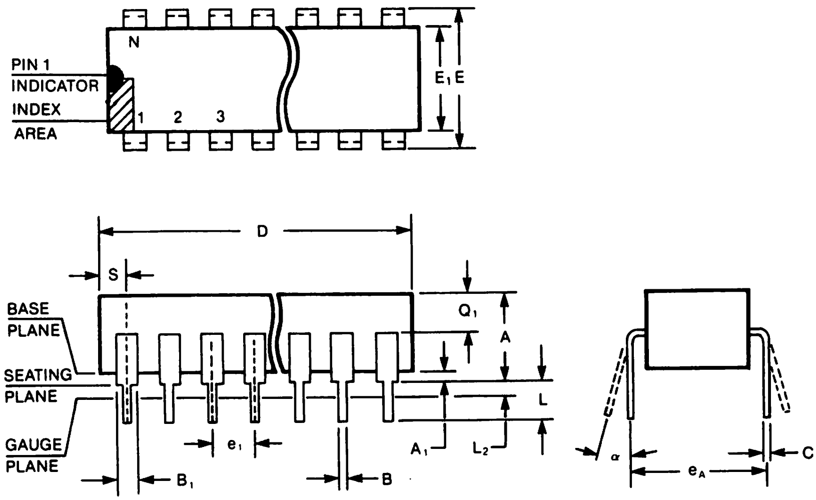
16 Lead Cerdip*



	MIN.	MAX.
A	.165	.210
A_1	.015	.045
B	.015	.020
B_1	.045	.070
C	.009	.011
D	.750	.795
E_1	.245	.300
e_1	.100 Typ.	
e_A	.300 Typ.	
L	.120	.160
α	2°	15°
Q_1	.050	.080
S	.010	.060

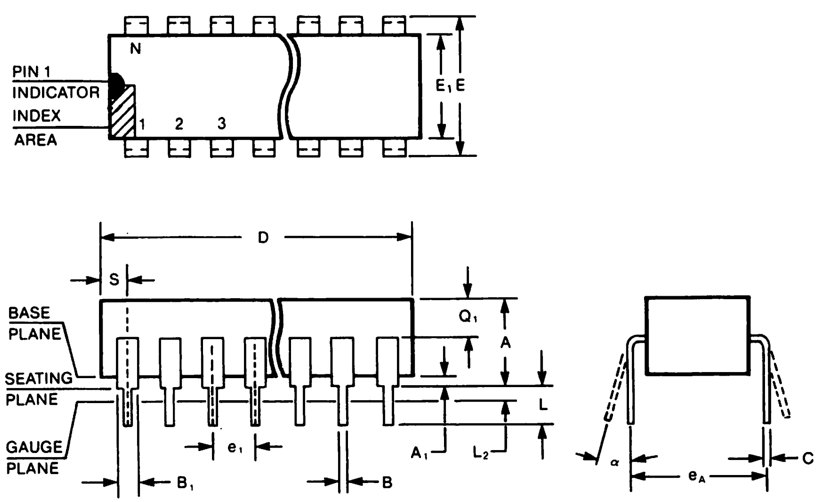
*JEDEC drawing #MO-001AG

18 Lead Cerdip



	MIN.	MAX.
A	.165	.202
A_1	.015	.040
B	.015	.020
B_1	.053	.065
C	.008	.012
D	.870	.923
E_1	.258	.306
e_1	.100 Typ.	
e_A	.300 Typ.	
L	.120	.155
α	4°	15°
Q_1	—	—
S	.020	.060

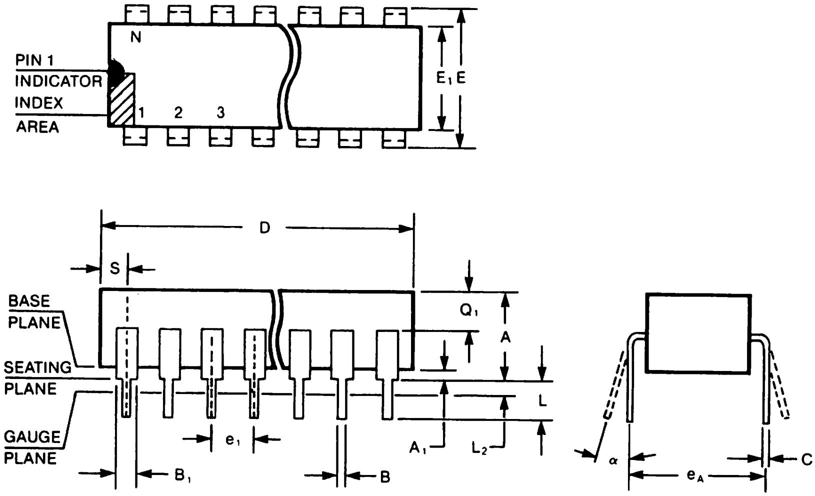
22 Lead Cerdip*



	MIN.	MAX.
A	.090	.150
A_1	.020	.065
B	.014	.020
B_1	.035	.065
C	.008	.012
D	1.050	1.110
E_1	.370	.390
e_1	.100 Typ.	
e_A	.400 Typ	
L	.120	.160
α	0°	15°
Q_1	.010	.050
S	.035	.060

*JEDEC drawing #MO-026AA

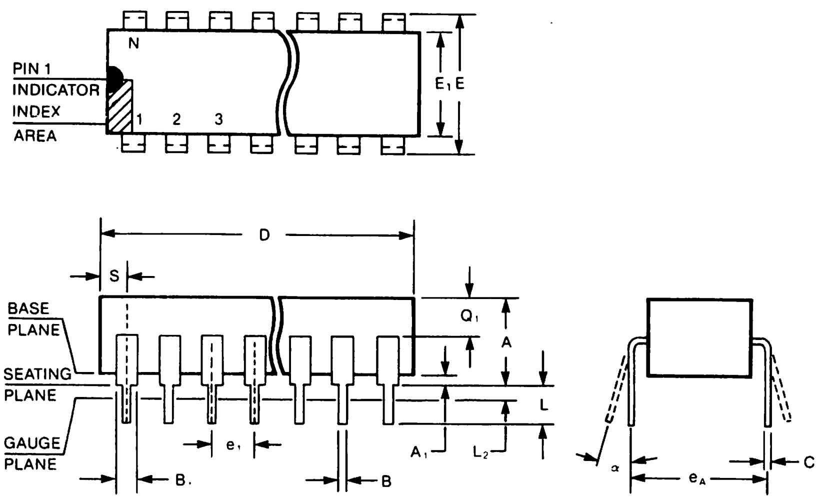
24 Lead Cerdip*



	MIN.	MAX.
A	.120	.250
A_1	.020	.070
B	.016	.020
B_1	.028	.070
C	.008	.012
D	1.200	1.290
E_1	.515	.580
e_1	.100 Typ.	
e_A	.600 Typ	
L	.100	.200
α	0°	15°
Q_1	.040	.075
S	.040	.100

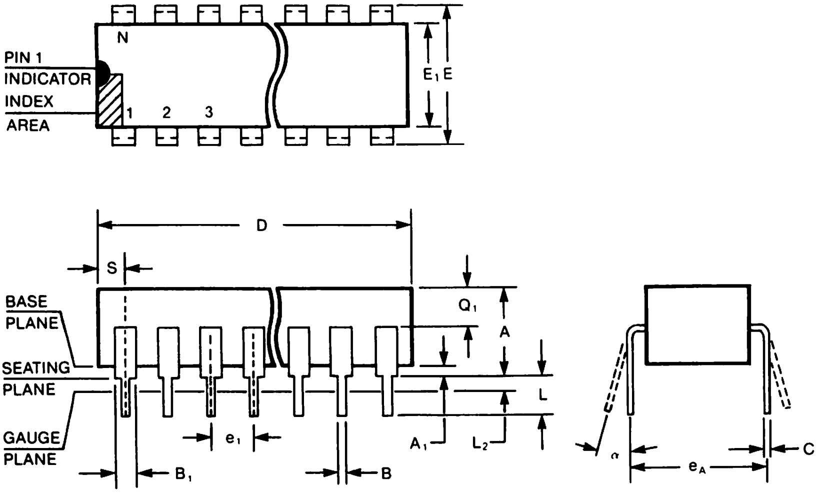
*JEDEC drawing #MO-015AA

28 Lead Cerdip



	MIN.	MAX.
A	.164	.219
A_1	.020	.070
B	.016	.020
B_1	.050	.060
C	.008	.012
D	1.430	1.485
E_1	.510	.541
e_1	.090	.110
e_A	.600	.620
L	.120	.155
α	4°	20°
Q_1	—	—
S	.060	.090

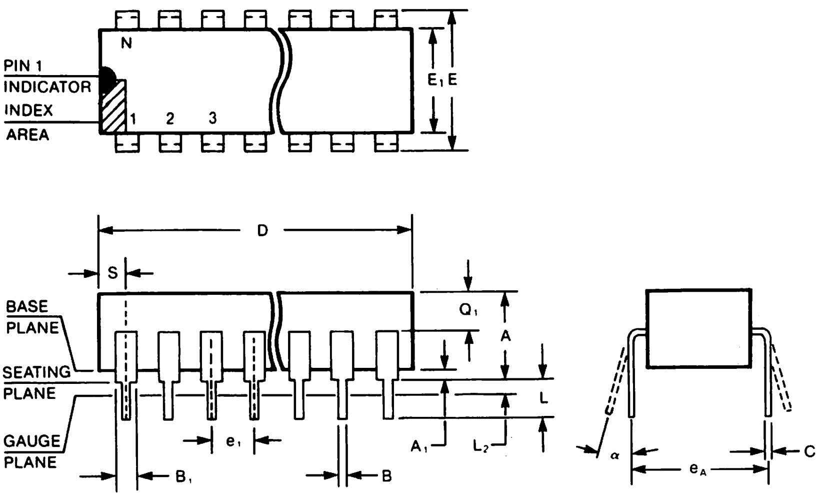
40 Lead Cerdip*



	MIN.	MAX.
A	.160	.220
A_1	.000	.070
B	.015	.020
B_1	.015	.055
C	.008	.012
D	2.020	2.070
E_1	.485	.580
e_1	.100 Typ.	
e_A	.600 Typ.	
L	.100	.200
α	0°	15°
Q_1	.070	.120
S	.060	.090

*JEDEC drawing
MO-015AJ

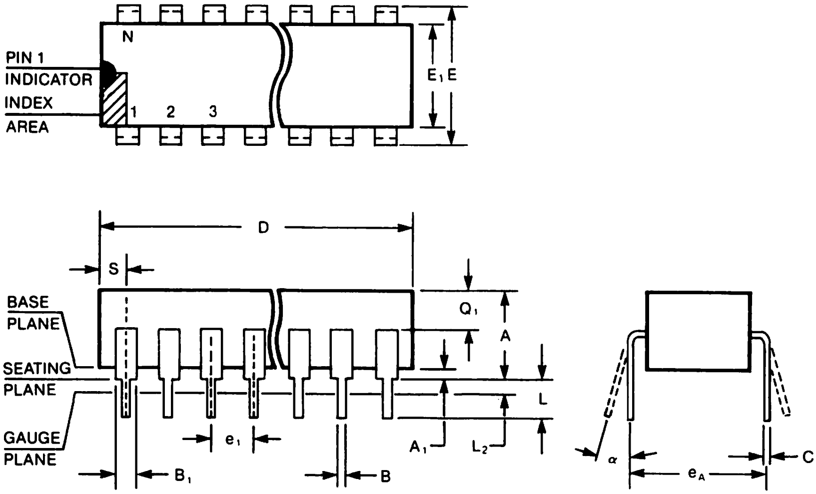
14 Lead Plastic*



	MIN.	MAX.
A	.140	.180
A_1	.015	.040
B	.014	.020
B_1	.044	.070
C	.008	.012
D	.730	.770
E_1	.240	.260
e_1	.100 Typ.	
e_A	.300 Typ.	
L	.115	.155
α	0°	15°
Q_1	.050	.085
S	.055	.095

*JEDEC drawing
#MO-001AH

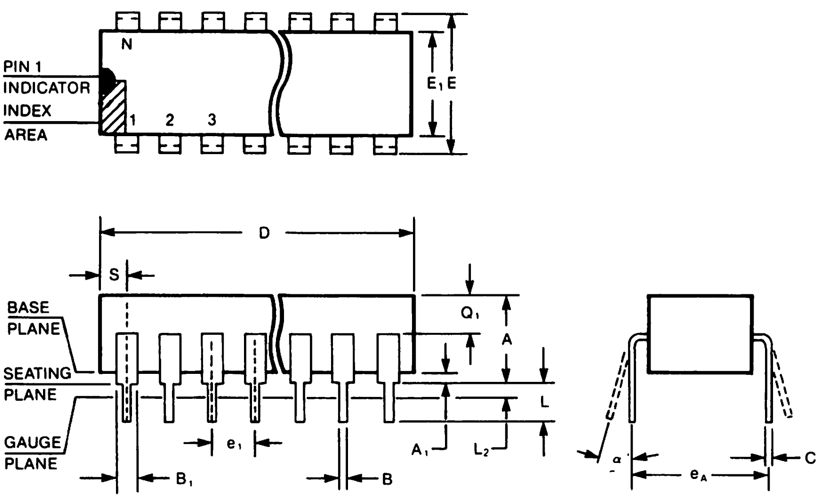
16 Lead Plastic*



	MIN.	MAX.
A	.120	.160
A_1	.020	.065
B	.014	.020
B_1	.035	.065
C	.008	.012
D	.745	.785
E_1	.240	.260
e_1	.100 Typ.	
e_A	.300 Typ.	
L	.125	.150
α	0°	15°
Q_1	.050	.085
S	.015	.060

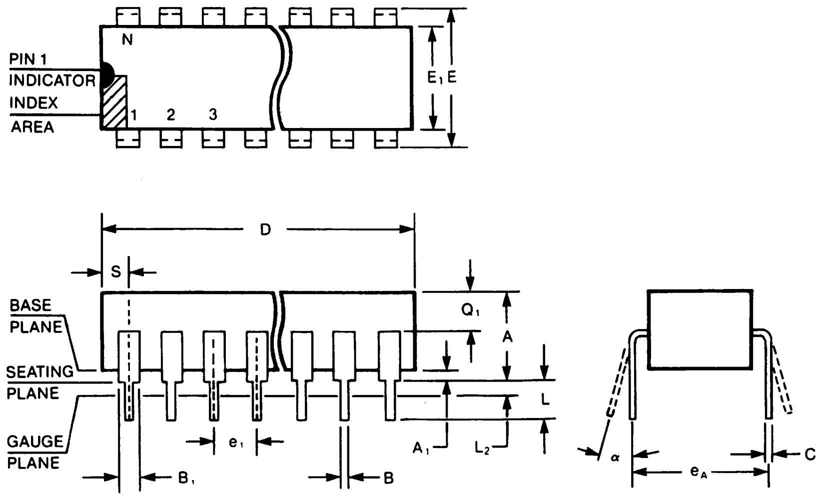
*JEDEC drawing
#MO-001AE

18 Lead Plastic



	MIN.	MAX.
A	.136	.175
A_1	.008	.040
B	.015	.021
B_1	.055	.065
C	.008	.013
D	.890	.910
E_1	.245	.255
e_1	.090	.110
e_A	.285	.315
L	.115	.145
α	2°	12°
Q_1	.060	.079
S	.040	.070

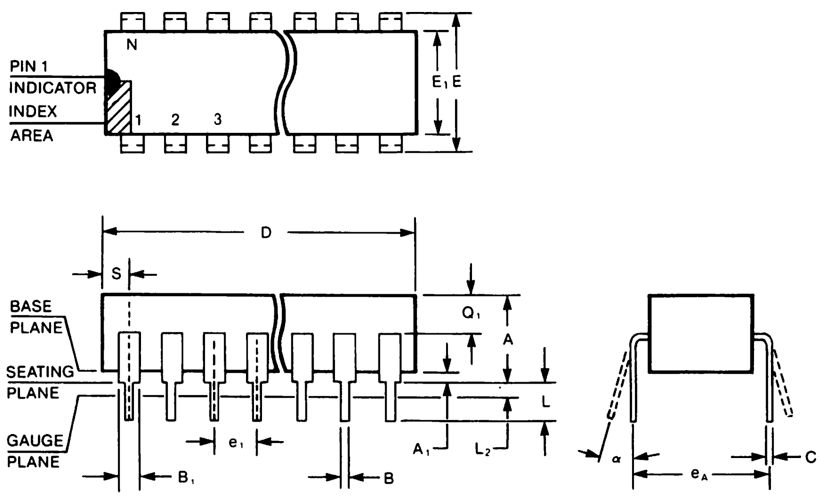
22 Lead Plastic*



	MIN.	MAX.
A	.090	.150
A_1	.020	.065
B	.014	.020
B_1	.035	.065
C	.008	.012
D	1.050	1.110
E_1	.370	.390
e_1	.100 Typ.	
e_A	.400 Typ.	
L	.120	.160
α	0°	15°
Q_1	.010	.050
S	.035	.060

*JEDEC drawing #MO-026AA

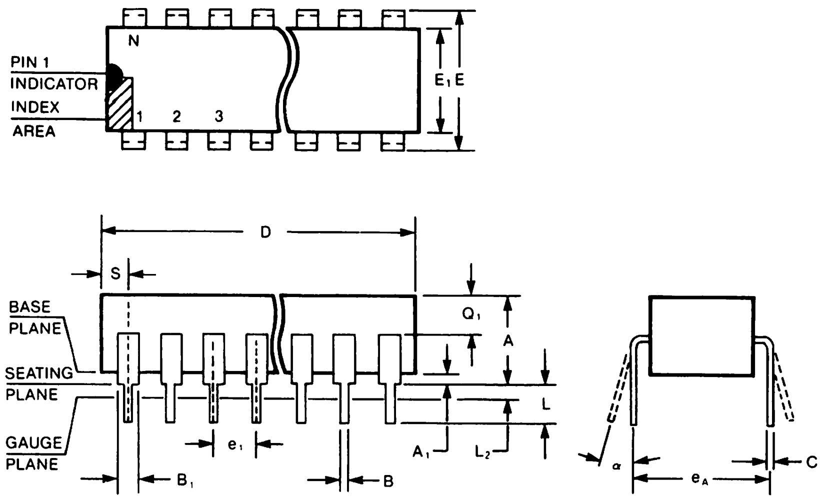
24 Lead Plastic*



	MIN.	MAX.
A	.120	.250
A_1	.020	.070
B	.016	.020
B_1	.028	.070
C	.008	.012
D	1.200	1.290
E_1	.515	.580
e_1	.100 Typ.	
e_A	.600 Typ.	
L	.100	.200
α	0°	15°
Q_1	.040	.075
S	.040	.100

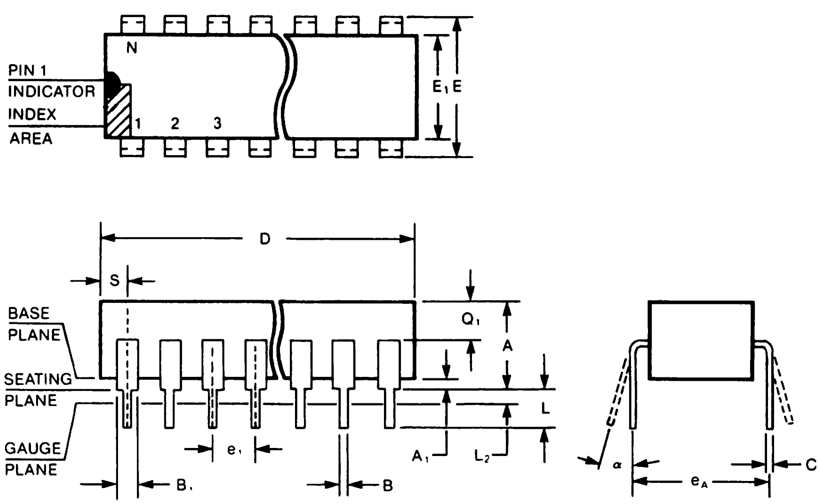
*JEDEC drawing #MO-015AA

28 Lead Plastic



	MIN.	MAX.
A	.157	.187
A_1	—	.040
B	.015	.021
B_1	.055	.065
C	.008	.013
D	1.440	1.460
E_1	.535	.545
e_1	.090	.110
e_A	.585	.615
L	.115	.145
α	4°	12°
Q_1	.070	.084
S	.060	.090

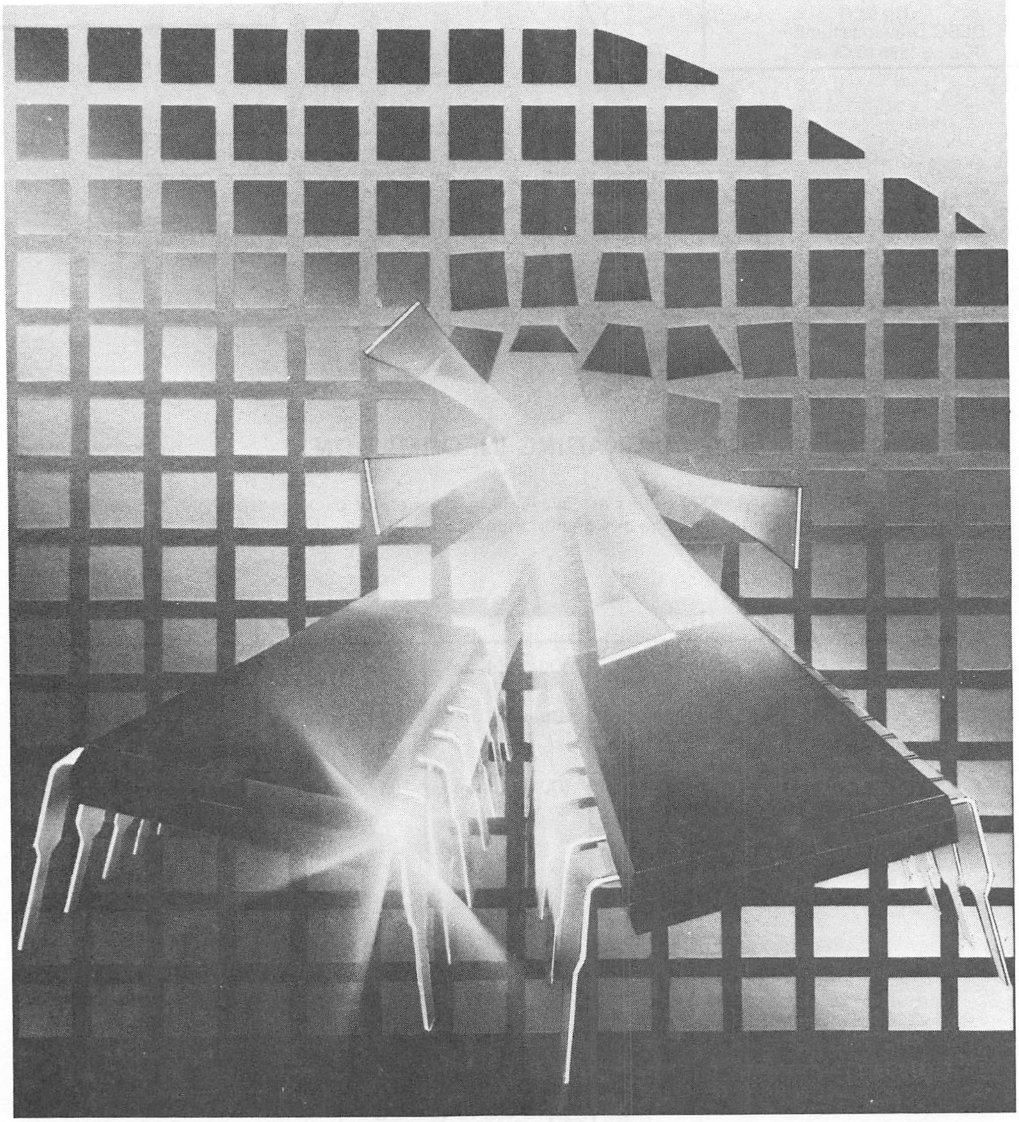
40 Lead Plastic*



	MIN.	MAX.
A	.160	.220
A_1	.000	.070
B	.015	.020
B_1	.015	.055
C	.008	.012
D	2.020	2.070
E_1	.485	.580
e_1	.100 Typ.	
e_A	.600 Typ.	
L	.100	.200
α	0°	15°
Q_1	.070	.120
S	.060	.090

*JEDEC drawing #MO-015AJ

Ordering Information



ORDERING INFORMATION

SCL 4xxxB C +

SCREENING LEVEL

SCL = Standard
BCL = High Reliability
883C = MIL-STD-883C Class B
DESC Drawing Number
JCL = 38510 Class B

DEVICE TYPE

Consists of four numerals plus one or two letters

PACKAGE TYPE

C = Cerdip (Frit-Seal Ceramic)
D = Ceramic (Welded-Seal or Side-Brazed)
E = Epoxy (Plastic)
H = Dice

SSS SOLID PLUS PROGRAM

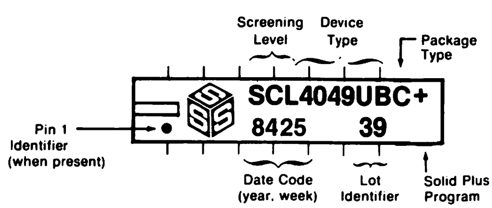
Blank = Standard
+ = Solid + Program

PACKAGING INFORMATION

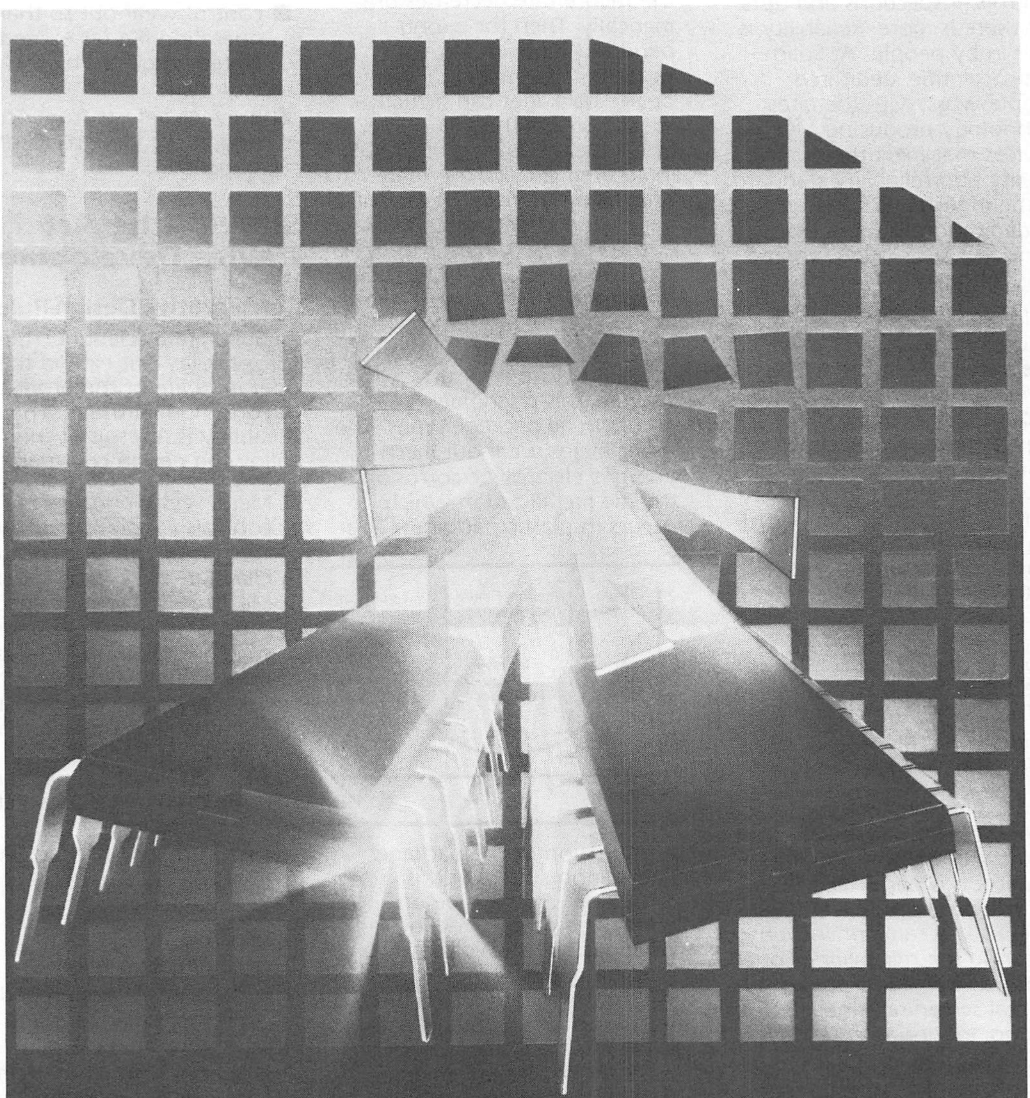
Devices in the 4000 Series are available in a variety of package types and temperature ranges. The single-letter package designator appears as a suffix to the device type.

Designator SCL	Type	Style	No. of Pins	Temperature Range
C	Cerdip (Frit-Seal)	Dual-in-Line (DIP)	14, 16, 24	−55° C to +125° C
D	Ceramic (Welded-Seal or Side-Brazed)	Dual-in-Line (DIP)	14, 16, 24	−55° C to +125° C
E	Epoxy (Plastic)	Dual-in-Line (DIP)	14, 16, 24	−40° C to +85° C
H	Dice	—	—	−55° C to +125° C

DEVICE MARKING



4000 Series High Reliability



Built-In Reliability

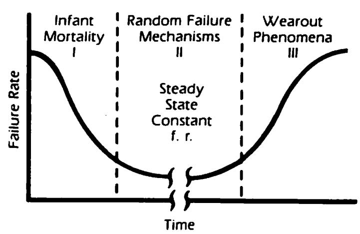
Reliability in MOS integrated circuits does not just happen—it must be built in. Built in through conservative designs, advanced wafer fabrication technology, and controlled by stringent in-process quality controls, inspections and tests. But there is more. Reliability is built in by people. At Solid State Scientific, dedicated people work with the latest technology producing MOS devices that meet the highest quality and reliability standards in the industry. SSS has proven its dedication to these high standards since 1968 when it was founded.

Solid State Scientific is a high volume manufacturer of MOS integrated circuits and offers a variety of high reliability options to meet customer requirements. Our facilities in Willow Grove, Pennsylvania have been certified by the Defense Electronics Supply Center for the production of Class B devices in accordance with MIL-M-38510.

In addition, regardless of product grade, Solid State Scientific has established definite minimum quality and reliability standards which apply across all product lines. All products are manufactured identically from incoming inspection through wafer probe of the die. Pre-seal visual inspection is performed in accordance with MIL-STD-883 level B. This same philosophy of ensuring the reliability of our products applies to environmental screening, final electrical testing and lot acceptance for packaged parts.

Integrated Circuit Reliability

CMOS integrated circuits exhibit the same basic reliability characteristics as other semiconductor devices in that the failure rate has three distinct phases. Within a relatively short time, certain failure mechanisms appear under moderate levels of stress. Failures which occur during this phase are called infant mortality failures. During infant mortality, the failure rate decreases dramatically. Then for a long period of time, infrequent random failures occur. Finally, device packages can actually wear out and the failure rate will increase again. For CMOS integrated circuits, there are only two significant wear-out mechanisms; electromigration and corrosion in plastic devices. Electromigration is a function of temperature and current density in the metallization and is influenced by the type of metal, grain structure and surface sealing. This phenomenon occurs in all package types. The other major wear-out mechanism is electrolytic corrosion of the die metallization which occurs in plastic packages. This



is a function of the package/passivation system and is influenced by the type of epoxy, the protective molding compound and chip glassivation materials.
When the failure rate is plotted as a function of time, the result is the basic bathtub curve characteristic of all semiconductor devices. While the bathtub curve is universal throughout the IC industry, actual values can vary greatly from one manufacturer to another. Solid State Scientific has many years of experience in the manufacturing of CMOS integrated circuits, and our design rules and processing techniques have been developed to:

- minimize the infant mortality failure mechanisms.
- detect potential failures before they reach the customer.
- control wear-out so that operating life far exceeds the lifetime required by the customer.
- prevent defects from occurring at the earliest possible stage.

State-of-the-Art Device Development

Conservative Design Rules

At Solid State Scientific, rules for mask lay-out extend the operating life of the product far beyond normal usage. This reliability is a result of the following design considerations:

- Metal width and spacing controls in conjunction with stringent in-process controls eliminate electro-migration. MIL-M-38510 Level B specifications call for a maximum current density in glassivated pure aluminum stripes of 5×10^5 amps/cm^2 Solid State Scientific demands no more than 1.5×10^5 amps/cm^2. Also, an absolute minimum design width for any metal line is maintained for standard industrial devices.
- Strictly controlled element spacings and sizes are specified for:
  - all diffusion widths
  - distances between pad and scribe line for leakage protection
  - spacings between elements to prevent inversion
  - spacing between the boundary of a diffusion and the contact cut for the diffusion to prevent leakage.

- metal-to-metal and pad-to-pad spacings
- pad size to insure room for a good bond
- High voltage reverse baised diodes to both V_{SS} and V_{DD} in conjunction with series resistors to protect inputs from voltage transients and ESD.

Each wafer contains its own process control test cells. This special device measures all process and design parameters that have a significant effect on yield and reliability.

Controlled Wafer Processing

Reliability Assured Through Stringent Controls

At Solid State Scientific we have one of the most highly controlled wafer processing facilities in the industry. All MOS products are manufactured in the same fabrication facility using identical materials, technology, and MIL-M-38510 procedures and controls. All SSS products are processed on a fully approved MIL-M-38510 wafer line, whether destined for the commercial or military market.

Reliability is assured through:

- a special tapered oxide process that controls the edges of all cuts in the oxide to obtain a nominal 45° angle.
- planetary rotation during metal evaporation. This technique results in a controlled oxide step with uniform metal thickness. Failure due to electron migration is eliminated.

Product Assurance Program

Table 1—Processing and Screening requirements for MIL-STD-883, MIL-M-38510 and Standard products.

	MIL-STD-883B Method In accordance with 5004 & 5005	**883C4 XXX DESC Drawing MIL-STD-883B Class B**	**MIL-M-38510 Class B**
Assembly			
Precap Visual (Cond. B)	2010B	X	X
Preconditioning			
Seal & Lot Identification		X	X
Stabilzation Bake 24 hrs @ 150°C	1008C	X	X
Temperature Cycle	1010C	X	X
Centrifute Y1	2001E	X	X
Fine Leak	1014B	X	X
Gross Leak	1014C	X	X
Test and Burn-In			
Initial Test		X	X
Static Burn-In, 160 Hr. Min. or Equiv.	1015	X	X
Final Electrical 25°C, DC and Functional (A-1, A-7)		X	X
Final Electrical AC 25°C (A-4, A-9)		X	X
Final Electrical −55°C DC and Functional (A-3, A-8)		X	X**
Final Electrical AC −55°C (A-6, A-11)		—	X**
Final Electrical +125°C DC and Functional (A-2, A-8b)		X	X**
Final Electrical AC +125°C (A-5, A-10)		—	X**
External Visual	2009	X	X

X = 100% Testing — = Not Required "(A-X)" are Subgroups

*" + " product has 168 hours of static burn-in or equivalent.

**Subgroups A-5, A-6, A-8, A-8b, A-10 and A-11 are only performed when required by the detailed specification.

- an ion-implant operation to increase the P-channel thick field inversion voltage. This allows SSS to offer the cost effectiveness of a smaller chip while maintaining the same low leakage and high voltage characteristics found in guard ring construction.
- precision phosphorous doping of the glass passivation that prevents surface inversion during the life of the device. Passivation layer thickness is carefully chosen to provide full coverage over the tapered oxide steps. This means superior long term stability and added moisture protection at the die level.
- test cells and test transistors on every wafer are probed for twelve parameters prior to metal alloying and fourteen parameters at final wafer probe. Trends are monitored continuously and variations are detected immediately. Typical parameters measured are:
  - threshold voltages of transistors
  - breakdown voltages of transistors
  - gate breakdown voltages
  - transistor contact resistance
  - metal strip fusing current

Our process controls are some of the most stringent in the industry. Every lot undergoes 100% inspection after each and every mask level operation.

Sampling Inspection

Tables 2, 3, 4 and 5 illustrate the sample criteria used to insure an LTPD requirement for military product. Sample sizes are based on the Poisson exponential binominal limit in accordance with MIL-S-19500. The tables of subgroup tests demonstrate the level of quality conformance of Hi-Rel Military and Standard products.

Table 2—Group A Electrical Sampling Inspection for Class B High-Reliability CMOS Integrated Circuits per MIL-STD-883, Method 5005

Subgroup	Test	Condition	LTPD Class B	883C4 XXX DESC Drawing MIL-STD-883B Class B	MIL-M-38510 Class B
1	DC Static Parameters	$T_A = +25°C$	2	✓	✓
2	DC Static Parameters	$T_A = +125°C$	3	✓	✓
3	DC Static Parameters	$T_A = -55°C$	5	✓	✓
4	Dynamic Parameters	$T_A = +25°C$	2	✓	✓
7	Functional Parameters	$T_A = +25°C$	2	✓	✓
9	AC Parameters	$T_A = +25°C$	2	✓	✓

Note: Performed on each inspection lot.

Table 3—Group B Sampling Inspection for Class B High-Reliability CMOS Integrated Circuits per MIL-STD-883, Method 5005

Subgroup	Test	MIL-STD-883 Method & Condition	883C4 XXX DESC Drawing MIL-STD-883B Class B	MIL-M-38510 Class B
1	Physical Dimension	2016 —	✓	✓
2	Resistance to Solvents	2015 —	✓	✓
3	Solderability	2003 Soldering Temperature 245°C ± 5°C	✓	✓
4	Internal Visual and Mechanical	2014 —	✓	✓
5	Bond Strength	2011	✓	✓
6	Internal Water Vapor Content	1018 —	✓	✓
7	Fine and Gross Leak	1014B, 1014C —	✓	✓
9	V_{ZAP}	Per Detailed Specification	✓	✓

Note: Performed on each package type and lead finish for each week of seal (date code).

Table 4—Group C Die-Related Tests for Class B High-Reliability CMOS Integrated Circuits per MIL-STD-883, Method 5005

Subgroup	Test	MIL-STD-883 Method & Condition	883C4 XXX DESC Drawing MIL-STD-883B Class B	MIL-M-38510 Class B
1	Operating Life	1005, T_A = 125°C, 1000 hrs. or equiv.	✓	✓
	Electrical Parameters	As Specified	✓	✓
2	Temperature Cycling	1010 Test Condition C	✓	✓
	Constant Acceleration	2001 Test Condition E	✓	✓
	Fine Leak	1014B —	✓	✓
	Gross Leak	1014C —	✓	✓
	Visual Examination	1010 or 1011	✓	✓
	Electrical Parameters	As Specified	✓	✓

Note: Performed every 13 weeks for each microcircuit group or as specified in the detailed drawing.

Table 5—Group D Package-Related Tests for High-Reliability CMOS Integrated Circuits per MIL-STD-883, Method 5005

Subgroup	Test	MIL-STD-883 Method & Condition	883C4 XXX DESC Drawing MIL-STD-883B Class B	MIL-M-38510 Class B
1	Physical Dimensions	2016 —	✓	✓
2	Lead Integrity	2004 —	✓	✓
	Fine Leak	1014B —	✓	✓
	Gross Leak	1014C —	✓	✓
3	Thermal Shock	1011 Test Condition B Min.	✓	✓
	Temperature Cycling	1010 Test Condition C 100 cycles	✓	✓
	Moisture Resistance	1004 —	✓	✓
	Fine Leak	1014 Test Condition B	✓	✓
	Gross Leak	1014 Test Condition C	✓	✓
	Visual Examination	Per Visual of Method 1004 and 1010	✓	✓
	Electrical Parameters	As Specified	✓	✓
4	Mechanical Shock	2002 Test Condition B	✓	✓
	Vibration, var. freq.	2007 Test Condition A	✓	✓
	Constant Acceleration, Y1 plane	2001 Test Condition E	✓	✓
	Fine Leak	1014 Test Condition B	✓	✓
	Gross Leak	1014 Test Condition C	✓	✓
	Visual Examination	1010 or 1011	✓	✓
	Electrical Parameters	As Specified	✓	✓
5	Salt Atmosphere	1009 Test Condition A	✓	✓
	Fine Leak	1014B —	✓	✓
	Gross Leak	1014C —	✓	✓
	Visual Examination	Per Visual of Method 1009	✓	✓
6	Internal Water Vapor Content	1018 5000ppm Max.	✓	✓
7	Adhesion of Lead Finish	2025 As Applicable	✓	✓
8	Lid Torque	2024 As Applicable	✓	✓

Note: Performed every 26 weeks or as specified in the detailed drawing.

Summary

Solid State Scientific has extensive experience in all aspects of CMOS integrated circuit technology. This expertise dates back to 1968 with the design and development of custom CMOS devices for space applications. In 1970 SSS began manufacturing the 4000 Series standard circuits. Today, with more than a decade of CMOS experience, SSS is respected as a major supplier of a wide variety of CMOS products.

Over the years, our products have established a reputation for outstanding reliability in applications as varied as data processing, military and space systems, automotive, and timekeeping products. This quality and reliability results from a combination of:

- conservative design rules
- advanced wafer fabrication capabilities
- stringent in-process controls and inspection procedures

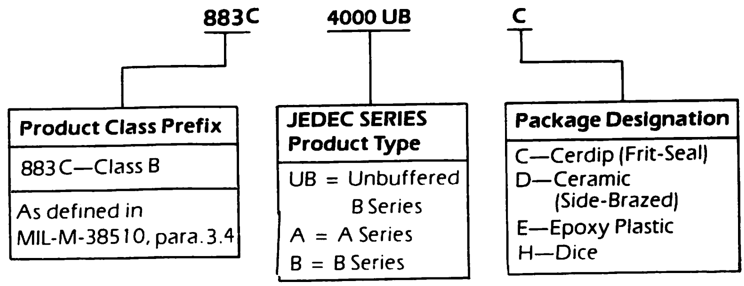
In addition, Solid State Scientific adds one more ingredient to every device; a company-wide dedication to customer satisfaction.

QPL Products

MIL-STD-883C Class B CMOS 4000 Series Products

CMOS 4000 Series devices are available in Cerdip (Frit-Seal) (C), Ceramic (Side-Brazed) (D) packages, and Dice (H).

Figure 1
MIL-STD-883C—Device Nomenclature

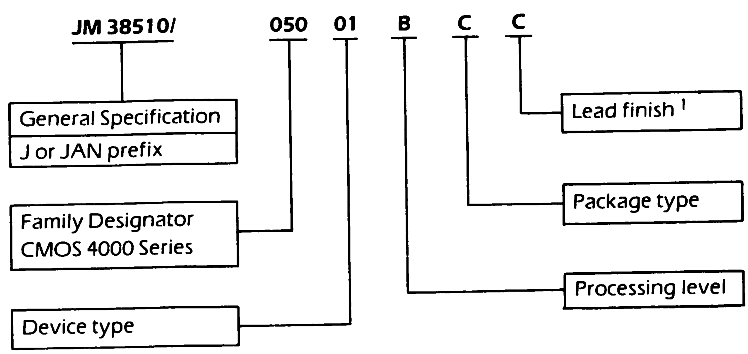


MIL-M-38510 Class B CMOS 4000 Series, QPL Accepted Product

Contact SSS Regional Sales Offices for the current listing of MIL-M-38510 Class B, QPL Accepted Products.

MIL-M-38510 CMOS 4000 Series devices are available in Ceramic (Side-Brazed) and Cerdip (Frit-Seal) packages.

Figure 2
MIL-M-38510—Device Nomenclature



MIL-M-38510 Package Type

C	14-lead 1/4 x 3/4 DIP [1]
E	16-lead 1/4 x 7/8 DIP [1]

MIL-M-38510 Lead Finish [1]

A	Hot Solder Dip	C	Gold Plate
B	Tin Plate	X	Optional

1. Note: Hot Solder Dip and Tin Plate lead finishes are available in Cerdip (Frit-Seal) packages. Tin plate and gold lead finishes are available in Ceramic (Side-Brazed) packages. When ordering tin plate lead finishes, specify package preferred.

Notes

Notes

Notes

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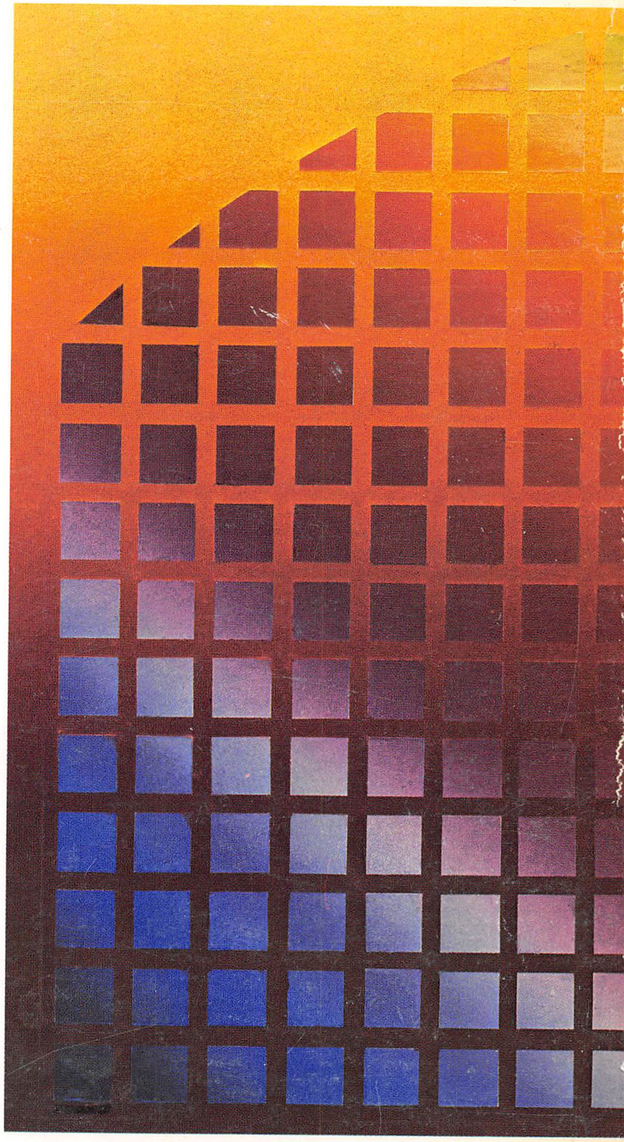

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